Programmable Gate Driving Platform for Easy Device Driving and Performance Tuning

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Background and Objectives

• Power semiconductors have drastically different gate or base driving requirements
• Various kinds of driving schemes have been developed to tackle switching transient issues
• Objectives
  ○ A programmable gate driving platform capable of driving most power semiconductor devices
  ○ Flexible to adjust transient performance but still replicable with off-the-shelf components

Technical Approaches

• Gate driver topology to allow easy reconfiguration of driving schemes
• PC to FPGA control interface to allow precision switching timing control and supply voltage control
• Miniaturized connection from gate driver to power semiconductor to reduce gate loop inductance
• Demonstration with Si IGBT, SiC MOSFET, SiC BJT, GaN HFET to validate the capabilities

Conclusions

• Programmable driver platform capable of emulating both voltage, impedance and current source driving is demonstrated
• The platform enables fast device characterization under different gate driving schemes and allows easy gate driving optimization
Programmable Gate Driving Architecture

- HDLC over UART to control both the switching timings and supply voltages
- Supply voltage control is achieved with digital potentiometers in the feedback loop of either LDO or Buck-Boost converter
- Castellated hole connections to minimize the gate loop inductance

- The programmable gate driver can emulate
  - Up to 9 level voltage source driving
  - Complex impedance driving
  - Current source driving

### General Topology

- **Impedance Driving**
- **Current Source Driving**
Gate Driving Performance Tuning

- Current source driving for SiC BJT significantly reduces the turn-off loss
- GaN HFET crosstalk mitigation demonstrates the performance tuning

GaN HFET Crosstalk Mitigation by Tuning Negative Voltage and Pulse Time

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