A Test Scheme for the Comprehensive Qualification of MMC Submodule Based on 10 kV SiC MOSFET under High $dv/dt$

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Summary

Background and motivation:
• Modular multilevel converters (MMCs) based on 10 kV SiC MOSFETs are promising in medium voltage applications
• Numerous challenges due to high $dv/dt$ and submodule voltage brought by 10 kV SiC MOSFETs: insulation design, noise immunity, etc
• Comprehensive submodule testing is critical and necessary to find problems at the submodule level

Proposed test scheme for MMC submodules:
• Simple test scheme: only 3 steps; test circuit with simple configuration
• AC-DC continuous test with two cascaded submodules resembles real MMC operation
• With designed modulation, two submodules switching simultaneously to generate high $dv/dt$
• Simple open loop method designed to achieve submodule voltage balancing

Conclusion:
• The proposed simple test scheme features an ac-dc continuous test circuit with two submodules in series to resemble real MMC operation
• The developed ac-dc continuous test circuit can test noise immunity under high $dv/dt$, thermal design, and insulation design of the MMC submodule simultaneously
• Submodule voltage balancing is realized with a simple open loop method with external parallel resistor
Proposed Test Scheme

AC-DC continuous test circuit: two MMC submodules in series

Modulation scheme: bipolar SPWM modulation

Submodule under test

Submodule with controllable $dv/dt$

AC-DC continuous test

Thermal design

Insulation design

Capability to withstand high $dv/dt$

Open loop voltage balancing of submodules

Submodule 1

Submodule 2

Without external parallel resistor

With external parallel resistor

Without parallel resistor for voltage balancing

With 100 kΩ parallel resistor for voltage balancing

Simulation results ($V_g=6$ kV)

$I_{load,pk} = \frac{mV_g}{2\pi f_{line}L_{load} + R_{load}}$
Experimental Setup and Results

• 500 kΩ/100 W balancing resistor for each submodule; MMC arm inductors used as load
• Proposed ac-dc test circuit for MMC submodules validated at 6 kV dc-link voltage
• 2X $dv/dt$ generated for submodule under test confirmed in the test
• Submodule voltage balancing achieved with the developed open loop method

\[ V_g = 2.1 \text{ kV} \]
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