Three-Phase DC Capacitor-Less
Solid-State Variable Capacitor

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Abstract—Grid-connected full bridge inverters typically have a bulky electrolytic dc capacitor to absorb the unbalanced power from the ac side. The electrolytic capacitors are vulnerable and normally have shorter lifetime than other components in the converter. In most full-bridge inverter applications, the dc voltage is required to be relatively constant. However, in reactive power compensation applications, such as solid-state variable capacitor (SSVC), the constant dc-bus voltage is unnecessary since the dc bus is floating. This paper proposes a three-phase dc capacitor-less SSVC, which removes the electrolytic dc capacitor from the circuit by releasing the constraints on dc bus voltage fluctuation. The dc voltage is supported by ac side voltage directly. The remaining dc capacitance has a value of only 3% compared to that of the conventional three-phase SSVC. The proposed three-phase dc capacitor-less SSVC is validated by simulation.

Keywords—SSVC, dc capacitor, reactive power, ripple voltage

I. INTRODUCTION

The conventional single-phase solid-state variable capacitor (SSVC) adopts H-bridge configuration to mimic the behavior of a capacitor. The H-bridge configuration suffers from the ripple power pulsating at twice the line frequency (2-ω). Conventionally, the ripple power is filtered by a bulky dc capacitor bank, resulting in low power density. Normally, to generate 1-p.u. reactive power, the H-bridge ends up with 10-p.u. dc capacitor [1]. Several power decoupling methods have been proposed to deal with this 2-ω ripple power in single-phase applications [2]–[11]. The fundamental idea of power decoupling methods is to transfer most of the ripple power from the dc capacitor to an extra energy storage component with relatively smaller size.

Unlike the single-phase inverter, the three-phase full bridge inverter does not need to have bulky dc capacitor because the 2-ω ripple power does not exist in a balanced three-phase system. However, sufficient dc capacitance is still necessary since the dc capacitor needs to absorb the ripple power introduced by an unbalanced load condition. The three-phase inverter dc capacitance is determined by the worst expected unbalanced condition. A constant dc voltage is not always necessary in applications such as SSVC because the dc capacitor is floating. Several control methods have been proposed to allow larger dc voltage ripple on the dc bus by increasing the dc voltage level [12]–[14], which allows a smaller dc-bus capacitance. The dc capacitance relies on the capability of the proposed control and the allowed dc voltage variation. Liu et al. [15] proposed a dc capacitor-less active capacitor that eliminates the dc capacitor from the single phase inverter by utilizing the grid voltage to support the dc bus voltage.

This paper proposes a three-phase dc capacitor-less SSVC that utilizes the grid voltage to support the dc bus voltage. Therefore, only an extremely small dc capacitor is needed on the dc bus. This paper is organized as follows. Section II explains the operating principle of the proposed three-phase dc capacitor-less SSVC. Section III provides the mathematical model of the proposed circuit. The control strategy of the proposed SSVC is presented in Section IV. The simulation results are provided in Section V for verification purposes.

II. OPERATING PRINCIPLE OF THREE-PHASE DC CAPACITOR-LESS SSVC

The basic idea is to rely on the grid side ac voltage to support the dc link voltage so that the dc link capacitor only processes the switching-frequency components. Since the dc capacitor does not need to filter the low frequency harmonics, the bulky electrolytic capacitor is no longer needed. Only a snubber capacitor remains in the hardware. Fig. 1 shows the three-phase dc capacitor-less SSVC circuits. The dc voltage is supported by

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alternating through the three line voltages (whichever is the largest).

At steady state, the phase voltages are

\[ v_a = \sqrt{2} V_s \sin(\omega t), \quad (1) \]
\[ v_b = \sqrt{2} V_s \sin(\omega t - 2\pi/3), \quad (2) \]
\[ v_c = \sqrt{2} V_s \sin(\omega t + 2\pi/3). \quad (3) \]

At steady state, the line currents are

\[ i_a = \sqrt{2} I_s \cos(\omega t), \quad (4) \]
\[ i_b = \sqrt{2} I_s \cos(\omega t - 2\pi/3), \quad (5) \]
\[ i_c = \sqrt{2} I_s \cos(\omega t + 2\pi/3), \quad (6) \]

where \( V_s \) is the phase voltage RMS value, \( I_s \) is the line current RMS value, and \( \omega \) is the line frequency. The resulting line voltages are

\[ v_{ab} = v_a - v_b = \sqrt{6} V_s \sin(\omega t + \pi/6), \quad (7) \]
\[ v_{bc} = v_b - v_c = \sqrt{6} V_s \sin(\omega t - \pi/2), \quad (8) \]
\[ v_{ca} = v_c - v_a = \sqrt{6} V_s \sin(\omega t + 5\pi/6). \quad (9) \]

Since \( v_{ab}, v_{bc}, \) and \( v_{ca} \) are alternatingly supporting the dc-bus voltage, the dc voltage can be formulated as

\[ v_{dc} = v_{ab}G_{ab} + v_{bc}G_{bc} + v_{ca}G_{ca}, \quad (10) \]

where \( G_{ij} \) is a gate function,

\[ G_{ab} = \begin{cases} 
1, & \pi/6 \leq \omega t \leq \pi/2 \\text{else} \\
-1, & 7\pi/6 \leq \omega t \leq 3\pi/2 
\end{cases} \quad (11) \]

\[ G_{bc} = \begin{cases} 
1, & 5\pi/6 \leq \omega t \leq 7\pi/6 \\text{else} \\
-1, & -\pi/6 \leq \omega t \leq \pi/6 
\end{cases} \quad (12) \]

\[ G_{ca} = \begin{cases} 
1, & -\pi/2 \leq \omega t \leq -\pi/6 \\text{else} \\
0, & \pi/2 \leq \omega t \leq 5\pi/6 
\end{cases} \quad (13) \]

When \( G_{ab} = 1, v_{ab} \) is selected to support the dc voltage. The switches \( S_{a1} S_{b2} \) are on and \( S_{a2} S_{b1} \) are off. The remaining phase operates at a duty cycle \( D \), where \( D \) satisfies

\[ v_{cb} = D \cdot v_{dc}. \quad (14) \]

Since \( v_{dc} = v_{ab} = \sqrt{6} V_s \sin(\omega t + \pi/6) \), combining (8) and (14) yields

\[ D = \frac{v_{cb}}{v_{dc}} = \frac{\sqrt{6} V_s \sin(\omega t + \pi/6)}{\sqrt{6} V_s \sin(\omega t + \pi/6)} = \frac{1}{\tan \omega t \cos(\pi/6) + \sin(\pi/6)}. \quad (15) \]

The linearization of \( D \) has a good approximation within the region of \( \omega t \in [\pi/6 \pi/2] \), therefore

\[ D \approx -\frac{3}{\pi} (\omega t - \pi/2). \quad (16) \]

\(-3/\pi\) is the slope of the \( D \) reference, the constant term \(-1/2\pi\) corrects the time offset. The comparison of (15) and (16) is illustrated in Fig. 2. The minor mismatch can be compensated by closed-loop control which will be presented in later sections. Similar to \( G_{ab} = 1 \), when \( G_{ab} = -1, v_{bc} \) is selected to support the dc voltage. The switches \( S_{a2} S_{b1} \) are on and \( S_{a1} S_{b2} \) are off. The remaining phase operates at the duty cycle \( D \), where \( D \) satisfies

\[ D \approx \frac{3}{\pi} (\omega t - \frac{\pi}{2}). \quad (17) \]

where \( \frac{\pi}{2} \) is a constant that corrects the time offset. The derivation of duty cycle in other regions of time is similar and therefore omitted in this paper. The complete modulation of the three-phase dc capacitor-less SSVC is shown in Fig. 2. The lower switches \( S_{a2}, S_{b2}, \) and \( S_{c2} \) are complimentary to \( S_{a1}, S_{b1}, \) and \( S_{c1} \), respectively.

III. MODELING OF DC CAPACITOR-LESS SSVC

A. External Dynamic Model

The external dynamic model of the proposed three-phase dc capacitor-less SSVC is similar to a three-phase inverter. Fig. 3 shows the equivalent circuit of the three-phase SSVC system in \( d-q \) frame. \( V_i \) is the source voltage; \( V' \) is the output voltage of SSVC converter at the bridge circuit terminal. \( I_s \) is the ac current, \( L_s \) is the filtering inductance, and \( R_s \) is the equivalent circuit resistance. The \( abc \) frame to \( dq \) frame transformation is formulated as follows,

\[ V_d = \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} \quad (18) \]

Fig. 2 Modulation strategy of three-phase dc capacitor-less SSVC.

Fig. 3. Equivalent circuit of the three-phase SSVC in \( d-q \) frame.
\[
\begin{align*}
&= \frac{2}{3} \begin{bmatrix}
\cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3})
\end{bmatrix}
\begin{bmatrix}
\frac{1}{2} \\
\frac{1}{2} \\
\frac{1}{2}
\end{bmatrix}
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix}, \\
&= \frac{2}{3} \begin{bmatrix}
\sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3})
\end{bmatrix}
\begin{bmatrix}
\frac{1}{2} \\
\frac{1}{2} \\
\frac{1}{2}
\end{bmatrix}
\begin{bmatrix}
i_d \\
i_q \\
i_0
\end{bmatrix}.
\end{align*}
\]

where \(v_c\) is the converter midpoint output voltage.

\[I_s = \begin{bmatrix}
i_d \\
i_q \\
i_0
\end{bmatrix}\]

\[= \frac{2}{3} \begin{bmatrix}
\sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3})
\end{bmatrix}
\begin{bmatrix}
\frac{1}{2} \\
\frac{1}{2} \\
\frac{1}{2}
\end{bmatrix}
\begin{bmatrix}
i_d \\
i_q \\
i_0
\end{bmatrix}.
\]

In three phase three wire system, the sum of all phases currents is zero,

\[i_a + i_b + i_c = 0.
\]

Therefore,

\[i_0 = 0.
\]

The active power absorbed by the inverter is

\[p = \frac{3}{2} v_d i_d + \frac{3}{2} v_q i_q.
\]

The reactive power absorbed by the inverter is

\[q = \frac{3}{2} v_d i_q - \frac{3}{2} v_q i_d.
\]

From the equivalent circuit, the dynamic behavior of the converter can be formulated as

\[L_s \frac{di_s}{dt} + R_s I_s = V_s - v_c.
\]

Since both the magnitude and the phase of \(I_s\) are functions of time, (25) can be re-written as,

\[L_s \frac{di_s}{dt} + \omega L_s \times I_s + R_s I_s = V_s - v_c,
\]

or

\[L_s \frac{di_s}{dt} + \omega L_s \times I_s + R_s I_s = V_s - v_c.
\]

\[L_s \frac{di_s}{dt} + \omega L_s \times I_s + R_s I_s = V_s - V_c.
\]

Fig. 4 shows the block diagram of the SSVC external dynamics derived from (26) and (27). Fig. 4 shows that the active current \(i_d\) and reactive current \(i_q\) are coupled with each other through the ac filtering inductance \(L_s\).

B. Internal Dynamic Model

The SSVC contains a dc capacitor. The dynamics of the dc capacitor are analyzed in this section. In instantaneous power theory [16], the instantaneous reactive power \(q\) does not affect the dc link capacitor voltage. Only the instantaneous active power \(p\) is accumulated in dc link capacitor. Therefore,

\[p_df = \frac{3}{2} v_d i_d + \frac{3}{2} v_q i_q = C_d v_d \frac{dvdc}{dt},
\]

where \(p_d\) is the instantaneous active power seen by the dc link. The dc capacitor voltage dynamic (28) will be used to compensate the dc voltage in later sections.

IV. CONTROL STRATEGY

The SSVC’s inherent purpose is to generate reactive power. Therefore, \(p\) and \(q\) should be controlled accordingly. From (23) and (24), the instantaneous power can be simplified as follows if \(i_d\) is controlled to 0.

\[p = \frac{3}{2} v_d i_d,
\]

\[q = \frac{3}{2} v_d i_q.
\]

This is normally the case for SSVC since the SSVC provides reactive power only. In order to generate the required reactive power, the active current and reactive current controller are established in this paper. The complete current control is shown in Fig. 5. The cross-coupling terms with \(\omega L_s\) are small and therefore neglected.

\(i_d\) and \(i_q\) are the active current and reactive current, respectively. The coupling effect of active and reactive current can be neglected in practice since the term \(\omega i_{dq} L_s\) is relatively small.

Fig. 4. Block diagram of the SSVC external dynamics.
The dc capacitor needs to be compensated with proper instantaneous active power in order to follow the fluctuating dc voltage. From (29) and (30):

\[
\frac{3}{2}v_q i_q = C_{dc} \frac{dv_{dc}}{dt} . \tag{31}
\]

Take \(v_{dc} = v_{ab}\) (from \(-\pi/6\) to \(\pi/6\)) for example.

\[
C_{dc} \frac{dv_{dc}}{dt} = C_{dc} \sqrt{V_s} \sin(\omega t - \pi/2) \frac{d}{dt} (\sqrt{V_s} \sin(\omega t - \pi/2)) \tag{32}
\]

\[
C_{dc} \frac{dv_{dc}}{dt} = 6C_{dc} V_s^2 \sin(\omega t - \pi/2) \frac{d}{dt} (\sin(\omega t - \pi/2) \cos(\omega t - \pi/2)) \tag{33}
\]

\[
C_{dc} \frac{dv_{dc}}{dt} = 6\omega C_{dc} V_s^2 \cos(\omega t - \pi/2) \cos(\omega t) - 6\omega C_{dc} V_s^2 \sin(\omega t - \pi/2) \sin(\omega t) \tag{34}
\]

\[
C_{dc} \frac{dv_{dc}}{dt} = -6\omega C_{dc} V_s^2 \cos(\omega t) \sin(\omega t) \tag{35}
\]

When \(-\pi/6 < \omega t < \pi/6\), \(\cos \omega t \approx 1\) and \(\sin \omega t \approx \omega t\). Therefore, (35) can be re-written as

\[
C_{dc} \frac{dv_{dc}}{dt} = -6\omega C_{dc} V_s^2 \omega t . \tag{36}
\]

Insert (36) into (31),

\[
\frac{3}{2} v_q i_q = -6\omega^2 C_{dc} V_s^2 \omega t , \tag{37}
\]

\[
v_q = -4\omega^2 C_{dc} V_s^2 \omega t / i_q . \tag{38}
\]

In order to compensate the dc voltage to follow the desired waveform, a feedforward \(v_q^*\) component needs to be added to the final \(v_q^*\) reference. The complete control diagram of three-phase dc capacitor-less SSVC is shown in Fig. 5.

V. SIMULATION

To verify the proposed three-phase dc capacitor-less SSVC, the simulation is conducted in Matlab. The key parameters of the simulation study are summarized in Table I. The schematic of the simulation circuit is shown in Fig. 1.
maintaining the dc link voltage fluctuation. This compensation follows (38). Fig. 8 shows the current waveforms with and without the $v_q$ compensation. Fig. 9 shows the converter dynamics with a step change of reactive power generation.

VI. CONCLUSION

Full bridge inverters typically have bulky electrolytic dc capacitor to absorb the unbalanced power from the ac side. The electrolytic capacitors are vulnerable and normally have shorter lifetime than other components in the converter. In most full-bridge inverter applications, the dc voltage is required to be relatively constant. However, in reactive power compensation applications, the constant dc-bus voltage is unnecessary since the dc bus is floating.

This paper proposes a three-phase dc capacitor-less SSVC, which removes the electrolytic dc capacitor from the circuit by releasing the constraints on dc bus voltage fluctuation. The dc voltage is supported by ac side voltage directly. The remaining dc capacitance required is only 3% compared to that of the conventional three-phase SSVC. The proposed three-phase dc capacitor-less SSVC is validated by simulation.

REFERENCES


The waveforms of the three-phase dc capacitor-less SSVC at steady state are shown in Fig. 6. Fig. 6(a) shows the line voltages and the dc link voltage. From Fig. 6(a), the dc link voltage is clamped by the maximum line voltage. Fig. 6(b) shows the line current. Fig. 6(c) shows the phase angle between the line current and phase voltage. The converter is generating reactive power. Fig. 7 shows the $v_q$ compensation for


