An Improved Turn-on Switching Transient Model of 10 kV SiC MOSFET

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2022 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-6654-0688-8/22/$31.00 ©2022 IEEE | DOI: 10.1109/APEC43599.2022.9773432

***Abstract* — The emerging 10 kV SiC MOSFET brings great benefits for medium and high voltage applications, and is drawing increased research attention. Accurate switching transient modeling of the 10 kV SiC MOSFET is critical for successful application. Curve tracer is usually used to extract parameters needed for device modeling. However, the transconductance extracted from curve tracer is tested at low voltage, which is different from the transconductance during actual high voltage turn-on switching transient because of short channel effect and drain induced barrier lowering effect. Moreover, the gate-drain capacitance extracted from curve tracer is tested at static off-state, which is also different from the gate-drain capacitance during dynamic turn-on switching transient as the MOSFET channel is turned on in this process. Conventional models based on curve tracer tests show obvious discrepancies compared to experiments. This paper investigates and characterizes the high voltage transconductance and dynamic gate-drain charge of the 10 kV SiC MOSFET during turn-on switching transient. An improved turn-on switching transient model considering these factors is proposed. Experiments with the 10 kV 20 A SiC MOSFET are conducted and verify the accuracy of the proposed improved model.**

Keywords* — *SiC, 10 kV SiC MOSFET, medium voltage application, transconductance, gate-drain charge, switching loss model.

I. Introduction

High voltage (HV, >3.3kV) silicon carbide (SiC) power semiconductor devices show superior performance in device blocking voltage and switching loss compared to silicon (Si) IGBT counterparts. HV SiC devices based converters have been drawing increased attention in medium voltage (MV) and high voltage applications such as MV motor drives [1-2] and grid interface converters [3-5]. They bring great benefits in efficiency, size, weight, and control bandwidth compared to Si IGBT based converters. The emerging 10 kV SiC MOSFETs are improving rapidly due to the maturation of SiC wafer processing technology. Accurate modeling of the 10 kV SiC MOSFET is important for successful application.

Researchers have characterized and modeled low voltage (LV, e.g., 1.2 kV and 1.7 kV) SiC MOSFETs [6-13] and those studies focus on MOSFET channel, parasitic capacitance, interaction with external circuits, and parameter extraction. For HV SiC MOSFETs, the emerging 10 kV SiC MOSFETs have been characterized to understand their characteristics in recent studies [14-20]. Some literature have modeled the 10 kV SiC MOSFETs [15, 17, 21]. The temperature-dependent steady-state and switching transient characteristic models are provided. The parasitic inductance and the nonlinearity of both transconductance and parasitic capacitance are also considered in these models.

However, parameters used in these models are based on curve tracer tested output and transfer curves, which are different from parameters that comes from high voltage switching transient measurements. The transconductance is tested with curve tracer at low voltage (e.g., 20V). But the current rise stage during the turn-on switching transient is under high drain-source voltage of the SiC MOSFET. Due to the short channel effect and drain induced barrier lowering effect [22-23], the transconductance varies under different drain-source voltage. The MOSFET capacitances are tested with the curve tracer at off-state. But the voltage fall stage during turn-on switching transient is under the MOSFET channel turned-on condition. The dynamic gate-drain charge during voltage fall stage is different from the gate-drain charge calculated from the C-V curve tested with a curve tracer. The high voltage transconductance and dynamic gate-drain charge of 10 kV SiC MOSFET during turn-on transient has not been investigated in literature.

This paper studies a 10 kV 20 A SiC MOSFET as shown in Fig. 1, which uses the 3rd generation 10 kV SiC MOSFET die developed by Wolfspeed and packaged by Powerex. The high voltage transconductance and dynamic gate-drain charge of the 10 kV SiC MOSFET during turn-on switching transient are investigated and characterized. An improved turn-on switching transient model of 10 kV SiC MOSFET is proposed and verified with experimental results.

Fig. 1. 10 kV 20 A SiC MOSFET.

II. Conventional Model

The simplified field cell structure of the 10 kV SiC MOSFET is shown in Fig. 2. The conventional model is briefly illustrated.

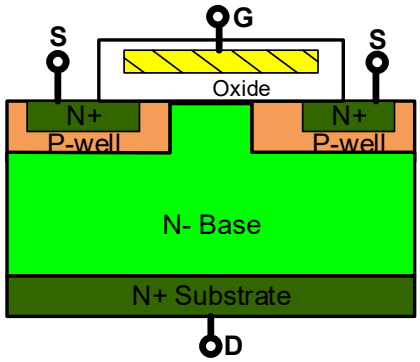


Fig. 2. Cell structure of the 10 kV SiC MOSFET.

For output characteristics, different from Si IGBTs and LV SiC MOSFETs, the voltage drop on base resistance R_B is much higher than that on the channel in the ohmic region. The on-state resistance R_{dson} is mainly determined by R_B. The R_{dson} can be extracted from ohmic region of the output curve tested with curve tracer. The body P-i-N diode can be described as (1).

$$v_{SD,PiN} = v_{PN} + i_d R_B \tag{1}$$

Here v_{pN} is the voltage drop in the p-n junction, which can be extracted from reverse conduction curve tested with curve tracer.

For channel current model, in the ohmic region, the channel current i_{ch} can be described as (2).

$$i_{ch} = k_p\left(v_{gs} - v_T - \frac{v_{ds}}{2}\right)v_{ds} \tag{2}$$

In the saturation region, a quadratic formula can be used to describe the relationship between gate-source voltage v_{gs} and channel current i_{ch} as (3).

$$i_{ch} = \frac{k_p}{2}\left(v_{gs} - v_T\right)^2 \tag{3}$$

Here v_T denotes the gate threshold voltage and k_p is the saturation current transconductance factor (A/V^2). Usually, v_T and k_p are extracted from transfer curve tested with curve tracer. However, due to the short channel effect and drain induced barrier lowering effect, saturation current transconductance factor k_p will also varies as v_{ds} varies.

For parasitic capacitance model, the internal parasitic capacitance C_{gs}, C_{gd}, and C_{ds} can be measured by curve tracer. C_{gs} does not change with V_{ds} but may vary with V_{gs}. C_{gd} and C_{ds} are V_{ds} dependent. With the consideration of the kink in the C-V curves included by the ion implantation, C_{gd} can be described as (4).

$$C_{gd} = \begin{cases} \dfrac{C_{gdi}}{\sqrt{v_{dg}}} & if\ v_{dg} \le v_{lim} \\ \dfrac{\dfrac{C_{gdi}}{\sqrt{v_{lim}}C_{gdb}}}{\left(v_{dg} - v_{lim}\right)^M} & \\ \dfrac{C_{gdi}}{\sqrt{v_{lim}}} + \dfrac{C_{gdb}}{\left(v_{dg} - v_{lim}\right)^M} & if\ v_{dg} \le v_{lim} \end{cases} \tag{4}$$

Here, C_{gdi} represents the capacitance of the ion implantation layer. v_{lim} is V_{dg} when the depletion region completely covers the ion implantation layer and equals to 50V. M is a voltage dependent factor which is affected by the doping in the base. These parameters can be extracted from the tested C-V curve. C_{ds} can be described with a similar formula and is not repeated here. Usually, M is 1/3 for C_{gd} and 1/2 for C_{ds}, respectively.

The parameters used in conventional model with this 10 kV 20 A SiC MOSFET are extracted and shown in Table 2 in Section V.

III. High Voltage Transconductance During Turn-on Transient

The turn-on switching transient of a SiC MOSFET can be divided into four stages: turn-on delay stage, current rise stage, voltage fall stage, and ringing stage. During the current rise stage of the turn-on switching transient, the MOSFET is in the saturation region and i_{ch} is controlled by v_{gs}. Note that v_{ds} maintains a high voltage during this stage while the transfer characteristic measured with a curve tracer is at low voltage. Transfer characteristic is impacted by v_{ds} due to the short channel effect and drain induced barrier lowering effect [22-23]. The channel current is controlled by electron emission over a potential barrier at the source. When the channel is short with a fixed gate voltage, the potential barrier will be lowered by the increased drain voltage, and thus channel current will increase. Most curve tracers are not capable to measure the transfer characteristic at high voltage (such as 7 kV) of the 10 kV SiC MOSFET.

The circuit as shown in Fig. 3 is proposed to measure the transfer characteristic at high drain-source voltage. The HV source from Spellman is capable to provide voltage up to 20 kV. The bus voltage V_{bus} and gate drive voltage V_{dr} can be adjusted to specified value.

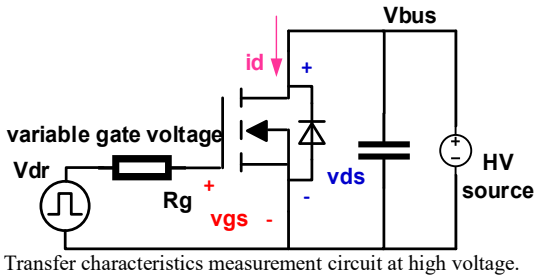


Fig. 3. Transfer characteristics measurement circuit at high voltage.

A single pulse is applied to the gate. v_{gs} and i_d are measured. With this setup, the device is tested with bus voltage from 20 V to 7 kV under varies gate voltage from 5 V to 15 V. Fig. 4 shows a typical waveform measured at 7 kV bus voltage and 8 V gate voltage. The applied pulse to the gate cannot be too long, otherwise the junction temperature rise is high. The pulse can also not be too short, otherwise the current has not become stable. The pulse is selected to be 1.1 μs in the measurement.

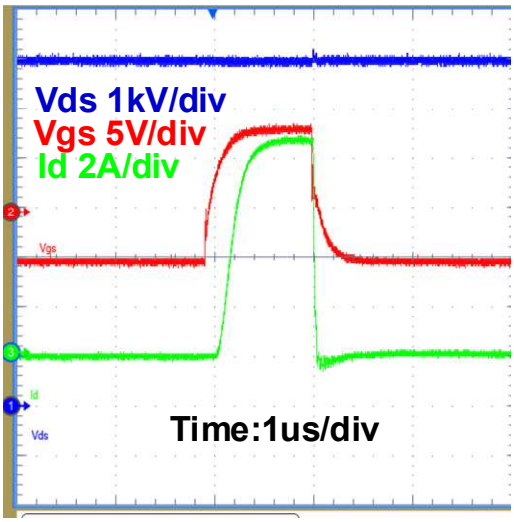


Fig. 4. Typical waveforms for transfer characteristics measurement at Vds = 7 kV and Vgs = 8 V.

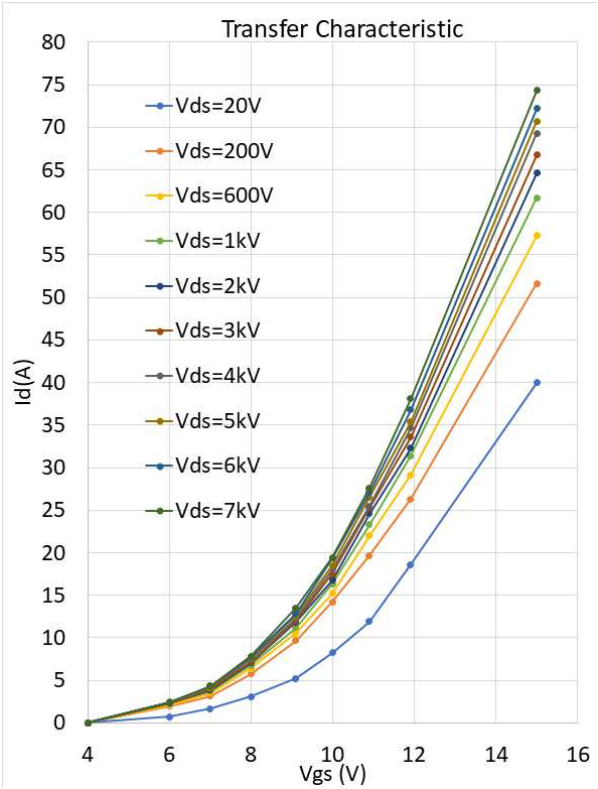


Fig. 5. Measured transfer curves (Vds: 20 V to 7 kV, Vgs: 5 V to 15 V).

The tested results are summarized in Fig. 5. It is obvious that channel current increases as v_{ds} increases. For example, at 10 V gate voltage, the channel saturation current increased from 8.27 A to 19.46 A when bus voltage increased from 20 V to 7 kV.

The extracted saturation current transconductance factor k_p (in (3)) increases from 0.7 to 1.2 when bus voltage increases from 20 V to 7 kV as shown in Fig. 6. k_p first quickly increases when bus voltage is low and then slowly increases when bus voltage is high.

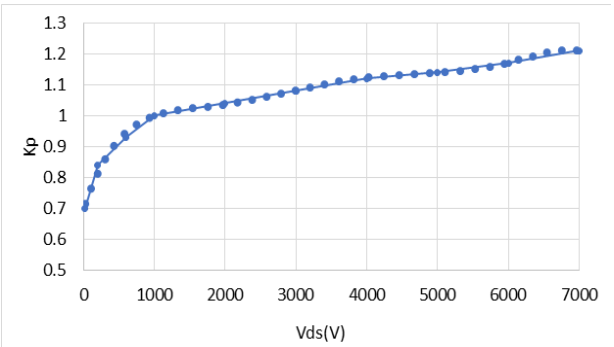


Fig. 6. Saturation current transconductance factor k_p as a function of V_{ds}.

IV. Dynamic Gate-drain Charge During Turn-on Transient

During the voltage fall stage of the turn-on switching transient, v_{gs} reaches the miller plateau voltage, and most of gate current i_g flows through gate-drain capacitance C_{gd}. C_{gd} discharge and v_{ds} falls quickly. The charge during this period is defined as Q_{gd}. The C-V curve measurement with a curve tracer is conducted at off-state of the MOSFET. But during the voltage fall stage, the channel is turned on. In addition to the original current i_{gd1} flowing through C_{gd}, additional current i_{gd2} will flow through the channel oxide capacitance as shown in Fig. 7. Thus, the dynamic charge Q_{gd_dy} is larger than the static charge Q_{gd_st} obtained from static C_{gd} measurement.

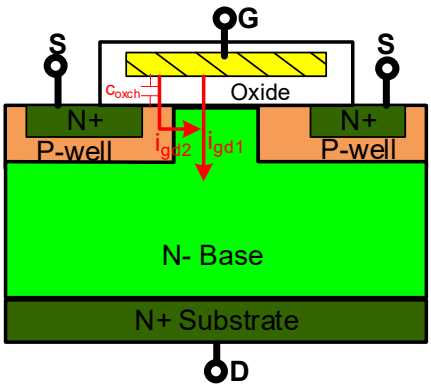


Fig. 7. Simplified illustration of i_{gd} during turn-on switching transient.

The circuit as shown in Fig. 8 is proposed to measure the dynamic charge Q_{gd_dy}, which is similar to the DPT circuit. But the gate resistance is selected to be very large to slow down the switching speed. In this test, the external gate resistance is selected as 750 Ω. Thus, the *di/dt* of the gate current is very small and the voltage drop on the parasitic inductances of gate loop can be ignored during the transient. Also, as the gate current is very small (a few milliamps), the voltage drop on the internal gate resistance can be neglected. Therefore, the measured v_{gs} is almost the same as the actual internal gate voltage of the MOSFET.

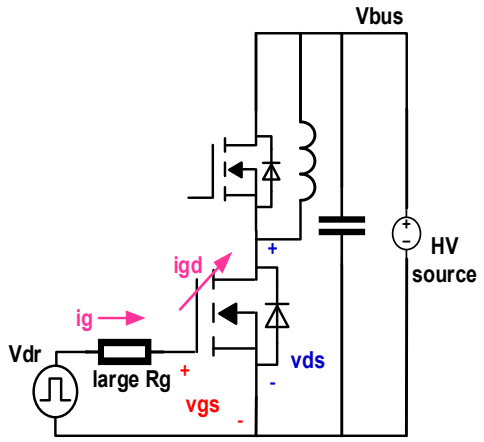


Fig. 8. Dynamic charge Q_{gd_dy} measurement circuit.

In the test, v_{ds} and i_{gd} are measured. Note that i_{gd} is not directly measured. The voltage across the external gate resistor is measured and i_g can be calculated. During the voltage fall stage, the gate voltage slightly increases and most of the gate current is discharging C_{gd}. Thus, i_{gd} is almost equal to i_g during the voltage fall stage.

Fig. 9 shows a typical waveform measured at 7 kV bus voltage. Note v_{gout} is gate driver IC output voltage measured at one terminal of the external gate resistor and $(v_{gout} - v_{gs})$ equals to the voltage across the external gate resistor. The obtained i_{gd} and v_{ds} relationship is shown in Fig. 10. The dynamic charge Q_{gd_dy} can be calculated based on (5). The actual C_{gd} during the voltage fall stage can also be obtained. The dynamic charge Q_{gd_dy} can be considered as two parts as shown in (6). One is the static charge Q_{gd_st} of the gate-drain capacitance obtained from curve tracer test at off-state. Another is the additional charge Q_{gd_ad} due to MOSFET channel turned-on. In this experiment, the charge equivalent capacitance for the additional charge Q_{gd_ad} is estimated to be around 2.2 ρF.

$$Q_{gd\_dy} = \int_{t_{vf1}}^{t_{vf2}} i_{gd}(t)dt = \int_{v_{vf1}}^{v_{vf2}} C_{gd}(v)dv \qquad (5)$$

$$Q_{gd\_dy} = Q_{gd\_st} + Q_{gd\_ad} \qquad (6)$$

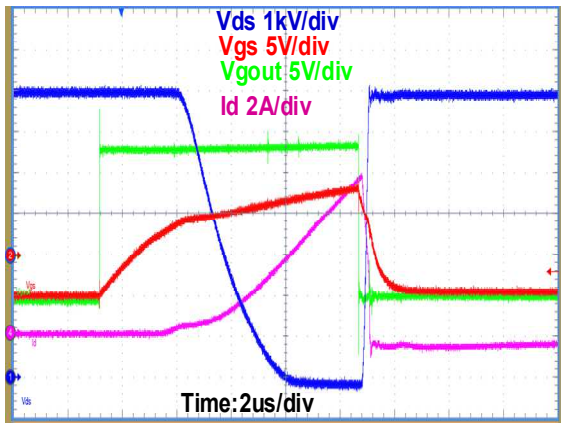


Fig. 9. Typical waveforms for dynamic Q_{gd_dy} measured at 7 kV bus voltage.

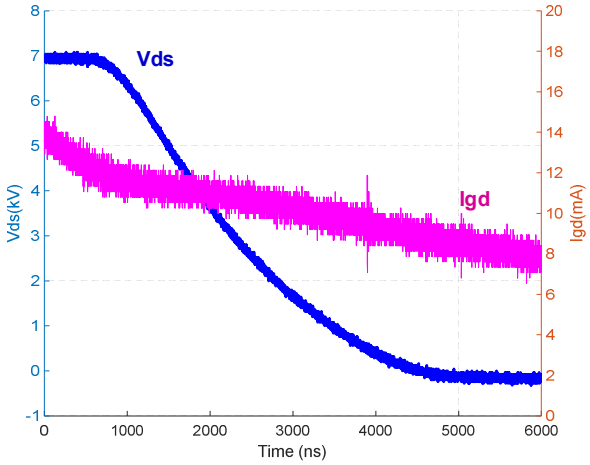


Fig. 10. Waveforms of i_{gd} and v_{ds} at 7 kV bus voltage.

V. Improved Model and Experimental Results

A DPT test platform is built with the 10 kV 20A SiC MOSFET as shown in Fig. 11. The main parameters are summarized in Table 1.

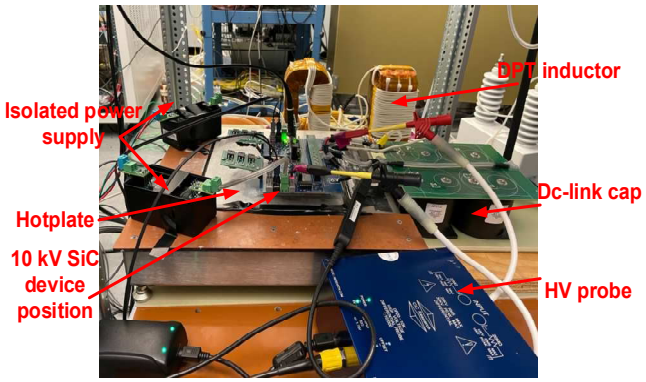


Fig. 11. 10 kV 20A SiC MOSFET based DPT test platform.

Table 1. Parameters for DPT test

Parameters	Description
semiconductor	10 kV 20 A SiC MOSFET
DPT inductor	4 mH
loop parasitic inductance	power loop 420 nH, gate loop 14 nH
gate voltage	on-state 15 V, off-state -5 V
external gate resistance	Turn-on 15 Ω, turn-off 3 Ω

First, the conventional model is developed in LTspice using Analog Behavior Model. Static characterization of the 10 kV SiC MOSFET using curve tracer (Keysight B1505A) is conducted and the main parameters used in the conventional model are extracted and summarized in Table 2.

Table 2. Parameters extracted for conventional model

Parameters	Value
saturation current transconductance factor k_p	$k_p = 0.7$
gate threshold voltage v_T	$v_T = 4.1V$ (25°C)
R_B	380 $m\Omega$
C_{gs}	6.3 nF
parameters for C_{gd}	$C_{gdi} = 1000\ pF, C_{gdb} = 50\ pF$ $M = 1/3$
parameters for C_{ds}	$C_{dsi} = 10\ nF, C_{dsb} = 2.5\ nF$ $M = 1/2$

Then, an improved model considering high voltage transconductance and dynamic gate-drain charge of the 10 kV SiC MOSFET is developed in LTspice. Based on the characterization results illustrated above, the saturation current transconductance factor k_p is represented as a function of the drain-source voltage v_{ds}. The gate-drain capacitance is represented based on characterized Q_{gd_dy} which is also a function of the drain-source voltage v_{ds}.

The experiments are conducted at different operation conditions and results are compared with models. Fig. 11 shows the turn-on transient waveforms at 6.5 kV and 20 A load current. The solid line waveforms are experiment waveforms and dashed line waveforms are simulation waveforms with different models.

Fig. 12 (a) shows the comparison between experiment and conventional model simulation. The current rise speed is slower than that in experiment. The results can be explained with previous analysis as the transconductance increases at high drain-source voltage due to short channel effect and drain induced barrier lowering effect. Fig. 12(b) shows the comparison between experiment results and model results considering high voltage transconductance. The current rise stage waveform in the model could match with experiment results. But the voltage fall speed is faster than that in experiment. This can also be explained with previous analysis as the dynamic gate-drain charge when the MOSFET channel turn on is larger than the static gate-drain charge. Fig. 12(c) shows the comparison between experiment results and model results considering both high voltage transconductance and dynamic gate-drain charge. Both the current rise stage and voltage fall stage with improved model match the experiment result, which verifies the proposed model.

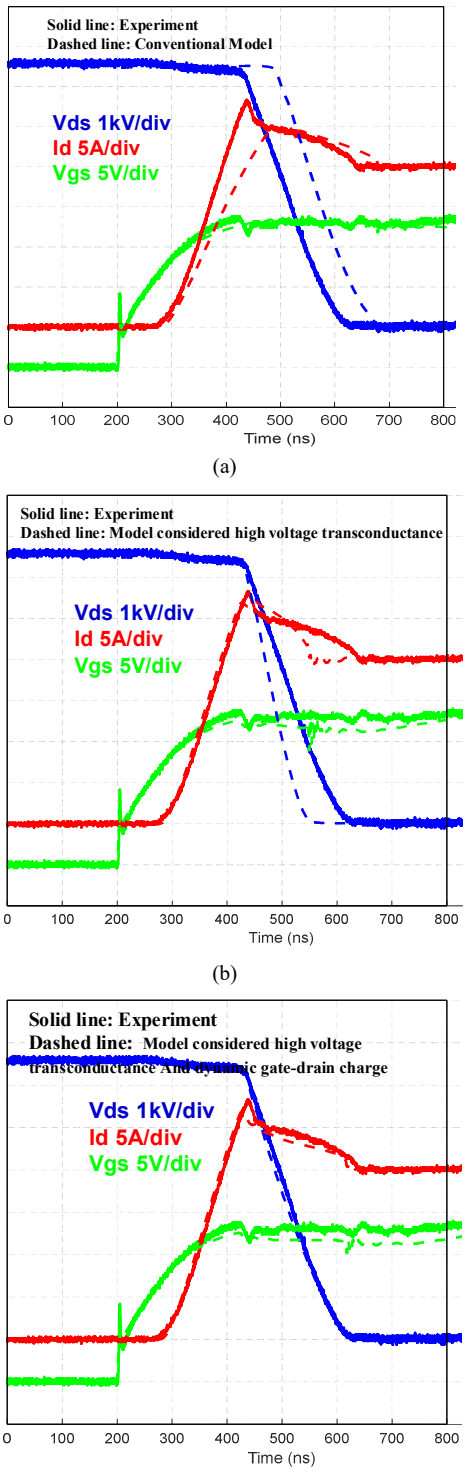
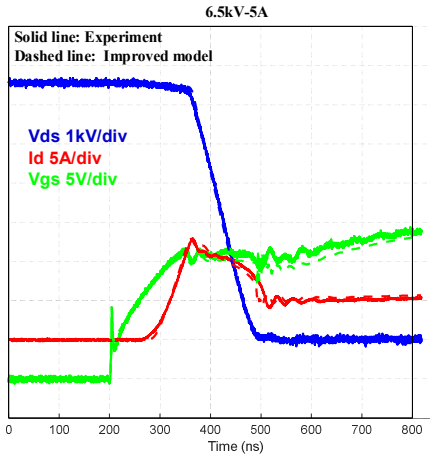
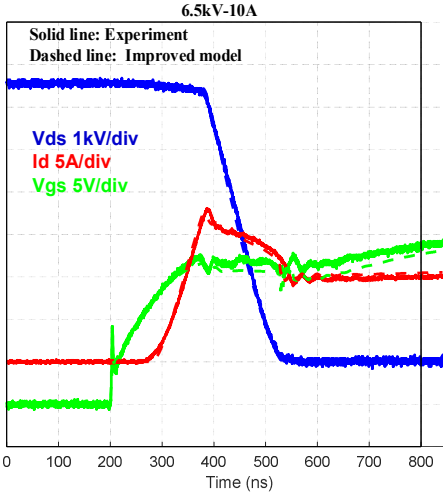


Fig. 12. Turn-on transient waveforms comparison at 6.5kV/20A. (a) conventional model, (b) model considering high voltage transconductance, (c) model considering both high voltage transconductance and dynamic gate-drain charge.

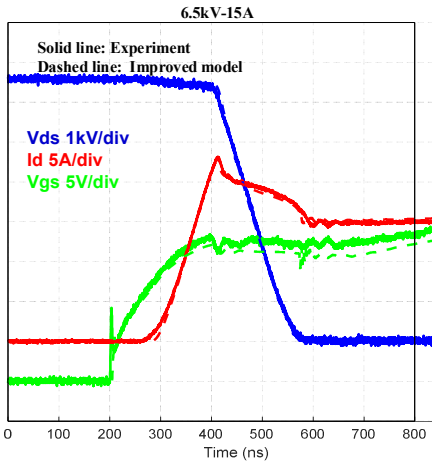
Fig. 13 shows the comparison between experiment and the improved model with different load. The improved model results match well with experimental results at different load conditions.



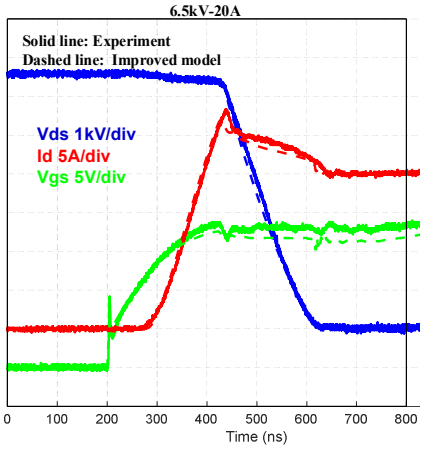
(a)



(b)



(c)



(d)

Fig. 13. Turn-on transient waveforms comparison between the experiments and the proposed improved model at 6.5 kV and different load conditions. (a) 5 A, (b) 10 A, (c) 15 A, (d) 20 A.

The turn-on switching energy of experimental results, conventional model, and the proposed improved model at different load conditions are summarized as shown in Table 3. The percentage errors between the two models with respect to the experimental results are also indicated.

Table 3. Turn-on switching energy comparison.

Eon (mJ)	5A	10A	15A	20A
Experiment	7.3	12.03	18.25	26.02
Proposed Model	7.23 (-0.96%)	11.85 (-1.5%)	17.87 (-2.08%)	25.46 (-2.15%)
Conventional Model	7.1 (-1.78%)	12.38 (+2.91%)	19.75 (+8.22%)	30.49 (+17.18%)

With the conventional model, the estimated switching loss for current rise stage is higher than that in experiment and the estimated switching loss for voltage fall stage is lower than that in experiment. In some conditions (such as light load in this experiment), the positive loss error during current rise stage cancels with negative loss error during voltage fall stage to some extent, and the total turn-on loss shows small error (<5%) compared to experimental results. In some conditions (such as heavy load in this experiment), the positive loss error during current rise stage dominates, and the total turn-on loss shows large error (>10%) compared to experimental results. The conventional model results do not have good consistency with experimental results over wide load conditions. The proposed improved model shows good consistency with experimental results. The predicted switching loss has <5% error during all the load conditions.

VI. Discussion

The device's self-heating impact is not considered in the tests illustrated in Section III and IV. For this 10 kV 20A SiC MOSFET, it is found that the transconductance is insensitive to junction temperature. In the curve tracer static tests, when the junction temperature increases from 25°C to 125°C, the device gate threshold voltage decreases from 4.2 V to 3 V,

while the saturation current transconductance factor nearly keeps unchanged and is around 0.7. Thus, for the high voltage transconductance test in section III, the self-heating impact on the saturation current transconductance factor value is not considered. The junction temperature rise is estimated with LTspice simulation based on the device transient thermal network provided by the vendor. For test conducted at 8 V gate voltage and 7 kV bus voltage as shown in Fig. 4, the estimated junction temperature rise is 19°C. The junction temperature will be higher at higher gate voltage condition. Thus, for other device that the transconductance is sensitive to junction temperature, the self-heating impact cannot be neglected and should be compensated when characterizing the high voltage transconductance. The SiC MOSFET parasitic capacitance is not sensitive to junction temperature. Thus, for the dynamic gate-drain charge test in section IV, the self-heating impact is also not considered.

The turn-off switching transient is not previously discussed in this paper. For this 10 kV 20 A SiC MOSFET, most of the MOSFET's current during turn-off switching transient flows through parasitic capacitors rather than the MOSFET channel. When the turn-off gate resistance varies, the turn-off switching energy is nearly constant and equals the energy stored in the parasitic capacitors of the MOSFET. The turn-off transient is dominated by the parasitic capacitors charging/discharging process and is not a strong function of gate voltage. The impact of high voltage transconductance discussed in the improved model is small during the turn-off transient. In addition, the turn-off loss only contributes a small portion of the total switching loss. Thus, only the turn-on transient is considered in the proposed improved model.

VII. Conclusion

This paper proposes an improved turn-on switching transient model of the 10 kV SiC MOSFET which considers the high voltage transconductance and dynamic gate-drain charge during the turn-on transient. Experiments with a 10 kV 20 A SiC MOSFET are conducted and verify the accuracy of the proposed improved model.

With the curve tracer test based conventional 10 kV SiC MOSFET model, the current rise speed is slower than that in the experiment as the high voltage transconductance is not considered while the voltage fall speed is faster than that in the experiment as the dynamic gate-drain charge is not considered. With the proposed improved model, both the current rise stage and voltage fall stage waveforms during the turn-on switching transient match well with that in the experiment. The loss error is within 5% over wide load conditions.

Acknowledgment

This work was primarily funded by U.S. DOE. The authors also thank GE, EPB, ORNL, Southern Company, Wolfspeed, and Powerex for their support of the project. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

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