Comprehensive Analysis and Improvement Methods of Noise Immunity of Desat Protection for High Voltage SiC MOSFETs With High DV/DT

XINGXUAN HUANG\textsuperscript{1}, SHIQI JI\textsuperscript{2} (Senior Member, IEEE), CHENG NIE\textsuperscript{3} (Member, IEEE), DINGRUI LI\textsuperscript{1}, MIN LIN\textsuperscript{1}, LEON M. TOLBERT\textsuperscript{1} (Fellow, IEEE), FRED WANG\textsuperscript{1,4} (Fellow, IEEE), AND WILLIAM GIEWONT\textsuperscript{5}

\textsuperscript{1}Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA
\textsuperscript{2}Department of Electrical Engineering, Tsinghua University, Beijing 100084, China
\textsuperscript{3}TBEA CO., Ltd., Xi’an 710000, China
\textsuperscript{4}Oak Ridge National Laboratory, Oak Ridge, TN 37830 USA
\textsuperscript{5}EPC Power, San Diego CA 92064 USA

CORRESPONDING AUTHOR: XINGXUAN HUANG (e-mail: xhuang36@vols.utk.edu)

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\textbf{ABSTRACT} This paper comprehensively analyzes desaturation (desat) protection for high voltage (>3.3 kV) silicon carbide (SiC) MOSFETs and especially how to build in noise immunity under high $dv/dt$. This study establishes a solid foundation for understanding the trade-offs between noise immunity and response speed of desat protection. Two implementations of the desat protection for high voltage SiC MOSFETs are examined, including desat protection based on discrete components and desat protection realized with a gate driver integrated circuit (IC). Both positive $dv/dt$ and negative $dv/dt$ are investigated. Analysis results show that the high $dv/dt$ with long duration caused by high voltage SiC MOSFETs’ switching results in strong noise interference in the desat protection circuitry. The impact of numerous influencing factors is investigated analytically, such as parasitic capacitances, parasitic inductance, damping resistance, and clamping impedance. Under high positive $dv/dt$, extremely small parasitic capacitances (<0.01 pF) between the drain terminal and protection circuitry could still compromise noise immunity of the desat protection circuitry that has a high-impedance voltage divider. Comprehensive design guidelines are summarized to boost the noise immunity, including circuit design, component selection, and PCB layout. The noise immunity margin under the positive $dv/dt$ is also derived quantitatively to guide the noise immunity improvement. The noise immunity analysis results and noise immunity improvement methods are validated with simulation and experimental results obtained from a phase leg based on 10 kV/20 A SiC MOSFETs.

\textbf{INDEX TERMS} SiC MOSFETs, high dv/dt, noise immunity, desat protection, gate driver design.

\section{I. INTRODUCTION}
The rapid development of SiC power semiconductor devices has led to the emergence of high voltage (>3.3 kV) SiC MOSFETs with superior device characteristics for power conversion applications. High voltage SiC MOSFETs feature high blocking voltage of up to 15 kV, low switching loss, and >10X higher switching frequency than Si IGBTs which are popular in medium voltage (MV) applications [1]–[6]. Therefore, high voltage SiC MOSFETs can play a critical part in the pursuit of next-generation MV converters with higher efficiency, smaller size and weight, higher control bandwidth, and more advanced control functions [7]–[12].

However, challenges should not be overlooked when applying high voltage SiC MOSFETs in MV converters.
Particularly, it is challenging to design the overcurrent/short circuit protection, which is an indispensable function in the gate driver for high voltage SiC MOSFETs. Compared to Si IGBTs, high voltage SiC MOSFETs have lower thermal capacitance, higher current density, and weaker short circuit withstand capability [13], [14]. Hence, faster protection response is desired. Meanwhile, high voltage SiC MOSFETs also generate high PWM voltage with high \( \frac{dv}{dt} \) [2]–[4], which makes the noise immunity issue more difficult to tackle when trying to hasten the protection response. Generally, high voltage SiC MOSFETs simultaneously require overcurrent/short circuit protection with fast response and strong noise immunity as well as simple implementation.

Several methods have been developed to protect high voltage SiC MOSFETs from overcurrent/short circuit conditions. A protection scheme based on an air-gapped current transformer has been adopted to protect discrete 10 kV SiC MOSFETs, which can clear the short circuit fault within 150 ns [15]. However, it is difficult to implement this scheme for high voltage SiC MOSFET modules with one or several half-bridge phase legs because the current transformer has to measure the current of the upper device via its drain terminal. As a result, the current transformer has to withstand high voltage between the primary side and secondary side whose potential is almost the same as the source terminal. Hence, it is complicated and costly to achieve the current transformer design with reliable insulation and high density, while still satisfying the clearance and creepage distance requirements. The protection scheme based on Rogowski coil current sensor also features fast response, but it requires complicated and expensive implementation to realize sufficient sensor accuracy and noise immunity when protecting SiC MOSFETs with fast transients from conducted or radiated EMI noise [16]–[19]. Complicated Rogowski coil design with a shield is required to achieve high accuracy and noise immunity under high \( \frac{dv}{dt} \).

The active integrator in the protection circuitry should be reset periodically to overcome the difficulty of Rogowski coil in measuring the dc current. Desaturation (desat) protection schemes have been widely adopted to protect various SiC MOSFETs because of their simple implementation for both discrete devices and modules and their effectiveness under various short circuit conditions [20]–[25].

In terms of noise immunity of the desat protection, however, response time has been often sacrificed to improve noise immunity and avoid false triggering under high \( \frac{dv}{dt} \), such as adopting a large blanking capacitance [20], [24]. As a result, the relatively long response time makes desat protection less competitive in some cases, such as high voltage SiC MOSFET modules with high current rating and hence high saturation current [19]. Also, the threshold current of desat protection is significantly higher at lower junction temperature because the on-resistance of high voltage SiC MOSFETs increases rapidly (to 2X–3X) from 25 °C to 125 °C [4], [16]. Thus, faster response of desat protection while maintaining strong noise immunity is desirable in order to limit short circuit current and loss when a fault occurs at lower junction temperature.

To achieve better trade-off between strong noise immunity and fast response, noise immunity of the desat protection circuitry for high voltage SiC MOSFETs should be analyzed thoroughly. Noise immunity of the desat protection has been studied partially under the high positive \( \frac{dv}{dt} \), with several methods proposed to avoid spurious triggering [22]. Nevertheless, there is no quantitative analysis about noise immunity, and several important impact factors have not been included in the analysis, such as parasitic inductance, clamping impedance, and voltage divider impedance. In summary, the desat protection circuitry for high voltage SiC MOSFETs is still not well understood in terms of noise immunity, which is still needed in order to shorten the protection response time while maintaining strong noise immunity.

This paper conducts a comprehensive and quantitative analysis of noise immunity for desat protection for high voltage SiC MOSFETs with high \( \frac{dv}{dt} \). This paper focuses on noise immunity in the detection process of desat protection for high voltage SiC MOSFETs. The noise immunity in other processes of desat protection is out of the scope of this paper. This paper is an extension of the work in [26]. The additional contribution includes the study of the desat protection realized by a gate driver IC as well as a comprehensive noise immunity analysis and possible improvements under negative \( \frac{dv}{dt} \). In this paper, comprehensive noise immunity analysis is provided in Section II, under both positive and negative \( \frac{dv}{dt} \). Based on noise immunity analysis results, Section III provides detailed noise immunity improvement guidelines supported by simulation and experimental results, and Section IV concludes the paper.

II. NOISE IMMUNITY ANALYSIS

Desat protection for high voltage SiC MOSFETs can be implemented with circuitry composed of discrete components or a gate driver IC with integrated desat protection function, as illustrated in Fig. 1. In this paper, noise immunity of both implementations will be analyzed in detail.

High current through the MOSFET is detected by desat protection by monitoring its drain-to-source voltage \( V_{ds} \). The protection threshold voltage \( V_{\text{desat,th}} \) is selected based on the I-V characteristic of the MOSFET and the desired protection threshold current. When the MOSFET is in conduction mode, \( V_{\text{desat}} \) in desat protection circuitry in Fig. 1 can track \( V_{ds} \) of the MOSFET. Once \( V_{\text{desat}} \) is higher than \( V_{\text{desat,th}} \), the protection will be triggered. During the turn-on transient, a blanking time is designed to effectively avoid false triggering of desat protection. The length of the blanking time can be tuned by changing \( C_{\text{blk}} \). The typical value of \( C_{\text{blk}} \) is lower than 200 pF.

When the MOSFET is turned off, the desat diode \( D_{\text{desat}} \) should withstand the high \( V_{ds} \) to protect the desat protection circuitry. \( D_{\text{desat}} \) should have the same or higher voltage rating than the high voltage SiC MOSFET. In the desat protection for high voltage SiC MOSFETs, the desat diode \( D_{\text{desat}} \) is usually implemented with one SiC Schottky diode or several SiC Schottky diodes in series. As shown in Fig. 2 and Fig. 3, the parasitic capacitance of the desat diode, \( C_{\text{desat}} \), is critical
in noise immunity analysis under high \(dv/dt\). Typically, the equivalent \(C_{\text{desat}}\) after linearization varies from 1 pF to 10 pF. The typical value of the parasitic inductance \(L_{\text{desat}}\) does not exceed 500 nH.

The gate driver IC with desat protection function (STGAP1AS from STMicroelectronic or others) enables more compact layout, as shown in Fig. 1(b), yet leads to too low of a threshold current for some high voltage SiC MOSFETs due to its low protection threshold voltage \((V_{\text{desat,th}} < 10 \text{ V})\) for desat protection [20], [23], [27].

With a voltage divider and a discrete comparator, the desat protection based on discrete components in Fig. 1(a) has more flexibility to achieve a desired response time and threshold current for various high voltage SiC MOSFETs [13], [21]. \(V_{cc}\) in Fig. 1(a) should be significantly higher than the selected protection threshold voltage \(V_{\text{desat,th}}\) to ensure that \(C_{\text{desat}}\) can track \(V_{ds}\) quickly when \(V_{ds}\) of the MOSFET reaches \(V_{\text{desat,th}}\).

If the on-state gate voltage \(V_{gs,\text{on}}\) of the MOSFET can satisfy this requirement, the output voltage of the gate driver IC is usually adopted as \(V_{cc}\). Otherwise, a different power supply is designed to output a constant voltage for \(V_{cc}\) for the protection circuitry. Once \(V_{cc}\) is selected, \(R_{\text{blk}}\) and \(C_{\text{blk}}\) are selected to realize the blanking time whose length is determined by the turn-on characteristic of the MOSFET. Also, to limit the power loss of \(R_{\text{blk}}\), \(V_{cc}\) should not be too large, and \(R_{\text{blk}}\) should not be too small.

The noise interference and spurious triggering of desat protection are mainly caused by high \(dv/dt\) generated by high voltage SiC MOSFETs. High \(dv/dt\) can disturb the operation of the desat protection circuitry via the parasitic capacitance \(C_{\text{desat}}\) of the desat diode \(D_{\text{desat}}\), including both implementations in Fig. 1. Fig. 2 and Fig. 3 illustrate the influence of high \(dv/dt\) and the resulting displacement current on the desat protection circuitry based on discrete components. In addition to \(C_{\text{desat}}\), the parasitic inductance \(L_{\text{desat}}\) should also be considered. A well-known mechanism of spurious triggering is caused by interference from high \(dv/dt\) that results in the blanking capacitor voltage \(V_{\text{desat}}\) or the comparator input voltage \(V_{\text{comp}}\) rising substantially and then exceeding the comparator threshold voltage \(V_{th}\) [13], [22].

Positive \(dv/dt\) results in a positive spike in \(V_{\text{desat}}\) and hence heavily impacts the noise immunity of the desat protection circuitry. Traditionally, \(R_{\text{damp}}\) is added to damp the oscillation. In the protection circuitry composed of discrete components, \(R_{\text{cla}}\) and a transistor \(M_{\text{cla}}\) are installed to clamp \(V_{\text{desat}}\) [22]. As illustrated in Fig. 2, \(R_{\text{cla}}\) and \(M_{\text{cla}}\) are introduced with the purpose of absorbing the displacement current of \(C_{\text{desat}}\) due to the high positive \(dv/dt\). \(R_{\text{cla}}\) and \(M_{\text{cla}}\) are indispensable if \(V_{cc}\) is a constant voltage level, instead of the output voltage of the gate driver IC. This is often the case when designing desat protection for high voltage SiC MOSFETs which requires relatively high \(V_{\text{desat,th}}\). If \(V_{cc}\) is provided by the output voltage of the gate driver IC, the displacement current can be absorbed by \(V_{cc}\), since \(V_{cc}\) will be the off-state gate voltage \(V_{gs,\text{off}}\) (usually between 0 V and −6 V) when high positive \(dv/dt\) is generated. In this case, \(M_{\text{cla}}\) and \(R_{\text{cla}}\) are not necessary. As for the desat protection circuitry realized by the gate driver IC, the discharge switch \(S_{\text{ds}}\) can absorb the displacement current from \(C_{\text{desat}}\). Still, there will be positive...
spikes and oscillations in \( V_{\text{desat}} \) due to high positive \( dv_{ds}/dt \), which will be studied in this paper.

The interference caused by the negative \( dv_{ds}/dt \) during the turn-on process of high voltage SiC MOSFETs, in most cases, will not falsely trigger the comparator. Instead, \( V_{\text{desat}} \) and \( V_{\text{comp}} \) could experience a voltage dip if the displacement current of \( C_{\text{desat}} \) is much higher than the current from \( V_{cc} \) or \( I_{cc} \). As shown in Fig. 3, \( C_{\text{blk}} \) will be discharged to contribute to the displacement current of \( C_{\text{desat}} \), and \( V_{\text{desat}} \) and \( V_{\text{comp}} \) will decline during the voltage fall time of \( V_{ds} \). In this case, the voltage dip in \( V_{\text{desat}} \) or \( V_{\text{comp}} \) could falsely trigger some comparators and hence the desat protection, due to the mechanism named phase reversal or phase inversion because the comparator input voltage is lower than the allowed minimum input voltage [28]–[30]. To alleviate the impact of the negative \( dv/dt \), the clamping diode \( D_{\text{blk}} \) (as shown in Fig. 1) is often added in the traditional design. However, the comparator could still be falsely triggered if the forward voltage drop of \( D_{\text{blk}} \) is not sufficiently small. Moreover, it is likely that \( V_{\text{comp}} \) has a significant voltage drop which falsely triggers the comparator and hence the protection in Fig. 1(a), since \( V_{\text{comp}} \) is not clamped by a diode.

In this paper, the desat protection circuitry designed for the 10 kV/20 A SiC MOSFET from Wolfspeed is studied as an example [21]. Parameters of the desat protection circuitry are shown in Fig. 1(a), and the circuit model is established in PLECS. Although the study example is a desat protection circuitry implemented with discrete components, the study results will also benefit noise immunity analysis of the desat protection realized by the gate driver IC. Thus, noise immunity of the desat protection realized by the gate driver IC will also be examined in detail in this section.

In the desat protection circuitry studied in this paper, the desat diode is implemented with three 3.3 kV SiC Schottky diodes in series (GAP3SLT33-220FP from GeneSiC) [31]. Such implementation can achieve 10 kV voltage rating and reduce the parasitic capacitance effectively. Consequently, the desat diode can be modeled with an ideal diode in parallel with the parasitic capacitance \( C_{\text{desat}} \), as shown in Fig. 1(a). Parasitic capacitance of the desat diode \( C_{\text{desat}} \) is nonlinear and decreases rapidly as \( V_{ds} \) increases. Meanwhile, the resulting displacement current does not change significantly since \( dv_{ds}/dt \) is low when the parasitic capacitance of the desat diode is large. The nonlinear \( C_{\text{desat}} \) is hence modeled with its charge-equivalent linear capacitance (2.3 pF) [31], [32].

**A. ANALYSIS OF BLANKING CAPACITOR VOLTAGE \( V_{\text{desat}} \)**

In this subsection, \( V_{\text{desat}} \) under the negative \( dv/dt \) will not be discussed in detail. The worst voltage dip of \( V_{\text{desat}} \) under negative \( dv/dt \) happens when \( D_{\text{blk}} \) enters the conduction mode. In such case, the voltage dip is simply determined by the forward voltage drop of \( D_{\text{blk}} \), \( V_{\text{diode}} \). The maximum positive spike in \( V_{\text{desat}} \) under negative \( dv/dt \) cannot be higher than that under positive \( dv/dt \). Thus, this subsection focuses on how positive \( dv/dt \) shapes \( V_{\text{desat}} \). The analysis of \( V_{\text{desat}} \) will benefit the noise immunity analysis of the two hardware implementations shown in Fig. 1.

Under a constant \( dv/dt \) of \(+100 \text{ V/ns}\) as \( V_{ds} \) rises from 0 to 7 kV, simulation waveforms of \( V_{\text{desat}} \) are displayed in Fig. 4. Because of \( M_{\text{cla}} \) and \( R_{\text{cla}} \) \((R_{\text{cla}} << R_{\text{blk}})\), \( V_{\text{desat}} \) is clamped to \( V_{\text{clamp}} \) \((-5 \text{ V})\) before \( V_{ds} \) starts to rise at \( t = 20 \text{ ns}\). This is a reasonable assumption because \( V_{\text{desat}} \) should be clamped at \( V_{\text{clamp}} \) before high positive \( dv/dt \) is generated, no matter whether the high voltage SiC MOSFET is the active switch or the synchronous switch. During the 70 ns voltage rise time \( t_{\text{rise}} \), \( V_{\text{desat}} \) reaches steady state after the oscillation is damped. At steady state, the spike of \( V_{\text{desat}} \) is proportional to \( R_{\text{cla}}, C_{\text{desat}}, \) and \( dv_{ds}/dt \), all of which heavily influence noise immunity.

The peak value of \( V_{\text{desat}} \) during the voltage rise time of \( V_{ds} \) is determined by the oscillations at the early stage of voltage rise time. According to simulation waveforms in Fig. 4, higher \( L_{\text{desat}} \) leads to higher peak value of \( V_{\text{desat}} \). If \( C_{\text{blk}} \) is decreased from 56 pF to 20 pF, the oscillations caused by high positive \( dv_{ds}/dt \) will result in higher peak in \( V_{\text{desat}} \). A larger \( R_{\text{damp}} \) is effective in suppressing the oscillations and positive spike in \( V_{\text{desat}} \), especially when the circuit has a large \( L_{\text{desat}} \) and/or a small \( C_{\text{blk}} \).

High frequency oscillation of \( V_{\text{desat}} \) at the beginning of \( t_{\text{rise}} \) can be analyzed via circuit analysis in the frequency domain.
The simplified circuit model used to analyze $V_{\text{desat}}$ is drawn in Fig. 5. Because $M_{\text{cla}}$ is fully on with low impedance before high $dv/dt$ is generated, $R_{\text{blk}}$ and the voltage divider formed by $R_{\text{d1}}$ and $R_{\text{d2}}$ with high impedance can be neglected. The difference between $V_{\text{clamp}}$ (−5 V) and 0 V (defined as potential of the source of the 10 kV SiC MOSFET) is also neglected to simplify the analysis.

The relationship between $V_{ds}$ and $V_{\text{desat}}$ in frequency domain can be expressed as:

$$\frac{V_{\text{desat}}(s)}{V_{ds}(s)} = \frac{sC_{\text{desat}}R_{\text{cla}}}{s^2LC_{\text{desat}}R_{\text{cla}}C_{\text{blk}} + s^2T_{d2} + sT_{d1} + 1}$$  \(1\)

$$T_{d2} = LC_{\text{desat}} + R_{\text{damp}}C_{\text{desat}}R_{\text{cla}}C_{\text{blk}}$$  \(2\)

$$T_{d1} = C_{\text{desat}}R_{\text{cla}} + C_{\text{blk}}R_{\text{cla}} + C_{\text{desat}}R_{\text{damp}}$$  \(3\)

Based on the Bode plot of $V_{\text{desat}}(s)/V_{ds}(s)$ in Fig. 6, the peak magnitude is reached at the resonance frequency $\omega_r$ ($\omega_r = \frac{1}{\sqrt{LC_{\text{damp}}}}$). $\omega_r$ is also the oscillation frequency of $V_{\text{desat}}$ in simulation waveforms in Fig. 4. With 300 nH $L_{\text{desat}}$, the peak of the Bode plot in Fig. 6 occurs at the resonance frequency $\omega_r$ of 192 MHz, which coincides well with the oscillation frequency of $V_{\text{desat}}$ in time-domain simulation waveform in Fig. 4. Because $V_{ds}$ has high $dv/dt$, it is rich with high frequency components, and those components can excite an oscillation at the resonance frequency. The peak magnitude of $V_{\text{desat}}(s)/V_{ds}(s)$, $V_{d, pk}$, can be expressed as follows.

$$V_{d, pk} = \frac{R_{\text{cla}}}{\sqrt{(R_{\text{cla}} + R_{\text{damp}})^2 + \left(\frac{C_{\text{desat}}R_{\text{damp}}C_{\text{cla}}}{L_{\text{desat}}C_{\text{damp}}}ight)}}$$  \(4\)

$V_{d, pk}$ is an important indicator of the peak value of $V_{\text{desat}}$ during the voltage rise time. Higher $L_{\text{desat}}$ results in slightly higher $V_{d, pk}$ and thus higher spike in $V_{\text{desat}}$ caused by the oscillations. Based on Fig. 6, the resonance frequency $\omega_r$ becomes lower as $L_{\text{desat}}$ increases. According to Fourier analysis of $V_{ds}$, the magnitude of $V_{ds}(\omega_r)$ increases as $\omega_r$ becomes lower and lower. This is another reason why a higher $L_{\text{desat}}$ makes $V_{\text{desat}}$ oscillate with higher peak value.

The effect of $R_{\text{damp}}$ on the peak value of $V_{\text{desat}}$ can also be explained by the analysis of the peak magnitude of $V_{\text{desat}}(s)/V_{ds}(s)$. As indicated in Fig. 7, $V_{d, pk}$ declines substantially with a higher $R_{\text{damp}}$ selected. If $R_{\text{damp}}$ is 0 Ω, $V_{d, pk}$ will reach the maximum value of 0 dB. A low $R_{\text{cla}}$ effectively shields $V_{\text{desat}}$ from the influence of high positive $dv/dt$, which reduces both $V_{d, pk}$ and the steady state level of $V_{\text{desat}}$ during the voltage rise time. According to (4), increasing $C_{\text{blk}}$ also reduces $V_{d, pk}$ and the high frequency oscillations in $V_{\text{desat}}$, which is demonstrated in simulation waveforms in Fig. 4.

The analysis of $V_{\text{desat}}$ in this subsection is also applicable for the desat protection realized with a gate driver IC in Fig. 1(b), in which $V_{\text{desat}}$ determines the comparator output. In this case, $V_{\text{desat}}$ can also be analyzed with the circuit model in Fig. 5, since the current source $I_{\text{cla}}$ can be neglected due to its high impedance. $R_{\text{cla}}$ is mainly dominated by the on-state resistance of the discharge switch $S_{\text{dis}}$, which is turned on as the high voltage SiC MOSFET is in OFF state. As a result, $R_{\text{cla}}$ is only determined by the gate driver IC.

**B. ANALYSIS OF COMPARATOR INPUT VOLTAGE $V_{\text{comp}}$**

1) **ANALYSIS OF $V_{\text{comp}}$ UNDER POSITIVE $dv/dt$**

In the desat protection based on discrete components, $V_{\text{comp}}$ plays a more critical role in noise immunity than $V_{\text{desat}}$. According to Fig. 4, there are no high frequency oscillations in $V_{\text{comp}}$, because the voltage divider and $C_d$ caused by the comparator and PCB layout form an effective low pass filter.
However, extremely small parasitic capacitances between the drain terminal and PCB traces or polygons of the protection circuitry should be considered. As drawn in Fig. 8, these parasitic capacitances (<0.1 pF) are critical due to the high positive \( \frac{dv}{dt} \) with considerable voltage rise time \( t_{\text{rise}} \) generated by high voltage SiC MOSFETs. \( C_{p1} \) and \( C_{p2} \) effectively increase the value of \( C_{\text{desat}} \). Particularly, \( C_{p3} \) coupled with the voltage divider results in a substantial positive spike in \( V_{\text{comp}} \).

To simplify the study, it is assumed that that \( V_{ds} \) rises with a constant \( \frac{dv}{dt} \). The displacement current of \( C_{p3} \) can hence be modeled by a constant dc current source \( I_{p3} \). During the voltage rise time \( t_{\text{rise}} \), \( V_{\text{desat}} \) can be modeled as a constant dc voltage source after neglecting the voltage divider, \( R_{\text{blk}} \) and high frequency oscillations in \( V_{\text{desat}} \). Before high positive \( \frac{dv}{dt} \) occurs, \( V_{\text{comp}} \) is already clamped to \( V_{\text{clamp}} \). With superposition theorem, \( V_{\text{comp}} \) in \( s \) domain can be calculated as:

\[
V_{\text{comp}}(s) = V_{\text{desat}} \frac{R_{d2}}{sC_d R_d 1 R_{d2} + R_{d2} + R_{d1}} + I_{p3} \frac{R_{d1} R_{d2}}{sC_d R_d 1 R_{d2} + R_{d1} + R_{d2}} \tag{5}
\]

In the equations in this paper, the reference point of \( V_{\text{desat}} \) and \( V_{\text{comp}} \) is \( V_{\text{clamp}} \) (−5 V), unless their reference point is otherwise explicitly noted.

From the perspective of noise immunity, the focus is the peak voltage spike \( V_{\text{spike}} \) of \( V_{\text{comp}} \), the maximum value of \( V_{\text{comp}}(t) \) at the end of the voltage rise time \( t_{\text{rise}} \), which is derived as follows. The reference point of \( V_{\text{spike}} \) is also \( V_{\text{clamp}} \).

\[
V_{\text{spike}} = V_{\text{comp}}(t_{\text{rise}}) = \left( R_{d1} C_{p3} + T \right) \frac{R_{d2}}{R_{d1} + R_{d2}} \frac{dv}{dt} \times \left( 1 - e^{-\frac{t_{\text{rise}}}{R_{d1} C_{\text{desat}}}} \right) \tag{6}
\]

\[
T = R_{\text{cla}} \left( C_{\text{desat}} + C_{p1} + C_{p2} \right) \tag{7}
\]

High \( \frac{dv}{dt} \) with long voltage rise time generated by high voltage SiC MOSFETs can make the desat protection circuitry vulnerable to noise and spurious triggering. Simulation results in Fig. 9 reveal that 0.004 pF \( C_{p3} \) induces a sufficiently high positive spike in \( V_{\text{comp}} \) to falsely trigger the desat protection for 10 kV SiC MOSFETs shown in Fig. 1(a), which is 60% higher than that in 1.7 kV SiC MOSFETs with the same \( \frac{dv}{dt} \) (+100 V/\( ns \)) and much shorter \( t_{\text{rise}} \). In the simulation, \( C_{p1} \), \( C_{p2} \), and \( C_{p3} \) are 0 pF, 0 pF, and 0.004 pF, respectively, and \( C_{\text{desat}} \) is still modeled with a 2.3 pF capacitor.

With the established model of \( V_{\text{spike}} \), the impact of the voltage rise time \( t_{\text{rise}} \) can be analyzed quantitatively, as plotted in Fig. 9(b). Longer \( t_{\text{rise}} \) results in a higher spike in the comparator input voltage \( V_{\text{comp}} \), making the protection more susceptible to spurious triggering. As \( t_{\text{rise}} \) becomes longer, \( V_{\text{spike}} \) continues to increase but more slowly and eventually saturates. The maximum value of \( V_{\text{spike}} \) can be expressed as:

\[
V_{\text{spike, max}} = \left( R_{d1} C_{p3} + T \right) \frac{R_{d2}}{R_{d1} + R_{d2}} \frac{dv}{dt} \tag{8}
\]

Fig. 9 also illustrates that the measured \( V_{\text{spike}} \) in simulation waveforms coincides well with the calculation result based on (6). However, if \( t_{\text{rise}} \) is not considerably longer than the time constant \( R_{\text{cla}} C_{\text{blk}} \), \( V_{\text{spike}} \) cannot be modeled by a constant dc voltage source, and the expression of \( V_{\text{spike}} \) is modified as follows.

\[
V_{\text{spike}} = \left[ R_{d1} C_{p3} + T \left( 1 - e^{-\frac{t_{\text{rise}}}{R_{d1} C_{\text{desat}}}} \right) \right] \frac{R_{d2}}{R_{d1} + R_{d2}} \frac{dv}{dt} \times \left( 1 - e^{-\frac{t_{\text{rise}}}{R_{d1} C_{\text{desat}}}} \right) \tag{9}
\]
Based on (9), the magnitude of V_{spike} as a function of voltage rise time and \(dv/dt\) is evaluated in Fig. 10, in which \(C_{p1}, C_{p2}, C_{p3}\), and \(C_d\) are still 0 pF, 0 pF, 0.004 pF, and 1 pF, respectively. In terms of generating high V_{spike} in the desat protection circuitry based on discrete components, the worst case occurs when high \(dv/dt\) and long voltage rise time appear simultaneously. Thus, the desat protection of high voltage (>3.3 kV) SiC MOSFETs with high \(dv/dt\) and longer duration is more vulnerable to noise generated by \(dv/dt\), compared to other power semiconductor devices such as lower voltage SiC MOSFETs (1.2 & 1.7 kV) or 3.3 kV, 4.5 kV, and 6.5 kV Si IGBTs which are currently dominant in MV applications, as shown in Fig. 10.

### 2) ANALYSIS OF V_{COMP} UNDER NEGATIVE DV/DT

When negative \(dv/dt\) is generated, \(V_{comp}\) will also be shaped heavily by the displacement currents from parasitic capacitances, especially \(C_{desat}\) and \(C_p3\). Different from the case with positive \(dv/dt\), \(V_{comp}\) is not necessarily clamped to \(V_{clamp}\) before negative \(dv/dt\) is generated, leading to different initial conditions. Yet, \(V_{comp}\) can still be analyzed with the analytical method used to study \(V_{comp}\) under high positive \(dv/dt\).

To analyze \(V_{comp}\), \(V_{desat}\) under negative \(dv/dt\) should be examined first to eliminate the nonlinearity caused by \(D_{blk}\). The influence of \(C_{p3}\) on \(V_{desat}\) can be neglected, because \(C_{p3}\) is much smaller than \(C_{desat}\). If zero voltage switching (ZVS) can be achieved with the high voltage SiC MOSFET, \(M_{cla}\) is already fully ON to clamp \(V_{comp}\) at \(V_{clamp}\) before negative \(dv/dt\) occurs, and \(M_{cla}\) always has low impedance during the voltage fall time \(t_{fall}\). In this case, \(V_{desat}(t = +\infty)\), the final value of \(V_{desat}\) at the end of voltage fall time, is derived as follows, assuming \(t_{fall}\) is infinitely long.

\[
V_{desat}(t = +\infty) = \frac{(V_{cc} - V_{clamp})R_{cla}}{R_{cla} + R_{blk}} + (C_{desat} + C_{p1} + C_{p2})\frac{dv}{dt}R_{cla} \tag{10}
\]

If the high voltage SiC MOSFET switches without any soft switching, \(M_{cla}\) will have high impedance during the entire voltage fall time, and \(V_{desat}(t = +\infty)\) can be calculated as below.

\[
V_{desat}(t = +\infty) = V_{cc} - V_{clamp} + (C_{desat} + C_{p1} + C_{p2})\frac{dv}{dt}R_{blk} \tag{11}
\]

In either case, \(V_{desat}\) will decline quickly and be clamped by the diode \(D_{blk}\) after the negative \(dv/dt\) is generated if \(V_{desat}(t = +\infty)\) is much lower than zero due to the sufficiently high displacement current. In both cases, with the requirement in (12) satisfied, \(V_{desat}\) can be modeled as a constant dc voltage source, \(V_{diode}\), during the voltage fall time.

\[
-(C_{desat} + C_{p1} + C_{p2})\frac{dv}{dt} > V_{cc} - V_{clamp} \tag{12}
\]

where \(\frac{dv}{dt}\) in the equation is negative. The minimum negative spike in \(V_{comp}\) at the end of the voltage fall time, \(V_{spike,n}\), can be calculated with the following equations.

\[
V_{spike,n} = V_{n,max} + (V_{ini} - V_{n,max}) e^{-t_{fall}/\tau}\tag{13}
\]

\[
V_{n,max} = \frac{R_{d2}}{R_{d1} + R_{d2}} R_{d1} C_{p3} \frac{dv}{dt} - V_{diode}\tag{14}
\]

\(V_{ini}\) is the initial value of \(V_{comp}\) when the voltage fall time starts. The reference point of \(V_{spike,n}\) and \(V_{ini}\) is also \(V_{clamp}\). In the cases where ZVS can be achieved, \(V_{ini}\) is 0 V. In the hard switching cases, \(V_{ini}\) is usually slightly higher than 0 V. With analysis based on parameters in Fig. 1(a) and 0 V \(V_{ini}\), as shown in Fig. 11, the negative voltage spike becomes more substantial as the voltage fall time increases. As can be seen in (13) and (14), \(C_{p3}\) together with high negative \(dv/dt\) contributes to a large portion of the negative spike in \(V_{comp}\), which makes \(V_{comp}\) much lower than the ground potential of the comparator during the voltage fall time. The duration of the negative spike increases as the voltage fall time becomes longer. The analytical results of \(V_{spike,n}\) in Fig. 11 match well with the simulation results in Fig. 12. Simulation results also show that adding \(D_{blk}\) is not effective in reducing the negative spike in \(V_{comp}\) caused by the displacement current from \(C_{p3}\). In general, higher negative \(dv/dt\) together with longer duration...
of $dv/dt$ generates stronger interference on the comparator input voltage.

Therefore, high negative $dv/dt$ with long duration generated by high voltage SiC MOSFETs leads to long negative transient input voltage in the desat comparator and poses a substantial challenge to the comparator’s ability to withstand negative input voltage. To avoid false triggering due to the negative $dv/dt$, the phase reversal issue of the desat comparator must be tackled and is covered in the next section.

### III. NOISE IMMUNITY IMPROVEMENT

Positive $dv_{ds}/dt$ can falsely trigger desat protection by generating positive voltage spikes in $V_{desat}$ and $V_{comp}$. On the other hand, negative $dv_{ds}/dt$ can falsely trigger the comparator and desat protection by the phase reversal mechanism. Based on the two mechanisms of false triggering, this section discusses how to improve the noise immunity of the desat protection for high voltage SiC MOSFETs.

#### A. DESAT PROTECTION REALIZED WITH GATE DRIVER IC

To improve noise immunity under negative $dv_{ds}/dt$, a Schottky diode with low forward voltage drop should be selected for $D_{blk}$. The gate driver IC should be selected accordingly to ensure it can withstand $V_{desat}$ without any phase reversal issue when $D_{blk}$ is in conduction mode.

The analysis of $V_{desat}$ in Section II lays a solid foundation for noise immunity improvement under the positive $dv_{ds}/dt$. The peak positive spike in $V_{desat}$ should be reduced during the voltage rise time. The design guidelines for better noise immunity are summarized in Table 1. The design guidelines in Table 1 have little influence on the protection response speed. Among the guidelines in Table 1, the top priority is to implement the desat diode with lower parasitic capacitance to suppress the displacement current. Then, the oscillations in $V_{desat}$ can be alleviated by reducing $L_{desat}$ and adding $R_{damp}$. $L_{desat}$ can be reduced by using wide PCB traces or other low-inductance connectors to connect the desat diode with the drain terminal and the protection circuitry. It should be noted that it is not recommended to adopt low-inductance connectors which can reduce $L_{desat}$ but also increase the equivalent $C_{desat}$ significantly. If $L_{desat}$ cannot be further decreased, $R_{damp}$ can be increased to suppress the oscillations and the peak in $V_{desat}$, based on the comprehensive analysis in Section II.

After reducing $C_{desat}$ and $L_{desat}$ and adding $R_{damp}$, strong noise immunity should be achieved in most cases, unless the selected gate driver IC leads to a large $R_{cl}$, and selecting a gate driver IC with low $R_{cl}$ is highly recommended. A Schottky diode with low forward voltage drop should be selected comparator can prevent phase reversal, and selecting a gate driver IC based on the manufacturer’s datasheet. Although increasing $C_{blk}$ is also effective in reducing the peak of $V_{desat}$ during the voltage rise time, it is not recommended to use a large $C_{blk}$ to suppress oscillation in $V_{desat}$ because that will lead to a long response time.

#### B. DESAT PROTECTION BASED ON DISCRETE COMPONENTS

1) THEORETICAL ANALYSIS

In the desat protection circuitry based on discrete components, we also readily improve noise immunity under the influence of negative $dv/dt$. One essential guideline is to select comparators without the phase reversal issue to avoid false triggering due to the negative spike in $V_{comp}$, which is also the simplest solution to this issue. Phase reversal is not an uncommon issue in comparators with traditional PNP-transistor input stage [30]. Nowadays, it is not difficult to find numerous low-cost comparators with a CMOS input stage which are designed to prevent phase reversal. In case it is uncertain whether the selected comparator can prevent phase reversal, a Schottky diode can also be installed to suppress a negative voltage spike in $V_{comp}$. On the other hand, op-amps and comparators with phase reversal issue should not be used in SiC-based MV converters with high $dv/dt$.

In terms of noise immunity improvement under positive $dv/dt$, the noise immunity margin $V_{margin}$ in $V_{comp}$ can be quantitatively calculated as follows.

$$V_{margin} = V_{th} - V_{clamp} - V_{spike} \quad (15)$$

$V_{th}$ is the threshold voltage of the comparator. $V_{th}, V_{clamp}$ is closely coupled with the threshold voltage of desat protection $V_{desat,th}$ and the voltage divider design. The reference point of $V_{th}$ and $V_{desat,th}$ is 0 V. The quantitative analysis is as follows.

$$V_{th} - V_{clamp} = (V_{desat,th} - V_{clamp}) \frac{R_{d2}}{R_{d1} + R_{d2}} \quad (16)$$

$V_{spike}$ can be calculated with (6), since high voltage SiC MOSFETs usually have long $t_{rise}$. Then, the expression of

![FIGURE 11. Simulation results of $V_{desat}$ and $V_{comp}$ with 0.004 pF $C_{ps}$ and 1 pF $C_{d}$.](image-url)
TABLE 2 Summary of Selection and Design Guidelines for the Comparator for Noise Immunity Improvement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Selection or design guideline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>Higher power supply voltage is preferred</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>Wider input voltage range is preferred</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>Slightly longer propagation delay is preferred; Trade-off: longer delay leads to desat protection with slower response</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>Higher threshold voltage is preferred; Filter capacitor added to stabilize threshold voltage</td>
</tr>
<tr>
<td>Phase reversal</td>
<td>Comparators without phase reversal issue should be selected; If not sure about phase reversal issue, a Schottky diode can be added to clamp V_{comp}</td>
</tr>
<tr>
<td>Pull-up resistance (only for comparators with open drain output)</td>
<td>Pull-up resistance should be small for better noise immunity</td>
</tr>
</tbody>
</table>

\[
V_{\text{margin}} = \frac{R_{d2}}{R_{d1} + R_{d2}} \left[ V_{\text{desat,th}} - V_{\text{clamp}} - T_r \frac{dv}{dt} \right] \\
\times \left[ 1 - e^{-\frac{t_{\text{rise}}}{C_{d}(R_{d1} + R_{d2})}} \right]  \quad (17)
\]

\[
T_r = R_{d1}C_{p3} + R_{\text{cla}}(C_{\text{desat}} + C_{p1} + C_{p2})  \quad (18)
\]

Noise immunity under high positive \(dv/dt\) can be improved by achieving a higher \(V_{\text{th}} - V_{\text{clamp}}\) and reducing \(V_{\text{spike}}\). Since \(V_{\text{desat,th}}\) is determined by the I-V characteristic and threshold current of the MOSFET, elevating \(V_{\text{th}} - V_{\text{clamp}}\) will lead to a higher voltage divider ratio \(\frac{R_{d2}}{R_{d1} + R_{d2}}\) and a higher \(V_{\text{margin}}\). Comparators’ capability of supporting a high \(V_{\text{th}} - V_{\text{clamp}}\) is critical when selecting the desat comparator. Hence, comparators with higher power supply voltage can support higher \(V_{\text{th}} - V_{\text{clamp}}\) and noise immunity margin. For example, 5 V comparators are more preferable than 3.3 V comparators. Also, comparators with rail-to-rail input voltage range are suggested so that \(V_{\text{th}} - V_{\text{clamp}}\) can be as close to the power supply voltage of the comparator as possible.

Also, comparators with longer propagation delay contribute to better noise immunity of the desat protection, which aids in the comparator to not respond to the extremely short spikes in \(V_{\text{comp}}\). Longer propagation delay of the comparator requires \(V_{\text{comp}}\) to maintain above comparator threshold voltage for a longer time in order to trigger the comparator. In other words, longer propagation delay leads to higher equivalent comparator threshold voltage. The voltage reference used as threshold voltage of the comparator should also be stable and immune from the impact of high \(dv/dt\). The selection and design guidelines about the comparator are summarized in Table 2 to improve the noise immunity of the desat protection.

To reach higher noise immunity margin, \(V_{\text{spike}}\) can be suppressed by reducing \(R_{\text{cla}}\), the parasitic capacitances, the voltage divider impedance, and increasing \(C_d\). If \(R_{\text{cla}}\) is reduced from 20 Ω to 2 Ω in the desat protection design in Fig. 1(a), \(V_{\text{spike}}\) is decreased to 4.1 V with 14% reduction. The reduction is not significant because the noise immunity margin in this case is dominated by the displacement current from \(C_{p3}\), instead of the displacement current from the desat diode. Therefore, if the voltage divider impedance is reduced by 67%, as shown in Fig. 13, \(V_{\text{spike}}\) can be reduced from 4.76 V to 2.1 V. If \(C_{p3}\) is suppressed to 0.001 pF, \(V_{\text{spike}}\) will be reduced to 1.8 V, with details shown in Fig. 14. Increasing \(C_d\) can also lower \(V_{\text{spike}}\) and improve the noise immunity. Fig. 9(b)
demonstrates that $V_{\text{spike}}$ is brought down to 3.6 V with 24% reduction by increasing $C_d$ from 1 pF to 5 pF. Increasing $C_d$ is more effective in improving noise immunity when $t_{\text{rise}}$ is shorter, as indicated in the contour plot of $V_{\text{spike}}$ in Fig. 15. With a long $t_{\text{rise}}$, a large $C_d$ is needed to achieve significant reduction in $V_{\text{spike}}$, which will slow down the response of desat protection. When increasing $C_d$, the trade-off between response time and noise immunity should be considered.

2) EXPERIMENTAL RESULTS
Ac-dc continuous test of the half bridge phase leg based on 10 kV/20 A SiC MOSFETs is utilized to validate noise immunity methods based on discrete components [33]. Details of the test setup are shown in Fig. 16. Parameters of the desat protection implemented in the phase leg are displayed in Fig. 1(a). Voltage signals of the desat protection for the lower MOSFET are measured with a 1 GHz TPP1000 probe (3.9 pF input capacitance) [34]. Powered by 0 V and −5 V rails, ADCMP600 from Analog Devices is selected as the comparator based on the guidelines in Table 2 [35]. The comparator does not have a phase reversal issue and features an input common-mode voltage range beyond the power supply rails. So, the desat comparator will not be spuriously triggered due to interference caused by the negative $dv_{ds}/dt$.

Continuous test results at 6 kV dc link voltage in Fig. 17 show that the peak positive spike in $V_{\text{comp}}$ is 2.56 V with an ideal $V_{\text{margin}}$ of 1.44 V under the positive $dv/dt$. Selecting higher $R_{\text{cla}}$ will reduce $V_{\text{margin}}$ significantly. As shown in Fig. 18, the desat protection for the lower MOSFET is falsely triggered by the positive $dv/dt$ ($\sim 65$ V/ns) during the 6 kV ac-dc continuous test, with $R_{\text{cla}}$ increased from 20 Ω to 90 Ω.

![Figure 15. Contour plot of $V_{\text{spike}}$ as a function of $C_d$ and $t_{\text{rise}}$ (0.004 pF $C_p$; 100 V/ns $dv/dt$).](image)

![Figure 16. Picture of the half bridge phase leg based on 10 kV/20 A SiC MOSFETs under ac-dc continuous test.](image)

![Figure 17. Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with desat protection circuitry shown in Fig. 1(a).](image)

![Figure 18. Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with $90 \, \Omega \, R_{\text{cla}}$. (a) Waveform of $V_{\text{comp}}$ when desat protection is falsely triggered by positive $dv_{ds}/dt$. (b) Waveform of $V_{\text{desat}}$.](image)
The measured spike $V_{\text{spike}}$ in $V_{\text{comp}}$ which falsely triggers the protection is 3.8 V. The equivalent $C_d$ is 5.3 pF with the input capacitance of the passive probe considered. From (5), we can see that the spike in $V_{\text{comp}}$ is composed of two components. The measured peak voltage spike in $V_{\text{desat}}$ is 11.2 V, which generates a positive spike of 1.55 V at $V_{\text{comp}}$. The remaining 2.25 V of the 3.8 V spike in $V_{\text{comp}}$ is due to the displacement current from $C_{p3}$. $R_{d1}$ in the desat protection circuitry shown in Fig. 1(a) is implemented with two 30 kΩ resistors in series, as illustrated in Fig. 19. Therefore, the drain terminal is coupled with the voltage divider via two parasitic capacitances, $C_{p3,a}$ and $C_{p3,b}$. $C_{p3,a}$ and $C_{p3,b}$ are mainly caused by the large drain plate of the discrete 10 kV/20 A SiC MOSFET and the heatsink with the same potential as the drain plate [7], [9], [33]. The finite element analysis in Ansys Q3D reveals that $C_{p3,a}$ and $C_{p3,b}$ are 0.0031 pF and 0.00131 pF, respectively. Based on the analysis in Section II, the additional spike in $V_{\text{comp}}$ due to $C_{p3,a}$ and $C_{p3,b}$ can be calculated as 1.54 V, which is slightly lower than the measured result, 2.25 V. The discrepancy is mainly because the Ansys Q3D analysis only extracts the parasitic capacitance caused by the drain plate and the heatsink. Other objects in the phase leg shown in Fig. 16 which have the same potential as the drain terminal of the MOSFET are not included in the Q3D model. In other words, the finite element analysis results still underestimate the capacitive coupling between the voltage divider and the drain terminal of the MOSFET with high $dv/dt$.

To suppress the capacitive coupling between the protection circuitry and the drain terminal, an external copper shielding layer connected with the source of the MOSFET is installed beneath the desat protection circuitry, since the drain plate of the MOSFET and the heatsink are under the gate driver board. With 90 kΩ $R_{cla}$, the copper shielding reduces the peak voltage spike in $V_{\text{comp}}$ from 3.8 V to 2.2 V, and false triggering of desat protection is eliminated, as shown in Fig. 20. The experimental results also demonstrate that the parasitic capacitances caused by the drain plate and the heatsink result in 1.6 V spike in $V_{\text{comp}}$, which coincides well with the calculated value, 1.54 V. The role played by $C_{p3,a}$ and $C_{p3,b}$ in the generation of a positive voltage spike in $V_{\text{comp}}$ is hence shown. Shielding is also shown to be an effective method to suppress the noise propagated to desat protection circuitry via extremely small parasitic capacitances.

Based on the analysis and experimental results, a new iteration of desat protection circuitry is designed to further boost its noise immunity under high positive $dv/dt$. Numerous methods are adopted simultaneously in PCB layout and component selection. Compared to the design in Fig. 1(a), $R_{d1}$ and $R_{d2}$ are reduced by 66.7%, and $R_{d1}$ is implemented by a single 20 kΩ resistor. $R_{cla}$ is reduced from 20 Ω to 10 Ω. As shown in Fig. 21, the PCB layout is updated to provide the shielding layer and effectively reduce the capacitive coupling between $V_{\text{comp}}$ and the drain terminal of the MOSFET with high $dv/dt$.

To realize the shielding, large grounding planes in the inner layers of the 4-layer PCB are utilized as the shielding layer, and all components of the desat protection circuitry are placed on top layer of the PCB. As displayed in Fig. 21, all components of the protection circuitry in the top layer are surface mount devices, and they are completely shielded by the yellow and blue grounding planes. The traces and pads of $V_{\text{comp}}$ are also minimized to reduce the capacitive coupling. The via connected to $V_{\text{comp}}$ is only for the passive voltage probe to...
measure $V_{\text{comp}}$. This PCB design not only significantly suppresses the influence from parasitic capacitances $C_{p1}$, $C_{p2}$, and $C_{p3}$, but also leads to parasitic capacitance which effectively increases $C_{d}$. According to Q3D analysis, the extracted $C_{p3}$ is 0.82 fF, and inner shielding layers results in an increase of 1.3 pF in $C_{d}$. Further decreasing $R_{\text{cla}}$ will benefit the noise immunity margin, but $R_{\text{cla}}$ and $M_{\text{cla}}$ could be damaged due to high instantaneous current if they are not selected carefully. According to the analytical model, the new iteration should achieve much higher noise immunity margin under $+65 \ V/\text{ns}$ $dv/dt$, with $V_{\text{spike}}$ reduced to 0.42 V.

Ac-dc continuous test results of the new proposed desat protection design in Fig. 22 show that the spike in $V_{\text{comp}}$ is significantly reduced. The measured peak spike in $V_{\text{comp}}$ under $+65 \ V/\text{ns} \ dv/dt$ is 0.5 V, which coincides well with the calculated result, 0.42 V. The voltage spike in $V_{\text{comp}}$ is mainly caused by displacement current from the desat diode. Compared to the original design in Fig. 1(a), the noise immunity margin $V_{\text{margin}}$ increases by 143%.

With the strong noise immunity of the proposed desat protection design fully validated, the installed blanking capacitor $C_{\text{blk}}$ is reduced from 56 pF to 15 pF to accelerate the protection response. Fig. 23 shows the hard switching fault (HSF) short circuit test result of the proposed desat protection design with 15 pF installed $C_{\text{blk}}$ [24], [36]. After the fault is generated, the gate driver responds within 735 ns and safely turns off the MOSFET with a soft turn-off process. The response time is 735 ns, which is defined in this paper as the time interval between the starting point of the fault and the moment when the short circuit current starts to drop. Under a HSF short circuit fault, the response time of the desat protection is mainly dominated by the blanking time [24]. In fact, the response time is only slightly longer than the blanking time. As shown in Fig. 24, HSF short circuit test is also conducted with the desat protection design shown in Fig. 1(a). With 56 pF installed $C_{\text{blk}}$, the desat protection design shown in Fig. 1(a) clears the fault with a response time of 985 ns. So, compared to the desat protection design in Fig. 1(a), the proposed desat protection design with much higher noise immunity margin can also achieve 25.4% shorter response time and 23.2% lower peak short circuit current. Detailed discussion of the response time will not be covered, since it is not the focus of this paper.

Based on the theoretical analysis and experimental results, design guidelines to realize better noise immunity of the desat protection are summarized in Table 3. The design guidelines

![FIGURE 24. HSF short circuit test result of the 10 kV/20 A SiC MOSFET with the desat protection design shown in Fig. 1(a) (56 pF installed $C_{\text{blk}}$).](image)

<table>
<thead>
<tr>
<th>Design guideline</th>
<th>Detailed guideline</th>
<th>Design trade-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduce $C_{p1}$, $C_{p2}$, and $C_{p3}$</td>
<td>Design shielding layer and/or box when doing PCB layout</td>
<td>Slightly slower response due to slightly higher $C_{d}$</td>
</tr>
<tr>
<td>Reduce $R_{\text{di}}$</td>
<td>Reduce voltage divider impedance</td>
<td>Slightly higher loss and slightly slower protection response</td>
</tr>
<tr>
<td>Reduce $C_{\text{d}}$</td>
<td>Select or implement desat diode with low parasitic capacitance as possible</td>
<td>Increasing cost and perhaps size</td>
</tr>
<tr>
<td>Reduce $R_{\text{cla}}$</td>
<td>Select a low $R_{\text{cla}}$, $R_{\text{cla}}$ and $M_{\text{cla}}$ need to handle higher pulse current</td>
<td>Case by case</td>
</tr>
<tr>
<td>Reduce $I_{\text{d}}$</td>
<td>Achieve lower parasitic inductance in PCB layout and connection</td>
<td></td>
</tr>
<tr>
<td>Add $R_{\text{comp}}$</td>
<td>Use slightly higher $R_{\text{comp}}$ if $L_{\text{d}}$ is relatively large Requirement: $R_{\text{comp}} &lt;&lt; R_{\text{cla}}$</td>
<td>No considerable trade-off; little impact on response time</td>
</tr>
<tr>
<td>Increase $C_{d}$</td>
<td>Add a small external capacitor (&lt;10 pF) to increase $C_{d}$</td>
<td>Slightly slower protection response</td>
</tr>
</tbody>
</table>
in Table 3 do not have substantial impact on the response time of the desat protection, although some may slightly slow the protection response. Like the desat protection realized by a gate driver IC, it is not recommended to select larger $C_{blk}$ to improve noise immunity of the desat protection based on discrete components. So, strong noise immunity and fast response do not contradict with each other. By following the design guidelines in Table 3, the response time of the desat protection based on discrete components should only be limited by the blanking time requirement.

Fundamentally speaking, the noise coupled with the voltage divider usually plays a more dominant role, which has the capability of generating considerable voltage spike via extremely small parasitic capacitances ($<0.01$ pF). Among the design guidelines in Table 3, two design guidelines related to the voltage divider have a higher priority, including reducing voltage divider impedance and reducing $C_{p3}$. Because of the high $dv/dt$ with long duration, it is important to reduce $C_{p3}$ as much as possible, even when it is already smaller than 0.01 pF. In general, to achieve strong noise immunity under high $dv/dt$, the most effective and fundamental method is to eliminate all capacitive coupling between the protection circuitry and the drain terminal with high $dv/dt$, instead of only focusing on the parasitic capacitance caused by the desat diode.

**IV. CONCLUSION**

Noise immunity of the desat protection for high voltage SiC MOSFETs is analyzed in this paper. Two mainstream implementations of the desat protection are studied, including the desat protection circuitry based on discrete components and the implementation with a gate driver IC with integrated desat protection function. The desat protection can be falsely triggered by both high positive $dv_{ds}/dt$ and negative $dv_{ds}/dt$ generated by high voltage SiC MOSFETs. Because of the long duration of the high $dv/dt$ generated by high voltage SiC MOSFETs, the extremely small parasitic capacitance ($<0.01$ pF) coupled with the voltage divider could have large influence on the noise induced into the desat protection circuitry based on discrete components. Other factors’ effect on noise is also studied, such as parasitic inductance, voltage divider impedance, damping resistance, and duration of high $dv/dt$.

The main concern with negative $dv_{ds}/dt$ is the resulting negative voltage spike that can falsely trigger the desat comparator with the phase reversal issue. Hence, the noise immunity under the negative $dv_{ds}/dt$ can be improved by selecting comparators without phase reversal issue and adding clamping diodes.

The more challenging issue is the high positive $dv_{ds}/dt$, which lasts for a much longer time than that generated by 1.2 kV and 1.7 kV SiC MOSFETs. The analytical model of the noise immunity margin is established to support the noise immunity improvement under high positive $dv/dt$. The noise immunity analysis and improvements are supported by simulation and experimental results. Different methods and their experimental validation based on the derived noise immunity margin are presented to enhance the noise immunity. Comprehensive design guidelines to boost noise immunity are summarized, including circuit design, component selection, and PCB layout. None of the design guidelines recommended in this paper to improve noise immunity will slow down the protection response significantly, and hence can be fully leveraged when designing the desat protection with fast response and strong noise immunity.

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LEON M. TOLBERT (Fellow, IEEE) received the bachelor’s, M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 1989, 1991, and 1999, respectively. He is currently a Chancellor’s Professor and the Min H. Kao Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN, USA. He is a Founding Member and Testbed Thrust Leader of the NSF/DOE Engineering Research Center, Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT). He is also an adjunct participant with Oak Ridge National Laboratory. His research interests include the utility applications of power electronics, microgrids, electric vehicles, and wide bandgap semiconductors. Dr. Tolbert was the recipient of the 2001 IEEE Industry Applications Society Outstanding Young Member Award, and eight prize paper awards from the IEEE Industry Applications Society and IEEE Power Electronics Society. He was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2007 to 2013 and the Paper Review Chair of the Industry Power Converter Committee of the IEEE Industry Applications Society from 2014 to 2017. He is currently the Academic Deputy Editor-in-Chief of the IEEE Power Electronics Magazine during 2021–2023.

WILLIAM GIEWONT received the bachelors’ degree in electrical engineering from Penn State University, State College, PA, USA, in 1979. He is currently the Chief Technical Officer/Engineer of EPC Power developing high efficiency, grid interactive multi-megawatt power converters. He started his career with General Electric, where he spent two decades developing industrial motor controls and power converters for a variety of applications. He has held lead positions with Danfoss Drives/Vacon, including the Director of Technology and Innovation, Director of Engineering, and Chief Engineer MV Drives. He also consults on power electronic research projects for The University of Tennessee CURENT Education Research Center and North Carolina State University FREEDM Systems Center. In total he has more than four decades of experience as a Researcher and Developer of power electronic converters and controls. His research and development interests include power electronics, power systems and controls.