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Improved multiline HVDC circuit breakers with asymmetric conducting branches

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ABSTRACT

This paper proposes two improved multiline HVDC circuit breakers (DCBs) for HVDC grid applications, including type-1 improved multiline DCB and type-2 improved multiline DCB. The two improved DCBs draw on the core idea of extended H-bridge. *m* adjacent DC transmission lines share a single main breaker (MB) and surge arrester. Due to the extended H-bridge design, bidirectional current flow can be achieved by a unidirectional MB. An upper conducting branch and a lower conducting branch are connected to a DC line. The upper and lower conducting branches in the two improved multiline DCBs are asymmetric. The upper conducting branch of both two improved DCBs is formed by a load commutation switch (LCS) and an ultra-fast disconnector (UFD). The lower conducting branch of the type-1 improved scheme is composed of a diode and a UFD; and of the type-2 improved scheme is made up of diode stack. Compared with other DCBs, the proposed type-1 DCB and type-2 DCB are more cost effective. Among the five DCBs, the type-2 improved scheme requires the least number of individual switching actions. The effectiveness and feasibility of the proposed schemes are verified through simulation of a bipolar three-terminal HVDC grid in PSCAD/EMTDC.

1. Introduction

High voltage direct current (HVDC) grid has been a research hotspot in recent years [1–4]. HVDC grid can be used to exchange power freely from country to country or even from continent to continent. In addition, HVDC grid is referred to a good solution for offshore wind power integration. However, there are many challenges in developing HVDC grids. One of them is DC fault clearance [5–7]. Generally, three ways can be used to clear DC faults: tripping AC circuit breaker, applying fault-blocking converter and adopting DC circuit breaker (DCB). Among them, adopting DCB is considered the best way to clear DC faults quickly and minimize the impact on AC/DC system operation.

At present, the research schemes of DCBs mainly focus on three types [8]: electromechanical DC circuit breakers based on conventional switches [9–11], solid-state DC circuit breakers based on pure power electronic devices [12–15] and hybrid DC circuit breakers based on both [16–23]. The hybrid DCB combines the advantages of the other two kinds of DCBs, which has low power loss and fast operating speed. The hybrid DCB has a very good application prospect and many new DCB schemes use the core idea of this hybrid structure for reference [24,25].

Although a typical hybrid DCB has the advantages mentioned above, its main breaker branch contains hundreds of power electronic switches to withstand the transient interruption voltage. Thus, the cost of a typical hybrid DCB remains expensive. Furthermore, the number of hybrid DCBs required in a fully selective fault clearing scheme is determined by the number of DC transmission lines rather than by the number of converters. A meshed HVDC grid will have multiple converters with many transmission lines. As a result, the number of hybrid DCBs required will increase substantially, resulting in significant costs.

Recently, scholars have been working on how to reduce the cost of DCB [26–38]. In general, these researchers attempt to reduce the DCB capital cost based on three methods: sharing DCB components, modifying current communication circuit and employing H-bridge configuration. An interlink DCB is investigated in [26]. In this DCB, half of the

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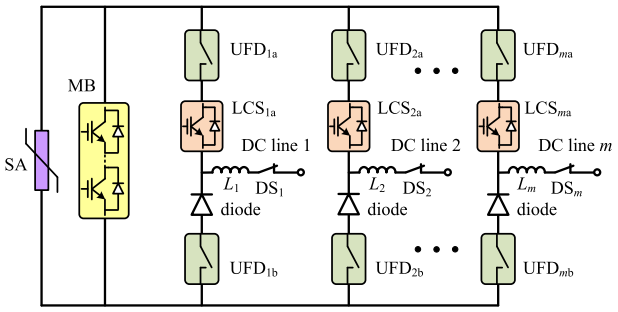

Fig. 1. Type-1 improved multiline DCB.

main breaker units are shared among the adjacent lines. But the cost of the interlink DCB is still high. In addition to the main breaker units, half of the load commutation switches (LCSs) are also shared in the multiport DCB in [28]. Since the main breaker is the most expensive component of the DCB, reference [30] further reduces the cost of the DCB by sharing the whole rather than half of the main breaker. This means that when there are multiple adjacent lines connected to a converter, only one main breaker is needed.

Modifying current communication circuit is another method to reduce the DCB cost. By applying this method, the DCB only contains mechanical breaker in its normal conducting branch, while its current communication branch is formed by a modified current communication circuit with pre-charged capacitor [31,32]. In this way, no LCS is used and the number of semiconductor switch is reduced. Besides, the conduction loss of the DCB could be reduced to be comparable with AC circuit breaker. Based on this idea, references [33,34] expand the topology into multi-line configuration so that more semiconductor switches can be saved. However, during fault isolation, electric arc is generated in these DCBs and external power source is required to precharge the capacitor.

The third method to reduce the DCB cost is to employ H-bridge configuration. The main breaker in [35] is formed in H-bridge structure which consists of a single high voltage IGBT valve and 4 diode stacks. In this DCB, bidirectional current interruption can be achieved by the unidirectional IGBT valve. So half amount of IGBTs are saved in the main breaker. Reference [36] used the similar structure as [35], but the 4 diode valves are replaced with 2 double-throw ultrafast disconnectors (UFDs). For the first time, the whole structure of the DCB is designed in H-bridge with a LCS and a UFD forming an arm in [37]. A multiline DCB is proposed in [38] by extending the structure of [37] to multiple DC lines. The most important advantage of this DCB is that when there are many adjacent lines connected to the converter, only one unidirectional main breaker is needed. This advantage makes the multiline DCB highly economical. However, the number of LCSs and UFDs are double. Besides, more individual switching actions are required for the multiline DCB than the hybrid DCB when clearing a DC fault, which might affect its reliability.

To overcome the drawbacks of the conventional multiline DCB, two improved multiline DCBs are proposed in this paper. The type-1 improved multiline DCB replaces the LCS in each lower conducting branch with a diode, so that the capital cost of the DCB is further reduced. Compared with the conventional multiline DCB, the type-2 improved DCB replaces the whole lower conducting branch with diode stack and the control strategy is also modified accordingly. In this way, the number of individual switching actions can be reduced, which can enhance the reliability of the DCB.

The rest of this paper is organized as follows. Section 2 discusses the type-1 improved multiline DCB. The basic topology, operation principle

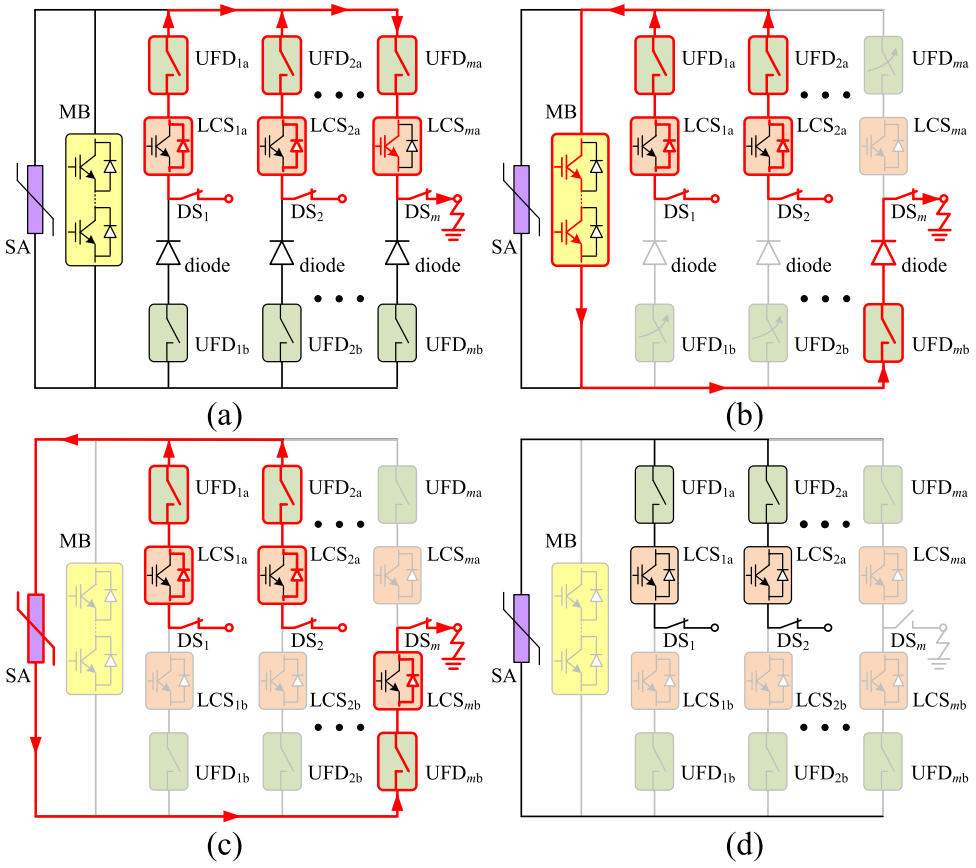

Fig. 2. DC fault interruption operation of the type-1 improved multiline DCB. (a) DC fault occurs. (b) Open LCS_{ma}, UFD_{ma} and $UFD_{1b} \sim LCS_{(m\text{-}1)b}$. (c) Open MB. (d) Open DS_m.

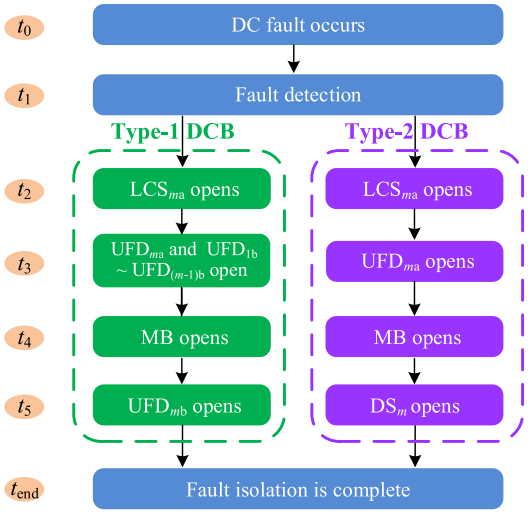

Fig. 3. DC faults isolation process with type-1 and type-2 DCBs.

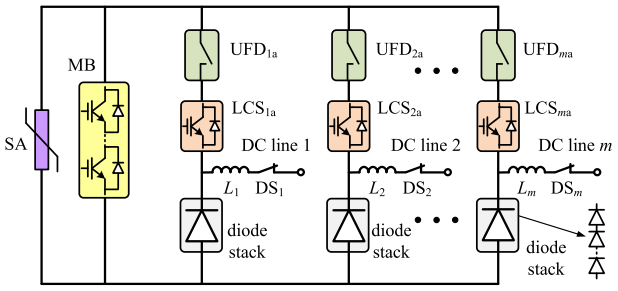

Fig. 4. Type-2 improved multiline DCB.

of the type-2 improved multiline DCB are presented in Section 3. Section 4 proposes the improved DCBs used in negative pole. The reclosing process is studied in Section 5. Section 6 carries out the comparative analysis of the five DCBs. Section 7 presents the simulation results in PSCAD/EMTDC, which verifies the validity and feasibility of the proposed DCBs. Finally, the conclusions of the paper are discussed in Section 8.

2. Type-1 improved multiline HVDC circuit breaker

The topological structure of the type-1 improved multiline DCB is presented in Fig. 1. Supposing that there are m DC lines connected to a converter, then the type-1 multiline DCB contains m upper conducting branches, m lower conducting branches, a transferring branch and an energy absorption branch. Each upper conducting branch includes one UFD and one LCS, while each lower conducting branch consists of a single diode and a UFD. One upper conducting branch and one lower conducting branch are series-connected and their common point is connected to a DC line. The main breaker (MB) which is the core component of the DCB forms the transferring branch. The energy absorption branch consists of surge arresters (SAs). The m current limiting reactors are used to mitigate the rate of current rise during DC fault period. The residual current disconnecting switch (DS) has two main roles. One role is to isolate the DCB from the system during a DC fault or routine maintenance. The other role is to chop the residual current so that the DC fault clearing time can be reduced [39]. Typically, the residual current threshold is a few tens to a few hundreds of amperes.

In normal operation, all switches of the type-1 improved multiline DCB are closed. The load current only flows through the upper conducting branches due to the high resistance of the MB. Assuming that a DC fault occurs on DC line m. The DC fault interruption operation based on the type-1 improved multiline DCB is as follows:

1) As soon as the DC fault occurs at time t_0, all the connected lines inject current into the fault point, leading to a high overcurrent [see Fig. 2 (a)].
2) When a DC fault is detected at time t_1, the faulty line is disconnected from the upper DC bus by opening the upper LCS and UFD, while the healthy lines are disconnected from the lower DC bus by opening the lower UFDs. Detail actions are described below. When the fault current flowing through the upper conducting branch reaches a preset value, the LCS_{ma} opens immediately at time t_2. The fault current will then commutate to the MB branch. As the current flowing through the UFD_{ma} decreases to zero and the voltage across it is under a fairly low level, the UFD_{ma} can be opened at time t_3 in order to fully open the faulty upper conducting branch. At the same time, UFD_{1b} ~ $LCS_{(m-1)b}$ are opened to isolate the healthy lines from the lower DC bus [see Fig. 2 (b)].
3) After the UFDs are fully opened, the MB opens to cut off the fault current at time t_4. The remaining energy will be consumed through the SA [see Fig. 2 (c)].
4) Once the fault current flowing through the faulty line drops to residual current level, the mechanical disconnector DS_m connected to the faulty line is opened to isolate the faulty line from the rest of the system at time t_5 [see Fig. 2 (d)].

The flowchart of DC faults isolation process with type-1 DCB is shown in Fig. 3. It should be noted that the required voltage rating of the diode in the type-1 improved multiline DCB is small, because the UFD isolates the diode from the primary voltage across the SA during current breaking.

3. Type-2 improved multiline HVDC circuit breaker

The proposed type-2 improved multiline DCB is shown in Fig. 4. Compared with the type-1 improved multiline DCB, the lower conducting branches of the type-2 improved multiline DCB are formed by diode stacks. As there is no LCS and UFD in the lower conducting branches, no switching actions are required for them during DC fault isolation process. This can also make the improved multiline DCB easier to operate.

In normal operation, all switches of the type-2 improved multiline DCB are closed. Assuming that a DC fault occurs on DC line m. The DC fault interruption operation based on the type-2 improved multiline DCB is as follows:

1) When the DC fault occurs on DC line m at time t_0, all the connected lines inject current into the fault point, leading to a high overcurrent [see Fig. 5 (a)].
2) When the fault current flowing through the upper conducting branch reaches a preset value at time t_1, the LCS_{ma} opens immediately at time t_2. The fault current will then commutate to the MB branch. Then the UFD_{ma} can be opened at time t_3 in order to fully open the faulty upper conducting branch [see Fig. 5 (b)].
3) The MB opens at time t_4 to cut off the fault current. The remaining energy is released by the SA [see Fig. 5 (c)].
4) When the current flowing through the SA drops to zero at time t_5, the DS_m opens and isolates the faulty line from the rest of the system [see Fig. 5 (d)].

The flowchart of DC faults isolation process with type-2 DCB is shown in Fig. 3. Different from the diodes used in the type-1 improved multiline DCB, the diode stacks in the type-2 improved multiline DCB need to tolerate system transient overvoltage. Thus, lots of diodes need to be connected in series in one diode stack. There are many reference cases that diode stack withstands system overvoltage [35,40–42], so it is

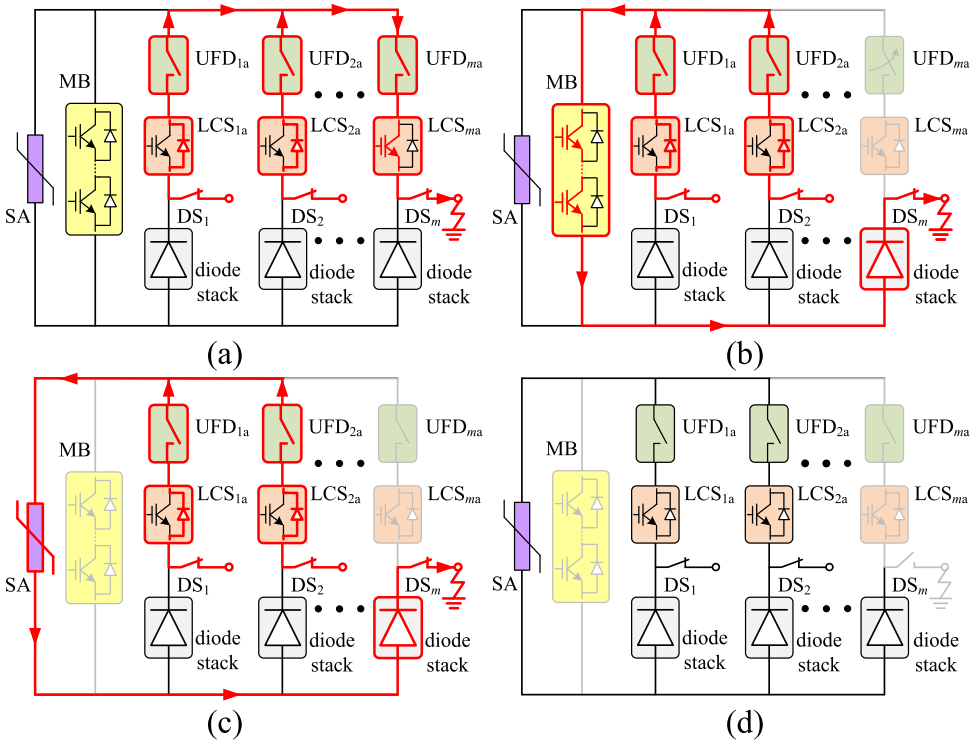

Fig. 5. DC Fault interruption operation of the type-2 improved multiline DCB. (a) DC fault occurs. (b) Open LCS_{ma} and UFD_{ma}. (c) Open MB. (d) Open DS_m.

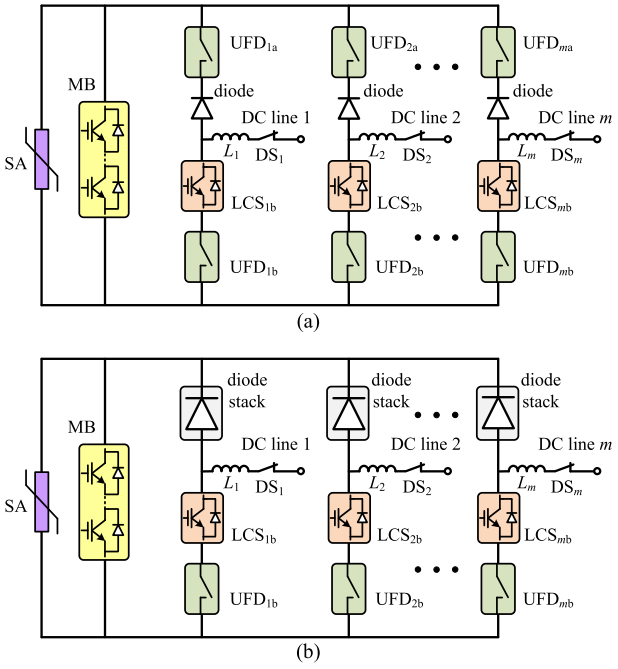

Fig. 6. Improved multiline DCBs used in negative pole. (a) Type-1 improved multiline DCB. (b) Type-2 improved multiline DCB.

possible and practical to use diode stack in the lower conducting branch.

4. Improved multiline DCBs used in negative pole

For a DC pole-to-ground fault occurred in the negative pole, the fault current flowing path is different from that of the positive pole-to-ground fault. So the topologies of improved multiline DCBs used in negative pole are also different which are shown in Fig. 6. Comparing Fig. 1, Fig. 4 and Fig. 6 it is seen that the upper and lower conducting branches are exchanged. Their operation sequences are similar to that shown in Fig. 2 and Fig. 5, which will not discussed in this paper.

5. Reclosing process

The overhead lines are widely used in the HVDC system. Thus, effective reclosing strategy is needed after a DC fault to improve the system reliability. The reclosing processes of the two improved multiline DCBs are similar. Here only discusses the reclosing process of the type-2 improved multiline DCB.

Before reclosing a DCB, it needs to cool down the arrester bank and deionize the DC line. The time required to cool down the arrester bank is relatively short as there is cooling system in the DCB. DC line deionization time is the main factor that affects the reclosing time of a DCB. In general, the DC line deionization time is in the range of 150 ms ~ 500 ms [6]. The typical deionization time is 300 ms which is also used in the testing for 500 kV modular cascaded hybrid HVDC breaker prototype [43]. The reclosing command is activated after a successful arc extinguishing and DC fault is deionized. The MB will be firstly reclosed to conduct current again. If the DC fault is permanent, current will inject to the fault point once again. When the fault current reaches the protection threshold, MB will be turned off. Finally, DS_m opens and isolates the faulty line from the rest of the system. If the DC fault is temporary and has been cleared before reclosing the MB, the current does not reach the protection threshold again. Then UFD_{ma} and LCS_{ma} will be reclosed one after another. Finally the system will be restored to pre-fault operating state.

6. Comparative analysis

The economic efficiency and the reliability are two important indices for the DCBs. In this section, these two indices of the five DCBs with LCS are compared: including the multiport DCB proposed in [28] (scheme 1), the integrated DCB proposed in [30] (scheme 2), the multiline DCB proposed in [38] (scheme 3), and type-1 (scheme 4) and type-2 (scheme

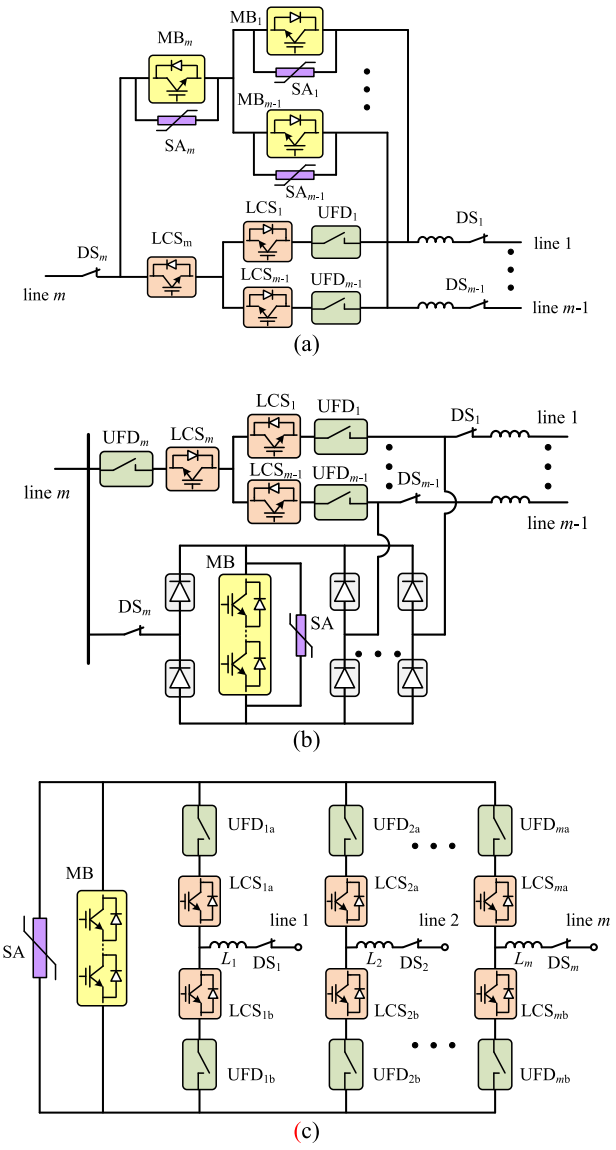

Fig. 7. Three existing DCBs for comparison. (a) Scheme 1: multiport DCB. (b) Scheme 2: integrated DCB. (c) Scheme 3: multiline DCB.

5) improved DCBs proposed in this paper. The DCB topologies of scheme 1, 2 and 3 are shown in Fig. 7 (a), Fig. 7 (b) and Fig. 7 (c) respectively. Detailed operation principles of these three DCBs are presented in [28,30,38].

6.1. Economic efficiency

Assuming that the rated DC voltage is 320 kV, the system transient overvoltage is 1.6 pu. The 5SNA 3000 K452300 IGBT module [44] is used for the LCS and MB. The voltage rating of this IGBT module is 4.5 kV, the current rating is 3 kA and the peak current is 6 kA. The 5SDD 38H5000 [45] is used for the diode stacks. This diode has voltage rating of 5 kV and maximum peak forward surge current of 45 kA (10 ms wide, half sine-wave current pulse). It should be noted that each IGBT module contains one IGBT and one anti-parallel diode.

The maximum voltage of the LCS can be estimated by [39]

$$\widehat{V}_{\mathrm{LCS}} \approx \frac{L_3(V_{\mathrm{DC}} - V_{\mathrm{CA}}) + L_{\mathrm{DC}} V_{\mathrm{ON}}}{L_{\mathrm{DC}} + L_3} + I_0\sqrt{\frac{L_2 + L_3}{C_1}} \tag{1}$$

where, V_{DC} is the voltage at the converter side, V_{CA} the voltage at the DC line side, V_{ON} is the on state voltage of MB branch, L_{DC} is the current limiting inductance, I_0 is the commutation current, L_2 and L_3 are the inductances of normal branch and MB branch, C_1 is the parallel capacitance of the LCS. For example [39], when I_0 is 3 kA, V_{ON} is 1 kV, the peak LCS voltage is 8 kV. Thus, the number of series IGBT modules required in each LCS is

$$n_{\mathrm{IGBT\_LCS}} = \frac{\widehat{V}_{\mathrm{LCS}}}{(1 - S_{\mathrm{f}})\widehat{V}_{\mathrm{IGBT}}} = \frac{8\ \mathrm{kV}}{\left(1 - \frac{1}{3}\right) \times 4.5\ \mathrm{kV}} = 3 \tag{2}$$

where $\widehat{V}_{\mathrm{IGBT}}$ is the voltage rating of IGBT, S_{f} is the safety margin used in the design which is selected as 1/3 in this paper. Therefore, one unidirectional LCS consists of 3 IGBTs and 3 diodes.

The system transient overvoltage is 1.6 pu which is 512 kV. Thus, the maximum voltage across the MB is $\widehat{V}_{\mathrm{MB}} = 512$ kV. The number of IGBT modules in one unidirectional MB can be calculated as

$$n_{\mathrm{IGBT\_MB}} = \frac{\widehat{V}_{\mathrm{MB}}}{(1 - S_{\mathrm{f}})\widehat{V}_{\mathrm{IGBT}}} = \frac{512\ \mathrm{kV}}{\left(1 - \frac{1}{3}\right) \times 4.5\ \mathrm{kV}} = 171 \tag{3}$$

Because each IGBT module contains one IGBT and one anti-parallel diode, one unidirectional MB is formed with 171 IGBTs and 171 diodes.

The diode stack used in scheme 2 and the proposed type-2 improved DCB also needs to tolerate system overvoltage. The transient overvoltage is 512 kV and the voltage rating of each diode is 5 kV, so the required number of series diodes in each diode stack is

Table 1
Economic Efficiency Comparison of the Five DCBs.

	Scheme 1 in [28]	Scheme 2 in [30]	Scheme 3 in [38]	Scheme 4 (type-1 DCB in this paper	Scheme 5 (type-2 DCB in this paper
Number of UFDs	m-1	m	$2m$	$2m$	m
Number of LCSs	m	m	$2m$	m	m
Number of DSs	m	m	m	m	m
Number of arresters	m	1	1	1	1
Number of MBs	m	1	1	1	1
Extra diode stacks	0	$2m$ (diode stacks)	0	m (diodes)	m (diode stacks)
Total number of IGBTs	$174m$	$3m + 171$	$6m + 171$	$3m + 171$	$3m + 171$
Total number of diodes	$174m$	$311m + 171$	$6m + 171$	$4m + 171$	$157m + 171$

Table 2
Number of Individual Switching Action for the Five DCBs.

	Scheme 1 in [28]	Scheme 2 in [30]	Scheme 3 in [38]	Scheme 4 (type-1 DCB in this paper	Scheme 5 (type-2 DCB in this paper
LCS	$2m$	1	$m + 1$	1	1
UFD	1	1	$m + 1$	$m + 1$	1
MB	m	1	1	1	1
DS	1	1	0	0	1
Total switching actions	$3m + 2$	4	$2m + 3$	$m + 3$	4

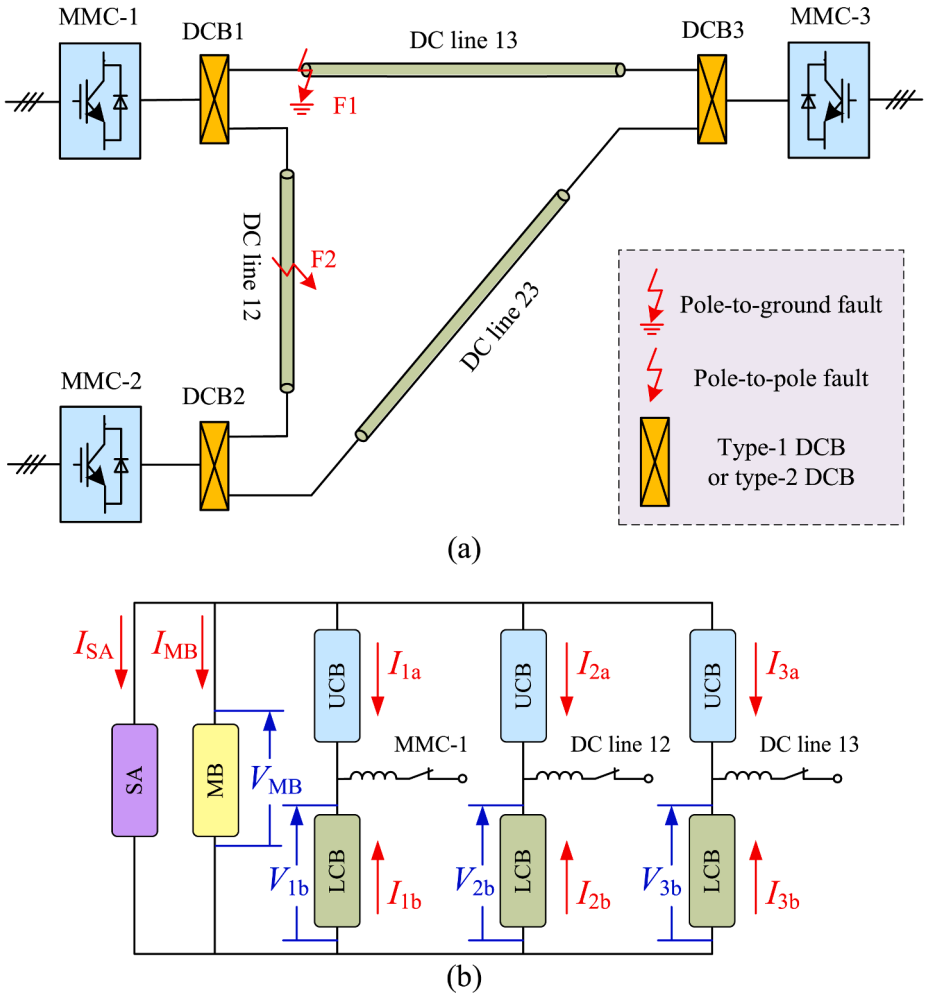

Fig. 8. Three-terminal bipolar HVDC grid. (a) Structure of HVDC grid. (b) Positive direction of voltages and currents of DCB1.

Table 3
Main circuit parameters.

	Items	Values
DC side	Voltage control in MMC-3	±320 kV
	Length of each DC line	100 km
	Resistance per unit length	0.01 Ω/km
	Inductance per unit length	0.85 mH/km
	Capacitance per unit length	0.013 μF/km
AC side	Active power control in MMC-1	600 MW
	Active power control in MMC-2	400 MW
	AC system voltage (L-L, RMS)	230 kV
	Transformer capacity	1.2p.u.
	Transformer ratio	230 kV/166 kV
	Transformer leakage	0.15p.u.
Converter	Number of SMs per arm	200
	SM capacitance	10 mF
	Capacitor voltage	1.6 kV
	Arm inductance	60 mH

$$n_{\mathrm{D\_stack}} = \frac{\widehat{V}_{\mathrm{TOV}}}{(1-S_{\mathrm{f}})\widehat{V}_{\mathrm{D}}} = \frac{512\ \mathrm{kV}}{\left(1-\frac{1}{3}\right)\times 5\ \mathrm{kV}} = 154 \tag{4}$$

1) Scheme 1

As for scheme 1, a part of the MBs, arresters and LCSs are shared among adjacent lines. Totally there are m-1 UFDs, m unidirectional LCSs, m unidirectional MBs, m arresters and m DSs in scheme 1. According to and , the number of IGBTs used in scheme 1 is calculated as

$$n_{\mathrm{IGBT\_scheme1}} = n_{\mathrm{IGBT\_LCS}}\cdot m + n_{\mathrm{IGBT\_MB}}\cdot m = 3m + 171m = 174m \tag{5}$$

The number of diodes used in scheme 1 is the same as IGBTs, which is also 174 m.

2) Scheme 2

Components of MB, SA and half amount of LCSs in scheme 2 are shared among the adjacent lines. Totally, scheme 2 consists of m unidirectional LCSs, m UFDs, m DSs, 2 m diode stacks, one unidirectional MB and one SA. The total number of IGBTs used in scheme 2 is given by

$$n_{\mathrm{IGBT\_scheme2}} = n_{\mathrm{IGBT\_LCS}}\cdot m + n_{\mathrm{IGBT\_MB}} = 3m + 171 \tag{6}$$

Different from scheme 1, the number of diodes used in scheme 2 also contains those in diode stacks. The total number of diodes adopted in scheme 2 is

$$n_{\mathrm{D\_scheme2}} = n_{\mathrm{D\_stack}}\cdot 2m + (3m + 171) = 311m + 171 \tag{7}$$

3) Scheme 3

Scheme 3 uses the H-bridge structure and only one MB is needed. But the number of UFDs and LCSs connected to one DC line increase from one to two. In total, there are 2 m UFDs, 2 m unidirectional LCSs, one unidirectional MBs, one arrester and m DSs in scheme 3. The total

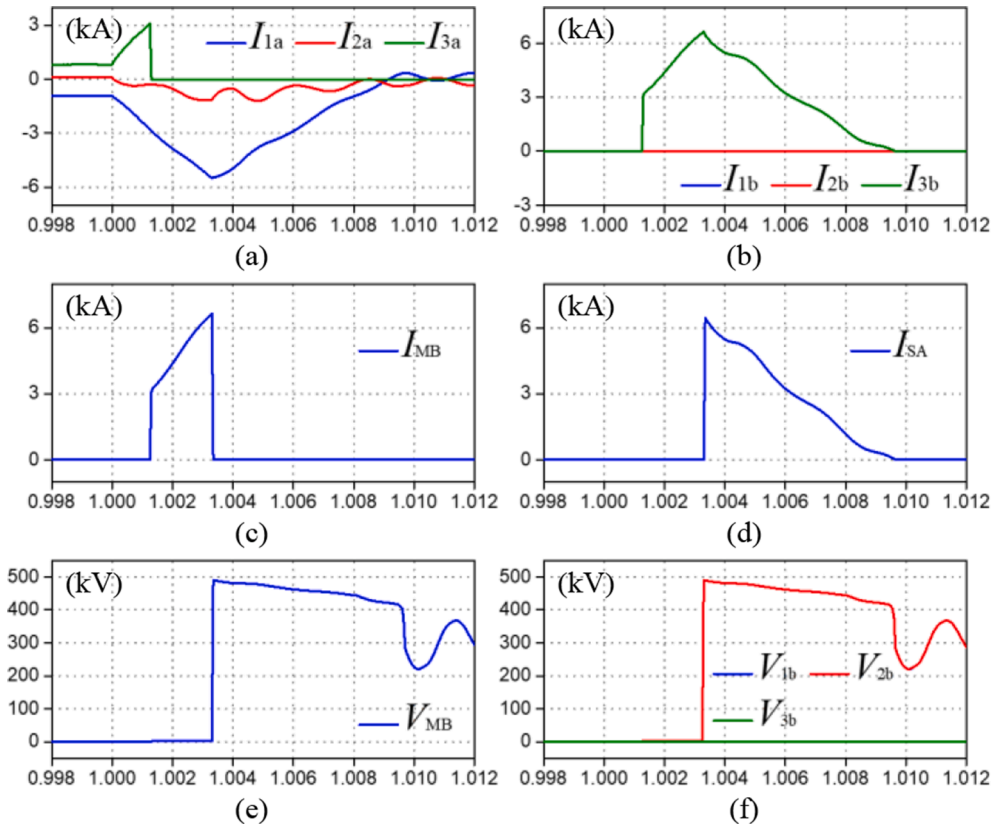

Fig. 9. Response of type-1 DCB under pole-to-ground fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of lower conducting branches.

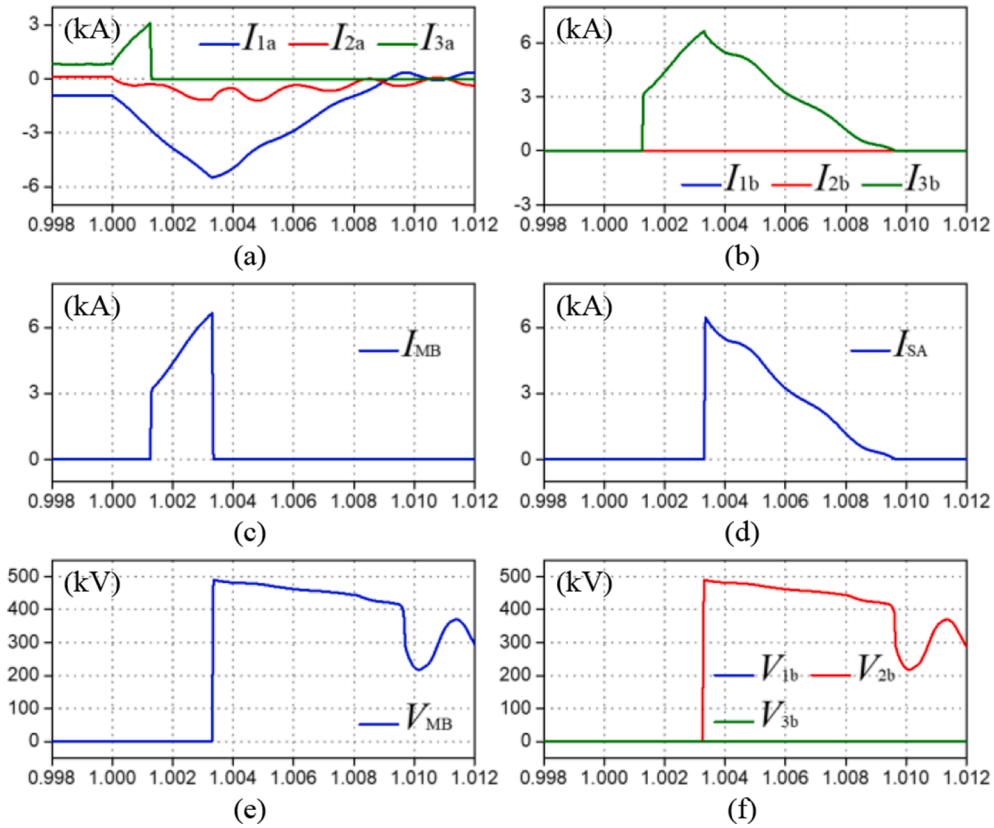

Fig. 10. Response of type-2 DCB under pole-to-ground fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of lower conducting branches.

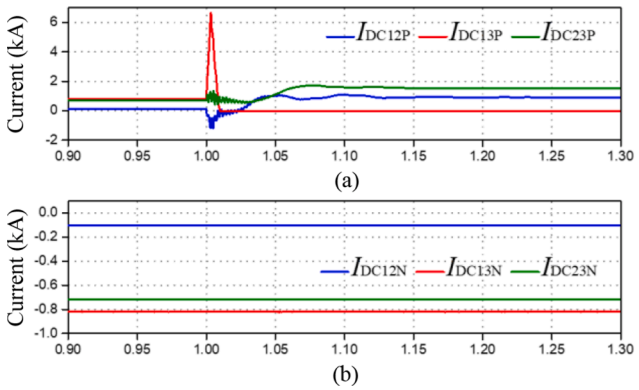

Fig. 11. DC line currents under pole-to-ground fault. (a) Positive pole. (b) Negative pole.

numbers of IGBTs and diodes used in scheme 3 are the same, which can be calculated as

$$n_{IGBT\_scheme3} = n_{D\_scheme3} = n_{IGBT\_LCS} \cdot 2m + n_{IGBT\_MB} = 6m + 171 \quad (8)$$

4) Scheme 4

For scheme 4 (the type-1 DCB proposed in this paper), there are 2 m UFDs, m unidirectional LCSs, one unidirectional MBs, one arrester, and m DSs. The number of IGBTs used in this DCB is

$$n_{\text{IGBT\_scheme4}} = n_{\text{IGBT\_LCS}} \cdot m + n_{\text{IGBT\_MB}} = 3m + 171 \quad (9)$$

The number of diodes is

$$n_{\text{D\_scheme4}} = n_{\text{IGBT\_LCS}} \cdot m + n_{\text{IGBT\_MB}} + m = 4m + 171 \quad (10)$$

5) Scheme 5

For scheme 5 (the type-2 DCB proposed in this paper), there are m UFDs, m unidirectional LCSs, one unidirectional MBs, one arrester, m DSs and m diode stacks. The number of IGBTs in scheme 5 is given by

$$n_{\text{IGBT\_scheme5}} = n_{\text{IGBT\_LCS}} \cdot m + n_{\text{IGBT\_MB}} = 3m + 171 \quad (11)$$

The number of diodes is calculated as

$$n_{D\_scheme5} = n_{IGBT\_LCS} \cdot m + n_{IGBT\_MB} + n_{D\_stack} \cdot m = 3m + 171 + 154m = 157m + 171 \quad (12)$$

Table 1 shows the comparison results of the five DCBs. It is seen that the number of IGBTs used in scheme 1 is far more than the other four DCBs. So scheme 1 is the most expensive DCB among the five schemes. Comparing scheme 2 with scheme 5 (typy-2 DCB) we can see that the latter uses less diodes than the former one and has higher economic efficiency. When we compare scheme 3 with scheme 4 (type-1 DCB), both IGBTs and diodes used in scheme 4 are less than those used in scheme 3. Therefore, among the five DCBs, the proposed type-1 DCB and type-2 DCB are more cost effective than the other three DCBs.

6.2. Number of individual switching action

During DC fault clearing, if there are more individual switching actions for a DCB, it is less reliable. Thus, it is very important to reduce the number of DCB individual switching action. In this subsection, different DCBs are compared in terms of this index.

The DC fault isolating process of scheme 1 is presented in [28]. Based on this process, the number of individual switching action of scheme 1 is

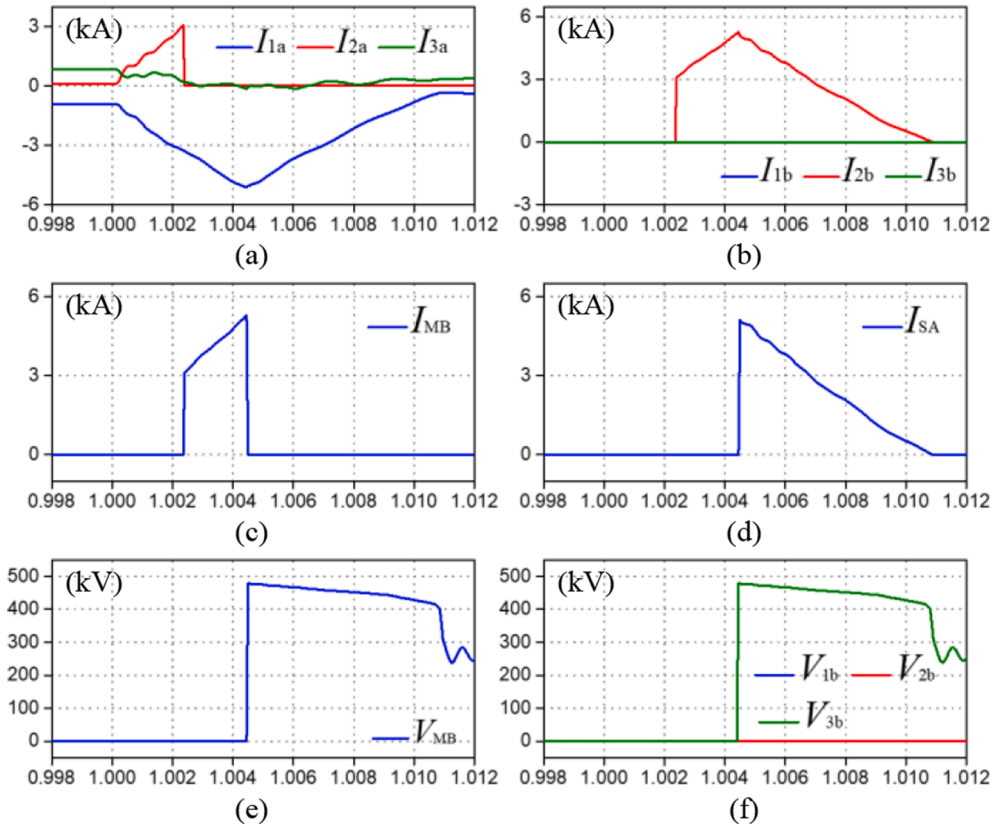

Fig. 12. Response of type-1 DCB under pole-to-pole fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of lower conducting branches.

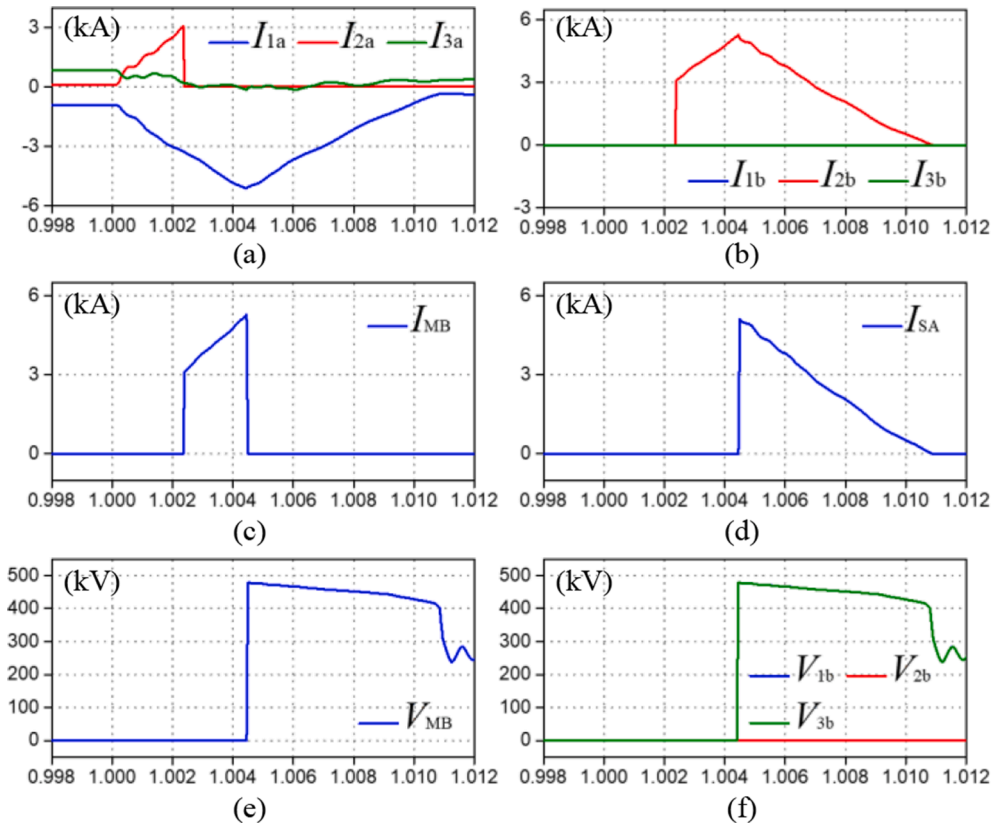

Fig. 13. Response of type-2 DCB under pole-to-pole fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of lower conducting branches.

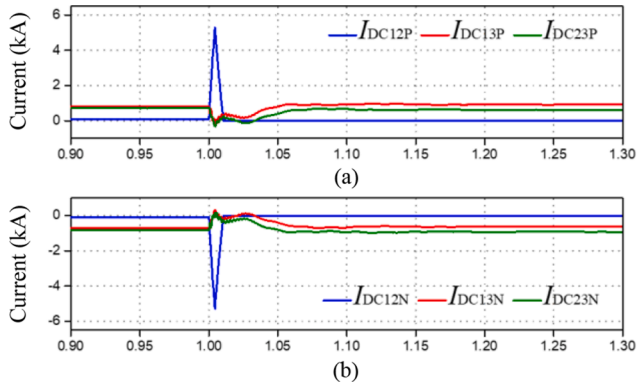

Fig. 14. DC line currents under pole-to-pole fault. (a) Positive pole. (b) Negative pole.

$4m + 2$ ($2m$ for the LCS, one for the UFD, $2m$ for the MB and one for the DS).

As for scheme 2 proposed in [30], the individual switching action is reduced significantly. Because diode stacks with no switching action are used in this DCB. Total, the number of individual switching action for scheme 2 is 4 (one for the LCS, one for the UFD, one for the MB and one for the DS).

In the process of isolating a DC fault, scheme 3 proposed in [38] requires $2m + 3$ individual switching actions ($m + 1$ for the LCS, $m + 1$ for the UFD and one for the MB).

As for the type-1 improved multiline DCB, these numbers are one for the LCS, $m + 1$ fot the UFD and one for the MB, respectively. Therefore, the total is $m + 3$. Whereas for the type-2 improved multiline DCB, only one LCS, one UFD, one MB and one DS are required to take action. So the total actions for the type-2 improved multiline DCB is 4.

The comparison results are shown in Table 2. It can be seen that among the five DCBs, scheme 2 and the proposed type-2 DCB are the most reliable one; the proposed type-1 DCB has better performance in reliability than scheme 1 and scheme 3.

7. Case study

7.1. Simulation system

To verify whether the proposed improved multiline DCBs are valid and feasible, a three-terminal bipolar HVDC grid shown in Fig. 8 (a) was built on PSCAD/EMTDC platform. Table 3 shows the main circuit parameters. The widely used half-bridge modular multilevel converter (MMC) topology is used for the converters. In steady state, MMC-1 and MMC-2 are under constant active power control, and their reference values are 600 MW and 400 MW respectively. MMC-3 adopts constant dc voltage control with reference value of ± 320 kV. The overcurrent protection is used for the converters and DC lines. When any arm current exceeds the defined current threshold (2 pu in this paper), the converter will be blocked. When the DC line current exceeds the defined protection threshold (3.0 kA in this paper), tripping command will be sent to the DCB.

The 5SNA 3000K452300 IGBT module [44] is used for the LCSs and the MBs. The 5SDD 38H5000 [45] is used for the diodes. Each LCS is structured with 3 × 3 IGBT modules. Its current and voltage ratings are fulfilled by 2 × 2 IGBT modules. The rest of the IGBT modules are used as redundancy. The commutation time from the LCS to the MB is 0.25 ms [19]. The UFD is simulated as a resistor switch with 2 ms opening delay. Each diode stack in the type-2 improved scheme contains 154 diodes. The current limiting inductance is 80 mH. Fig. 8 (b) shows the positive direction of voltages and currents of DCB1 in positive pole.

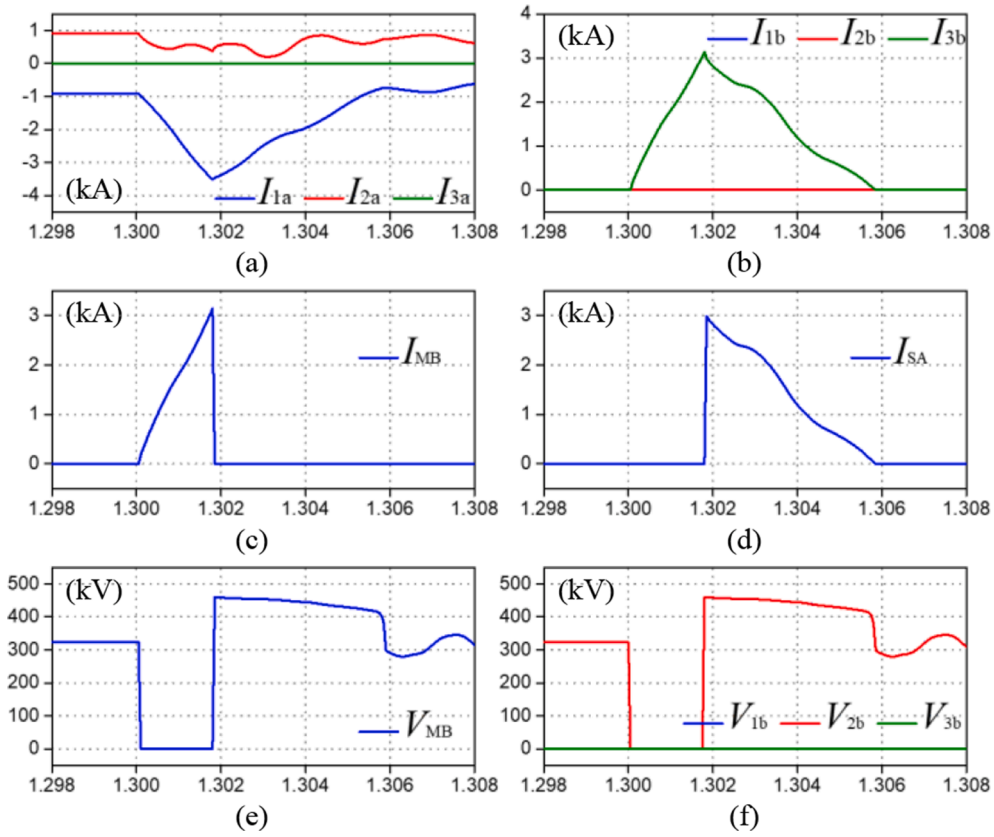

Fig. 15. Reclosing dynamic response of DCB1 under permanent DC fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of diode stacks.

7.2. Pole-to-ground fault

A low-impedance positive pole-to-ground fault (0.1 Ω) F_1 is placed at the terminal of DC line 13 near MMC-1 at time t = 1.0 s. Fig. 9 and Fig. 10 illustrates the response currents and voltages of DCB1 with the type-1 and type-2 DCB, respectively.

At time t = 1.0 s the grounding fault occurs and the DC currents increase rapidly. As soon as the line current exceeds 3.0 kA, the DCB is activated and the corresponding interruption strategy is applied.

From Fig. 9 and Fig. 10 we can see that peak currents flowing through the MBs of the two DCBs are 6.654 kA and 6.655 kA, respectively. As soon as the MB is turned off, I_{MB} reduces to zero quickly and I_{SA} increases correspondingly. The peak voltages on the MBs of different DCBs are 490.07 kV and 490.09 kV, respectively. Therefore, the performances of the two improved multiline DCBs are almost the same during pole-to-ground fault.

Fig. 11 shows the currents of three DC lines during pole-to-ground fault with the type-2 improved multiline DCB (the performance is similar with type-1 improved multiline DCB). When different DCBs are used, the power flows are almost the same. Fig. 11 (a) is the positive pole currents and Fig. 11 (b) is the negative pole currents. As shown in Fig. 11, the current of DC line 13 in positive pole increases quickly as soon as the grounding fault occurs. After the actions of the DCBs, DC currents restore to a stable state after violent oscillation of tens of milliseconds. Since the fault is a positive pole-to-ground fault, the performance of negative pole is not affected.

7.3. Pole-to-pole fault

A low-impedance pole-to-pole fault (0.1 Ω) F_2 is placed at the midpoint of DC line 12 at time t = 1.0 s. Fig. 12 and Fig. 13 depicts the dynamic performance of DCB1 with different DCB topologies. The response of DCB1 under pole-to-pole fault is similar to that under pole-to-ground fault.

For the type-1 improved multiline DCB, the peak current of MB is 5.285 kA, and the transient overvoltage of is 478.46 kV. For the type-2 improved multiline DCB, the peak current of MB is 5.284 kA, and the transient overvoltage of is 478.44 kV.

From Fig. 12 and Fig. 13 it is seen that the proposed two improved DCBs can clear pole-to-pole fault effectively, and their performances during DC faults are similar.

Fig. 14 shows the power flow of the system during pole-to-pole fault. Both positive pole and negative pole are affected due to the pole-to-pole fault. After the fault, DC line 12 is isolated and no current flows through it.

7.4. Reclosing

The reclosing processes are different for a permanent DC fault and a temporary DC fault. Both two reclosing processes are studied in this section. Assuming that the reclosing is applied after the pole-to-ground fault F_1. Only the type-2 improved multiline DCB is tested.

Fig. 15 shows the reclosing dynamic response of the DCB1 under permanent DC fault. The reclosing signal is received at time t = 1.3 s. Then the MB closes to reconnect DC line 13 to the HVDC grid. Because the fault still exists, the current flowing through the MB increases sharply again. The protection threshold value is set to 3.0 kA for this test system. The MB current reaches this protection threshold value after about 1.7 ms. Therefore the MB opens again and the current commutates to the arrester path. During this reclosing process, the currents and voltages of the DCB shown in Fig. 15 are smaller than those of the fault isolation process shown in Fig. 10.

Fig. 16 shows the reclosing dynamic response of the DCB1 under temporary DC fault. Similarly, the MB closes at time t = 1.3 s to

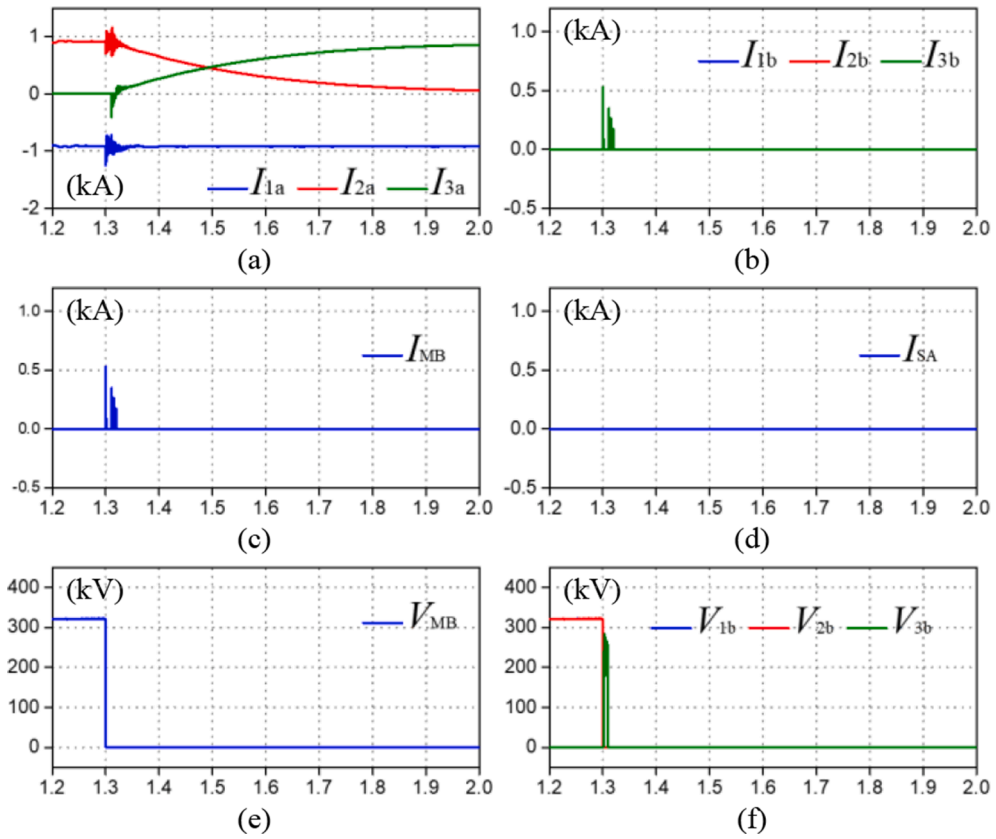

Fig. 16. Reclosing dynamic response of DCB1 under temporary DC fault. (a) Currents of upper conducting branches. (b) Currents of lower conducting branches. (c) MB current. (d) SA current. (e) MB voltage. (f) Voltages of diode stacks.

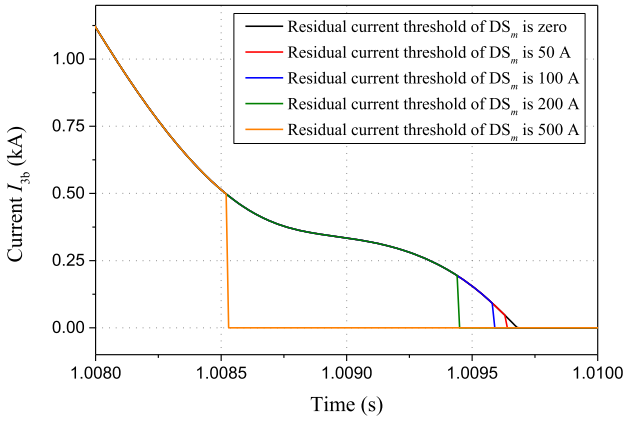

Fig. 17. Current I_{3b} with different residual current thresholds of DS$_m$.

reconnect DC line 13 to the HVDC grid. The required speed for reclosing is not as high as that for fault isolation. At time $t = 1.31$ s the UFD$_{3a}$ closes with zero current and zero voltage. At time $t = 1.32$ s the LCS$_{3a}$ is turned on so that DC current can flow through the upper conducting branch 3 to DC line 13. As shown in Fig. 16, DC current coming from MMC-1 is redistributed to DC line 12 and DC line 13 after the reclosing process of the DCB. After a time period the power flow of the HVDC grid returns to the pre-fault state.

8. Discussion

In order to investigate the impact of residual current threshold on DC fault clearing time, a case study is conducted for different residual current thresholds of DS$_m$ when the type-1 DCB is under pole-to-ground fault. Fig. 17 shows the waveforms of current I_{3b}. It can be seen that the current I_{3b} can be reduced to zero faster as the residual current threshold of DS$_m$ increases. This means that the DC fault clearing time is reduced with larger residual current threshold of DS$_m$. Specifically, if the DS$_m$ has a residual current threshold of 500 A, the DC fault clearing time is 1180 μs faster than the original case with zero residual current threshold.

9. Conclusion

Two improved multiline HVDC circuit breakers based on asymmetric conducting branches are proposed in this paper. The operation principle and reclosing process of the proposed DCBs are discussed. The economic efficiency and the reliability of these two DCBs are compared with other three DCBs. A model of a three-terminal bipolar HVDC grid is developed in PSCAD/EMTDC. Simulation results prove the validity and feasibility of the proposed schemes. The improved multiline DCBs have the following features:

1) For a converter with multiple adjacent DC lines, only one MB and SA are required in the improved DCBs. Besides, bidirectional breaking capability can be achieved by the unidirectional MB. This feature makes it very suitable for HVDC grid applications.
2) Compared with the other three DCBs, the proposed type-1 and type-2 DCBs use less power devices, which makes them more cost effective.
3) Among the five DCBs, the proposed type-2 DCB has the least individual switching actions during DC fault isolation process, which results in the highest operation reliability.

There will be more and more HVDC grids in the future. The proposed DCBs can bring great benefits to these applications.

CRediT authorship contribution statement

Huangqing Xiao: Conceptualization, Methodology, Writing – original draft. **Xiaowei Huang:** Software, Data curation. **Feng Xu:** Resources, Visualization, Investigation. **Leisi Dai:** Validation, Investigation. **Yongjun Zhang:** Writing – review & editing. **Zexiang Cai:** Writing – review & editing. **Yilu Liu:** Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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