

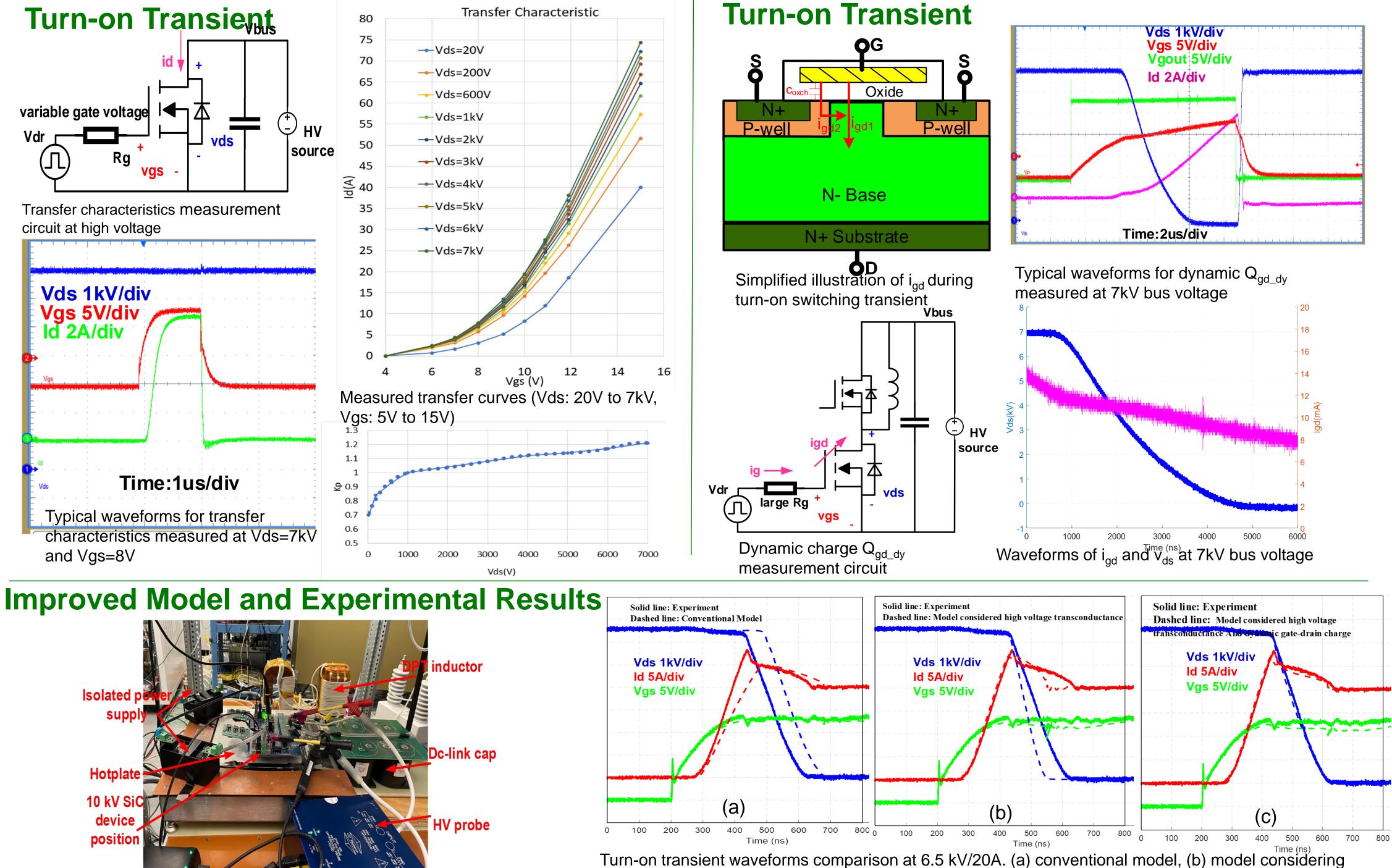
An Improved Turn-on Switching Transient Model of **10 kV SiC MOSFET**

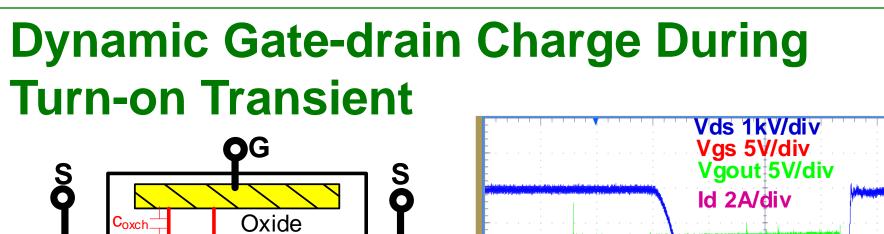
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Background

- The emerging 10 kV SiC MOSFET brings great benefit for medium and high voltage applications. Accurate switching transient modeling of the 10 kV SiC MOSFETs is critical for successful application.
- Conventional models based on curve tracer results fail to consider transconductance and dynamic gate charge during actual high voltage turn-on switching transient, and shows obvious discrepancies compared to experiments.
- Transconductance varies under different drain-source voltage due to SiC MOSFET short channel effect and drain induced barrier ۲ lowering effect. Dynamic gate-drain charge under MOSFET channel turn-on condition is different from static gate-drain charge when MOSFET channel is off.

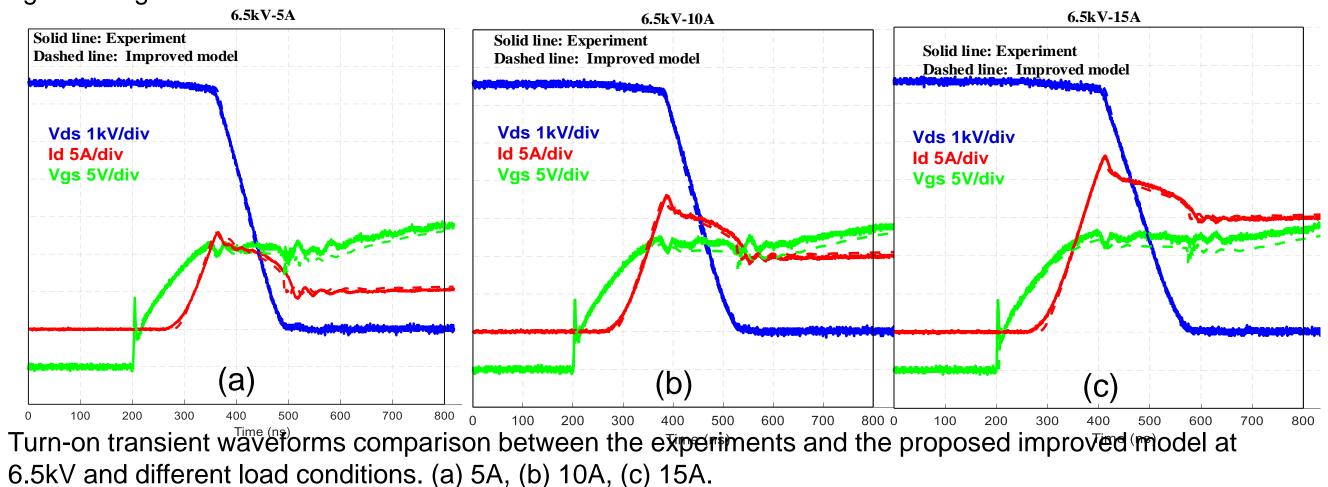
High Voltage Transconductance During





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	Parameters		Value		
	transconductance factor \mathbf{k}_{p}		$k_{p} = 0.7$		
	threshold voltage v _T		$v_T = 4.1V \ (25^{\circ}C)$		
	R _B		$380 \ m\Omega$		
	C _{gs}		6.3 <i>nF</i>		
			$C_{gdi} = 1000 \ pF, C_{gdb} = 50 \ pF$		οF
	parameters for C_{gd}		M = 1/3		
	parameters for C _{ds}		$C_{dsi} = 10 \ nF, C_{dsb} = 2.5 \ nF$ M = 1/2		F
Eon	(mJ)	5A	10A	15A	20A
Experiment		7.3	12.03	18.25	26.02
Proposed		7.23	11.85	17.87	25.46
Model		(-0.96%)	(-1.5%)	(-2.08%)	(-2.15%)
Conventional		7.1	12.38	19.75	30.49
Мо	del	(-1.78%)	(+2.91%)	(+8.22%)	(+17.18%)

high voltage transconductance, (c) model considering both high voltage transconductance and dynamic gate charge.



Conclusions

- An improved turn-on switching transient model of the 10kV SiC MOSFET which considers the high voltage transconductance and dynamic gate-drain charge during turn-on transient is proposed and experimentally verified.
- With the proposed model, both current rise stage and voltage fall stage waveforms during turn-on transient match well with that in the experiment. The loss error is within 5% over wide load conditions.



