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Switching Loss Reduction On Cascaded H-Bridge Converter With Diode Clamped Transformer Grounding Scheme

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***Abstract*—Parasitic capacitance of dc/dc transformers interfacing the cascaded H-Bridge (CHB) converter can introduce extra switching losses. A switching loss reduction method with diode clamped grounding for dc/dc transformers connecting CHB is proposed in this paper. The transformer grounding is connected to diode clamping circuit on the low voltage dc link to partially cancel the voltage charging/discharging the parasitic capacitances. Simulation and test have been demonstrated that the proposed method has reduced 53% of the parasitics induced loss and ~6% of the total converter loss in the setup with one simple diode half-bridge clamping circuit added on each converter cell.**

Keywords—cascaded H-bridge (CHB) converters, transformer, grounding, switching loss

I. Introduction

Power electronic devices and converters play an important role in modern power systems [1-3]. As medium voltage (MV) SiC devices and magnetics technology have brought benefit on medium voltage power conversion, high power and high voltage converters using isolated dc/dc with dc/ac stages are more and more popular for power grid applications [4-9]. For converter systems using isolated dc/dc converters, the parasitics may become a concern on interference and losses as the operating and insulation voltages increase [10-13]. One of the critical parasitics is the common-mode (CM) parasitic capacitance of the MV dc/dc transformers and inductors [14]. Due to safety and noise suppression concerns, the transformer electric shielding or metal case is usually grounded to the earth (see Fig. 1), which connects the CM capacitance from the transformer MV winding to the ground. In this case, the low voltage (LV) winding or the area near the MV winding may not see high electric field, yet the voltage of MV winding can charge and discharge the CM or grounding capacitance through the grounding loop. Current spikes can be induced by charging and discharging the dc/dc transformer parasitic capacitance, which can be seen in Fig. 2, causing not only insulation and EMI concerns, but also extra switching losses for CHB devices, which can account for over 15% of converter total loss [15]. Previous efforts have been made on CHB modulation to equivalent parasitics charging frequency, but the complex modulation can cause unbalanced switching losses on different devices [15]. The CM capacitance induced loss can also be limited by reducing the parasitics with different shielding strategies [16], but difficulties will be added on insulation design for the transformers and converters.

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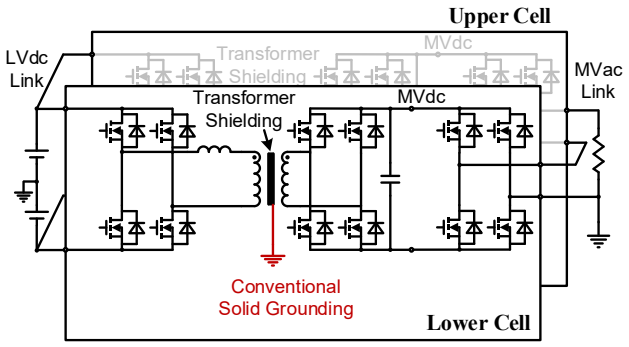

Fig. 1: Topology of converter using cells consisting of dc/dc and dc/ac, showing conventional transformer solid grounding.

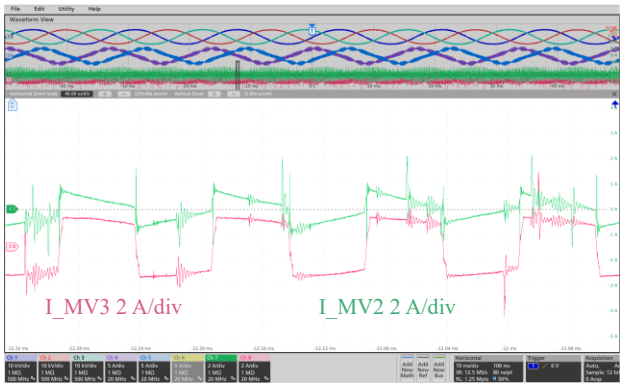

Fig. 2. Current spikes in transformers having high grounding capacitance [16].

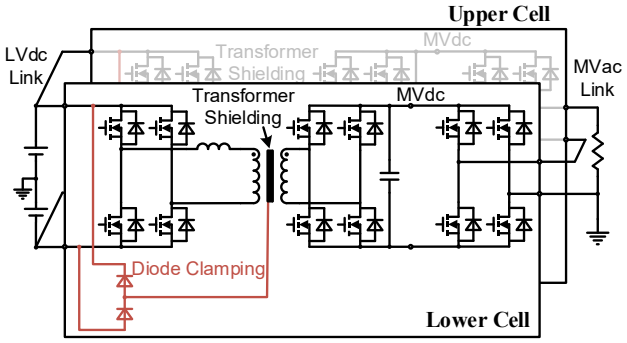

Fig. 3: Topology of converter using cells consisting of dc/dc and dc/ac, showing diode clamped transformer grounding.

In this paper, a diode clamped transformer grounding scheme is introduced to partially cancel the voltage stress across the transformer parasitic capacitance to the ground, and therefore, the losses caused by transformer capacitance can be reduced. Section II introduces the proposed grounding method. Simulation and test results are shown in Section III, along with discussions on influencing factors to the loss reduction. Section IV concludes the paper.

II. Proposed Diode Clamped Transformer Grounding

A. Topology with Diode Clamped Grounding Circuit

First, the proposed topology with diode clamped grounding is shown in Fig. 3. Unlike the conventional topology in Fig. 1, the transformer shielding is not directly connected to the earth. However, the shielding is connected to a diode half-bridge network, which is linked to the LV dc link. Therefore, the potential of the transformer shielding is not solidly tied to the ground, but has a partially floating potential, which can cancel the CM voltage imposed on the MV winding by the CHB converter modulation.

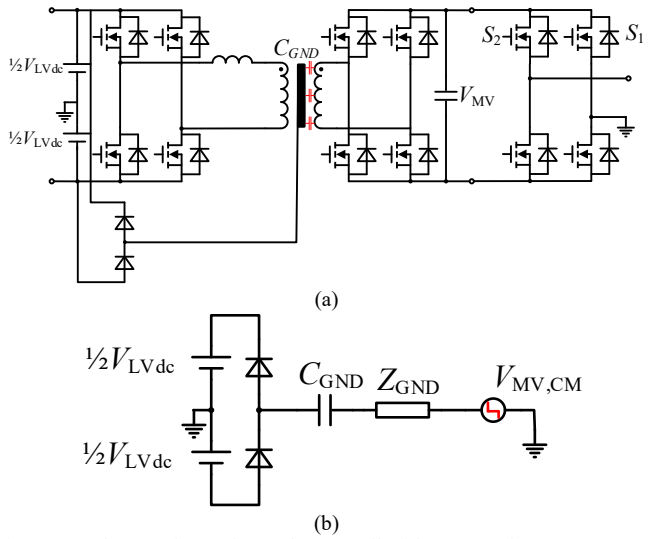

Fig. 4: Topology under study: (a) lowest cell with DAB and CHB converters using diode clamped circuit, (b) simplified CM loop.

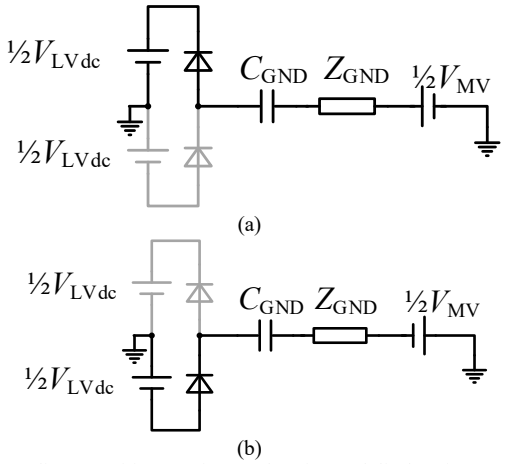

Fig. 5: Grounding parasitic capacitance charging and discharging modes with: (a) positive CM voltage, (b) negative CM voltage.

B. Operational Analysis of the Diode Grounding Circuit

As the MV dc/dc transformer is usually shielded between the LV and MV windings, only the MV side switching is studied. Also, with DAB converter acting with single phase-shift modulation, the DAB itself does not generate CM mode voltage. Therefore, the circuit loop concerning CM capacitance induced loss can be further simplified as the grounding CM capacitance directly connected to the CHB converter and diode clamping circuit, which is also grounded on the ac side, which is illustrated in Fig. 4.

Hence, the CM loop of CHB can be analyzed. As the CHB is grounded, for the lowest stage, the CM voltage of the MV dc side is

$$v_{MV,CM} = \frac{(1 - 2S_1)V_{MV}}{2} \tag{1}$$

where, S_1 is the switching function as in Fig. 4 [15]. From (1), the CM voltage of the MV dc side is flipping between half and negative half of the MV dc-link voltage. Therefore, as the CM voltage changes the polarity, the CM capacitance gets charged and discharged, through the diode clamping circuit. The two modes of the CM loop can be depicted as in Fig. 5.

From Fig. 6, as the CM voltage changes, the diode clamping circuit rectifies the charging/discharging current, causing voltage drop of half LV dc-link voltage on the circuit. Therefore, the voltage across the capacitance can be reduced by half of V_{LVdc}. Suppose the grounding impedance Z_{GND} is mainly resistive, the energy lost in the capacitance charging circuit is

$$E_{loss} = \frac{1}{2} C \Delta V^2 \tag{2}$$

Where, C is the grounding CM capacitance, ΔV the voltage change on the CM capacitance. For conventional solid grounded transformer, the total CM grounding induced loss for the lowest stage is [15]

$$P_{loss,solid} = C V_{MV}^2 f \tag{3}$$

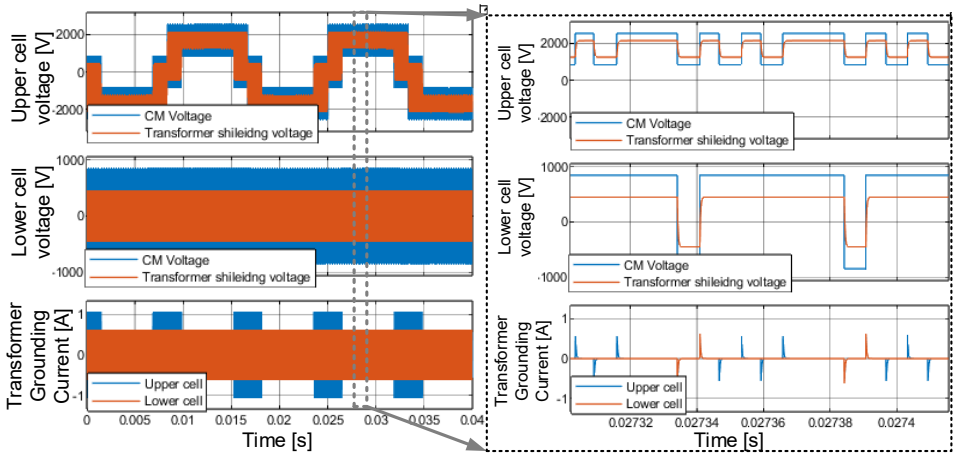

Fig. 6: Simulation results of diode clamped grounding, the transformer shielding potential swing for both upper and lower cell is reduced by half of LVdc link voltage (400 V).

Where, f is the equivalent switching frequency of the CHB converter. For the proposed diode clamping circuit, the loss can be reduced to

$$P_{loss,proposed} = C\Delta V^2 f = C(V_{MV} - V_{LVdc})^2 f \quad (4)$$

By subtracting (4) with (3), the loss reduction for the lowest stage is

$$\Delta P_{loss} = C[V_{MV}^2 - (V_{MV} - V_{LVdc})^2]f \quad (5)$$

Note that, the closer values V_{MV} and V_{LVdc} yield more effective loss reduction, and the analysis can be easily scale up to multiple cells cascaded by changing the switching frequency f to the sum of equivalent CM frequencies [15], and the Fig. 5 can also be valid with correct CM voltage levels.

III. Simulation and Test Validation

As the effectiveness of the diode clamping circuit has been analyzed, simulation and experimental tests have been performed to get the proposed grounding method validated.

A. Simulation Verification

First, the simulation of a two-stage CHB converter with DAB transformers, as shown in Fig. 1 and 3, has been performed. The LV and MV dc-links are set to 800 V and 1600 V, and the waveforms of CM voltage, voltages across CM capacitances and charging currents are shown in Fig. 6. As the CHB device switches, the transformer parasitics see the common mode (CM) voltage abstracted by ½LVdc voltage (400 V) as in Fig. 6.

B. Test Verification

Then, tests have been performed with the same rating of the simulation. The photographs of the MV dc/dc transformer and the diode clamping circuits are shown in Fig. 7. The test waveforms are shown in Fig. 8. From the waveforms, the shielding layer potential is not constantly zero, floating between the positive and negative of half LV dc link. The power loss with constant resistive load up to 12 kW is shown in Fig. 9. Loss reduction can be achieved constantly under variable output voltage by approximately 18 W, 53% of parasitic loss reduced (theoretically 34 W), and ~6% reduction on the total converter loss. Although the transformer potential swings (±½V_{LVdc}), the LV dc-link is typically below 1 kV and the margin on low

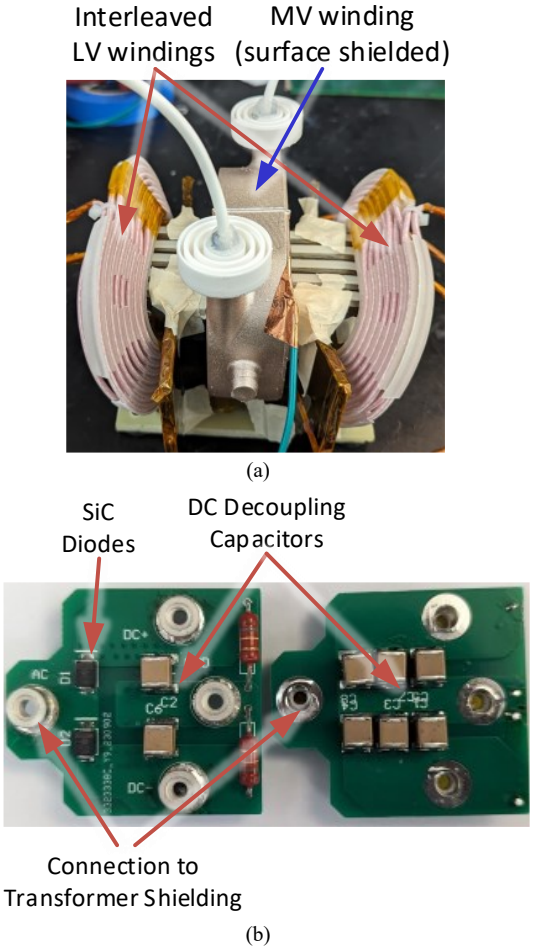

Fig. 7: Photography of (a) MV dc/dc transformer, (b) diode clamping circuit.

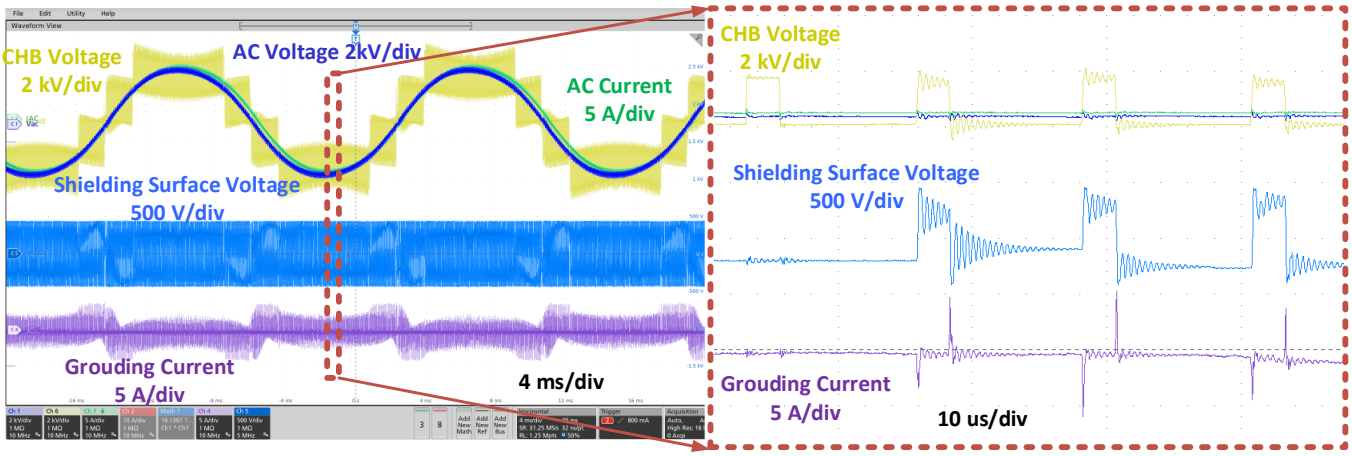

Fig. 8: Test waveforms for diode clamped grounding (with shielding voltage and grounding current for the upper cell).

voltage side insulation is usually high enough, so no further requirement on LV winding and power stage insulation is required.

C. *Impact Factors on Loss Reduction*

Since several different components can be found in the grounding loop, e.g., clamping diodes, grounding impedance, CHB devices, the effectiveness of the loss reduction can be influenced by multiple factors, too. The impact factors mainly include diode parasitics, grounding impedance, and modulation non-ideality, such as gate signal delays.

For the diodes, the non-idealities may cause extra conduction and switching losses. As the charging current is pulsating current with amplitude up to several amperes and short duration (<400 ns), and the diode forward voltage drop is also low compared to the CM voltage change, the conduction loss can be negligible. For the switching loss, as SiC Schottky diodes are used, no reverse recovery loss is assumed, while the charges built-up in the junction capacitance should be considered. As the CHB MV devices hard switch, the diode junction capacitance discharges and causes CHB device switching loss. The switching energy loss for each diode is

$$E_{loss,SBD} = \int C(v_r) v_r dv_r \tag{6}$$

where, the v_r is the diode reverse bias voltage during CHB device switching. As estimated during the test, the diode switching loss should be around 0.96 W.

The grounding parasitics can be complicated, which may be comprised of impedances of grounding wires, transformer shielding layer, and commutating loop of diode clamping boards. As the grounding loop should be low impedance required by the safety guidelines, only inductances are considered. To study the impact of total grounding impedance, a simulation sweep has been done to find out the loss variation on the grounding loop. Fig. 10 shows the loss results, from which the parasitic inductance increases from zero to 10 uH, while the loss is increased by 3 W. Hence, the inductance may impact the loss reduction, while as long as the grounding loop is controlled as short as possible, the loss impact is low.

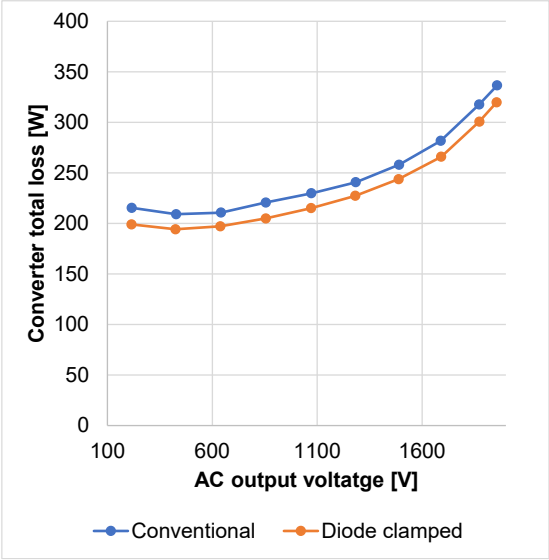

Fig. 9: Tested loss comparison between conventional and diode clamped grounding.

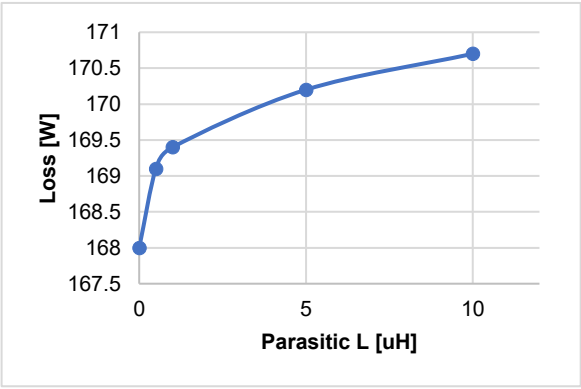

Fig. 10: Simulation sweep of grounding inductance and capacitance associated loss.

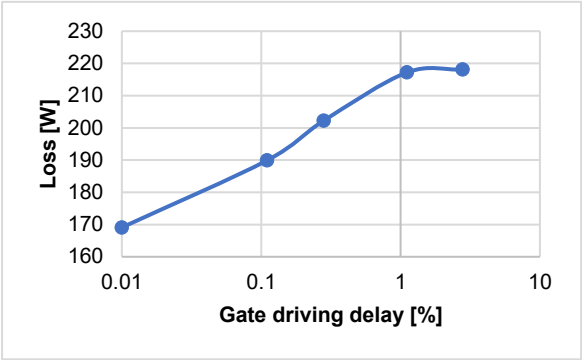

Fig. 11: Simulation sweep of gate driving delay and capacitance associated loss.

Modulation mismatches may cause mismatched CM voltages waveform, which can cause unexpected charging and discharging events on the CM capacitances. Fig. 11 shows the simulation sweep with gate driving delays. As shown in the figure, when gate driving delays up to 1% of the switching period, the loss can be increased by 30%, which can counterpart the proposed loss reduction. Therefore, the modulation and gate signaling may increase the CM capacitance induced loss, and the modulation delay and dead-time should be well managed.

IV. Conclusion

In this paper, a diode clamping circuit is proposed to reduce the CM parasitics induced switching loss on the CHB converters. The principle of loss reduction has been analyzed and validated through the simulation and test results. For the tested cases, the proposed method has reduced the parasitics associated loss up to 53%, which aligns with the analysis. The impact factors influencing the reduction effectiveness have also been discussed, among which the diode junction energy and gate signal delays may have high impact and should be carefully considered.

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This work made use of the shared facilities of the Engineering Research Centre Program of the National Science Foundation (NSF) and the Department of Energy under NSF Award no. EEC-1041877. The authors also would like to acknowledge the contribution of Southern Company and Powerex.

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