

Packaging a 100kW All-GaN-based Three-level Active Neutral Point Clamped Power Module for Electric Vehicle Motor Drives

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Abstract – This paper, to the best knowledge of the authors, for the first time reports the packaging of a 100kW three-level active neutral point clamped (3L-ANPC) phase leg power module for electric vehicle (EV) traction inverter applications using 650V/150A e-mode gallium nitride high-electron-mobility transistors (GaN HEMTs). Compared with two-level (2L) half bridge power module, the main challenges of packaging a 3L-ANPC phase leg power module are high number of switches (6 switches vs 2 switches) and multiple commutation loops (1 commutation loop vs 4 commutation loops). In addition, there are four switches involved in the two long commutation loops. Those parasitic loop inductances must be minimized simultaneously. Those challenges are addressed by meticulous packaging of the power module, featuring low power loop inductances, double-sided cooled power module, low junction-to-coolant thermal resistance, symmetrical layout for the two parallel dies of each switch and mechanical robustness, etc. The simulated loop inductances are 1.92nH for the short loops and 5.21nH for the long loops, respectively; resulting in a 471V and 540V of turn-off voltage spikes in a double pulse test simulation at 400V/200A. The simulated junction-to-coolant thermal resistances are 0.37°C/W and 0.53 °C/W for different switches, respectively.

Keywords—GaN packaging, 3L-ANPC, power module, double-sided cooling, EV traction inverter

I. INTRODUCTION

For next generation EVs, the power ratings of traction motors are increasing from tens of kW to hundreds of kW and the voltages of battery packs are also increasing from 400V to 800V, which call for EV traction inverters with a rated power of 100kW or higher at a DC bus voltage of 800V [1, 2]. Meanwhile, the targeted power density of the EV traction inverter listed by U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability) is increasing from 13.4 kW/L by 2020 to 33kW/L by 2025 [3], making GaN HEMT a promising candidate due to its fast switching speed and low switching loss that can result in smaller heatsinks and footprints, and smaller passives by switching at higher switching frequency [4].

Given that 650V GaN HEMTs are the mainstream choice, a 3L-ANPC topology for EV traction inverters is emerging, particularly for the 800V DC-bus voltage [2]. The efficiency comparison based on same Rds-on of each switch at room temperature of 3L-ANPC inverter and 2L 1200V SiC MOSFET are simulated by PLECS and given in Fig. 1. The 3L-ANPC inverter featuring two GaN System 650V/10mΩ dies in parallel for each switch, and 2L inverter featuring four Wolfspeed 1200V/21 mΩ SiC MOSFET. The main semiconductor specifications are listed in Table. I and Table. II, and the operating point details are listed in Table. III, respectively [5, 6]. Compared with the traditional 2L SiC

inverter, the minimized switching loss of GaN HEMTs combined with more voltage vector selections makes GaN-based 3L-ANPC inverters advantageous in terms of efficiency, particularly in the light and medium load since 95% of an typical EV driving cycle running at less than 30% of full load [2].

However, high voltage slew rate dv/dt and high current slew rate di/dt resulting from fast switching speed makes GaN HEMTs very sensitive to loop parasitic inductance [7]. Therefore, meticulous packaging design to reduce parasitic loop inductance is essential to fully exploit their benefits resulting from fast switching speed. The reported GaN HEMT power modules in literature are mainly focused on packaging 2L half bridge [8]. This paper, to the best knowledge of the authors, for the first time reports the packaging of 3L-ANPC phase leg power module based on 650V/150A GaN HEMT.

TABLE I. 650V/10mΩ GAN DIE SPECIFICATIONS

Parameter	Value	Test conditions
$R_{DS(on)}$	10mΩ	$V_{GS} = 6V$ $I_{DS} = 50A$ $T_j = 25^\circ C$
Q_G	33nC	$V_{GS} = 0 \text{ to } 6V$ $V_{DS} = 400V$
C_{OSS}	370pF	$V_{DS} = 400V$ $V_{GS} = 0V$ $f = 100kHz$

TABLE II. 1200V/21mΩ SiC MOSFET E3M0021120K SPECIFICATIONS

Parameter	Value	Test Conditions
$R_{DS(on)}$	21mΩ	$V_{GS} = 15V$ $I_{DS} = 62.1A$ $T_j = 25^\circ C$
Q_G	177nC	$V_{GS} = -4V \text{ to } 16V$ $V_{DS} = 800V$ $I_{DS} = 62.12A$
C_{OSS}	174pF	$V_{DS} = 0V \text{ to } 1000V$ $V_{GS} = 0V$ $V_{AC} = 25mV$ $f = 100kHz$

TABLE III. COMPARISON CONDITIONS

DC bus voltage	800V
Ambient temp.	85°C
Fundamental frequency	100Hz
Switching frequency	20kHz
RL load, power factor 0.85	
SiC junction to coolant thermal resistance $R_{J2C,SiC}$	0.5°C/W
GaN junction-to-coolant thermal resistance $R_{J2C,GaN}$	0.3°C/W
Modulation scheme	3L-ANPC: (NT-SVPWM, both 0-states are used.
	2L:7S-SVPWM

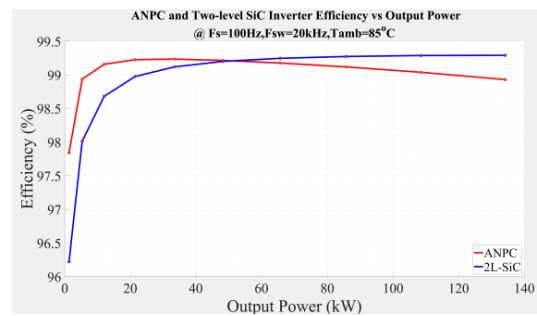


Fig. 1. All 650V GaN based 3L-ANPC and 1200V SiC MOSFET based 2L inverter efficiency vs output power

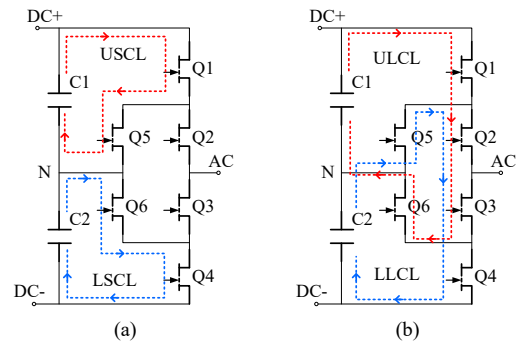


Fig. 2. Commutation loops of a 3L-ANPC phase leg with RL load (a) short commutation loops: upper arm short commutation loop (USCL) and lower arm short commutation loop (LSCL) (b) long commutation loops: upper arm long commutation loop (ULCL) and lower arm long commutation loop (LLCL)

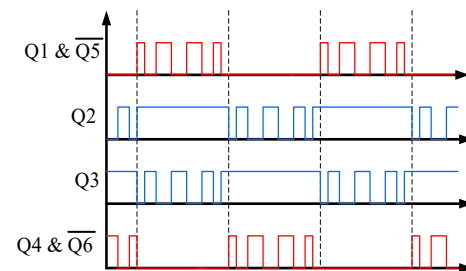


Fig. 3. Gate signals of a 3L-ANPC phase leg

II. CHALLENGES OF PACKAGING A 3L-ANPC INVERTER PHASE LEG

Generally, the loads of EV traction inverter are permanent magnet (PM) motors or induction motors with a lagging power factor around 0.8~0.9, and space vector pulse width modulation (SVPWM) are adopted for the inverter modulation. Thus, the inverter must be capable of 4-quadrant operation, yielding four commutation loops, as shown in Fig. 2, two short commutation loops and two long commutation loops [9]. Only two switches are involved in the two short commutation loops. However, four switches are involved in

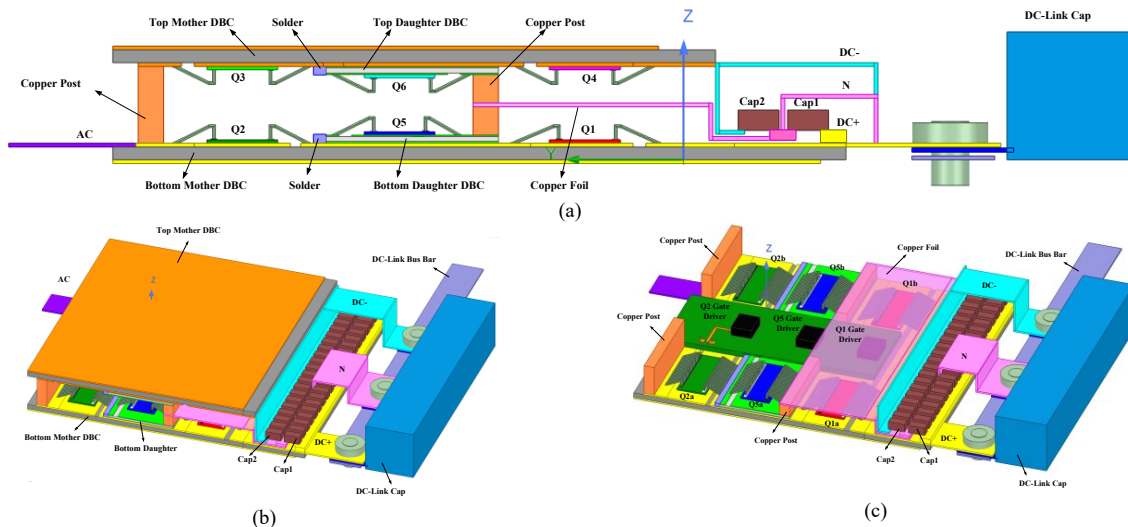


Fig. 4. All GaN based 3L-ANPC phase leg power module: (a) side view (b) upper arm layout (c) overall power module with bus bar and DC-Link capacitor

the two long commutation loops, which unavoidably increases the loop inductances. Those loop inductances must be reduced simultaneously.

Compared with the 2L half bridge power module, the high number of switches (6 switches vs 2 switches) in the 3L-ANPC phase leg is another main challenge. And three switches interconnected at one node complicates the layout design further. In addition, there are four terminals with an extra neutral terminal and two sets of decoupling capacitors. Furthermore, all the switches must be effectively cooled by attaching to a substrate. Meanwhile, other requirements such as symmetrical layout for parallel dies, minimized gate driving loop inductances, minimized magnetic and electric coupling between power loop and gate driving loop, etc., should also be considered. All of these factors make packaging a 3L-ANPC phase leg power module much more challenging than a 2L half bridge. The design challenges or design objects are summarized as follows:

- 1) High switch number.
- 2) Four commutation loops with simultaneously reduced loop inductances.
- 3) Low junction-to-coolant thermal resistance for all the switches.
- 4) Symmetrical layout of the parallel dies of each switch.
- 5) Minimized gate driving loop inductances.
- 6) Magnetically and electrically decoupled power loops and gate driving loops.
- 7) Compact design to improve power density.
- 8) Mechanically robust
- 9) Ease for mass production

III. POWER MODULE DESIGN AND SIMULATION

A. Structure Design.

In the proposed design, two mother direct bonded copper substrates (DBC) and two daughter DBCs are adopted to construct a 3L-ANPC phase leg power module, with each set

TABLE IV. DBC SPECIFICATIONS

	Material	Thickness
Mother DBC	Cu/AlN/Cu	0.3mm/1mm/0.3mm
Daughter DBC	Cu/AlN/Cu	0.127mm/0.381mm/0.127mm

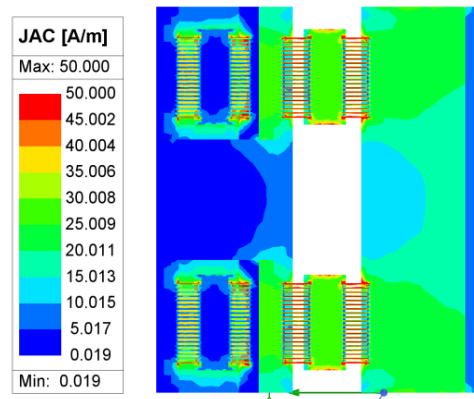


Fig. 5. Current distribution of short commutation loop at excitation voltage 400V and 100MHz. Current is almost evenly distributed among the two parallel dies.

of DBCs accommodating an arm of a phase leg and the neutral terminal sandwiched in the middle as shown in Fig. 4. In order to create another conducting layer to accommodate the interconnection of three dies, the daughter DBCs are attached to the mother DBCs with one edge of the daughter DBC connected to the mother DBC. The switches Q1, Q2, Q3 and Q4 are attached to the two mother DBCs, while the neutral switches Q5 and Q6 are attached to the two daughter DBCs, respectively. The daughter DBCs only serve for die attachment and sitting the wire bonding points. Hence, a thinner DBC can be used. The properties of the mother DBC and daughter DBCs are listed in Table IV, respectively.

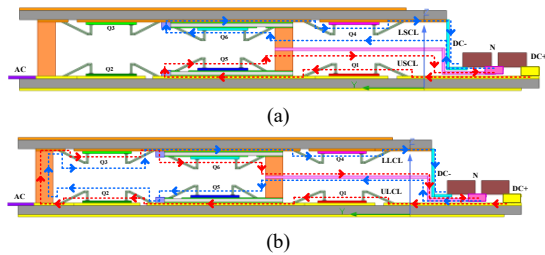


Fig. 6. Commutation loops (a) short commutation loops. red: upper arm, blue: lower arm; (b) long commutation loops. red: upper arm, blue: lower arm.

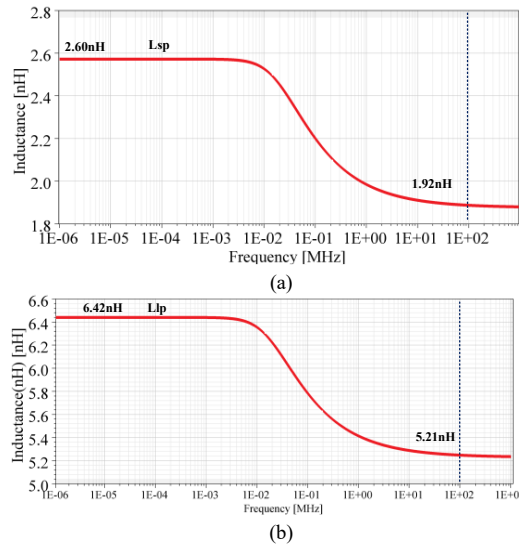


Fig. 7. Simulated power loop inductance by ANSYS Q3D (a) the short commutation loops inductance (b) the long commutation loops

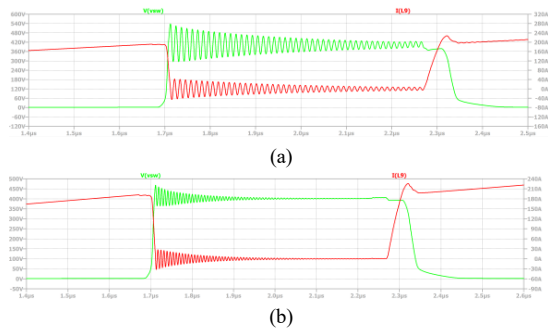


Fig. 8. Double pulse test simulation for the long loop: $V_{dc}=400V$, $I_d = 200A$, $R_{gon}=10\Omega$, $R_{goff}=2\Omega$

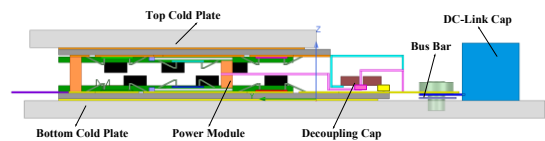


Fig. 9. Assembly of power module with cold plates

Given the high current of a traction inverter and relatively small copper thickness of PCBs, PCBs are avoided in the power loop design.

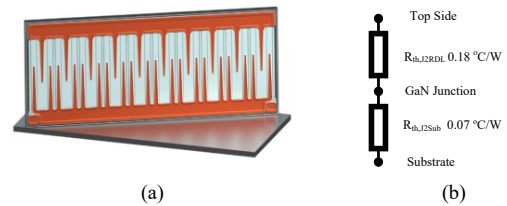


Fig. 10. (a) GaN System 650V E-mode GaN die GS-065-150-1-D (b) Thermal network model

Two long copper posts are used to connect the top mother DBC (lower arm) and bottom mother DBC (upper arm), and four short copper posts are used to connect the two neutral switches to the neutral terminal. They also provide the mechanical support and withstand the mechanical stresses from the top and bottom cold plates. Distributed terminals with a thin layer of Kapton coating are adopted. Two sets of decoupling capacitors are placed on those wide terminals. Besides connecting the power module and DC-Link capacitor, they also serve to (a) accommodate the decoupling capacitors, (b) evenly distribute the current among the two parallel dies in steady state (fundamental frequency) and during fast transient commutation period as shown in Fig. 5., (c) cool the decoupling capacitors, and (d) provide mechanical support on the DC-Link side.

B. Loop Inductance.

The two short commutation loops and two long commutation loops are marked in Fig. 6 (a) and (b), respectively. Flux cancelling is one of effective methods to reduce the loop inductance [10]. By maximizing the negative mutual inductance, the total loop inductance is minimized. In the proposed design, the forward current paths and the backward current paths of both the short and long commutation loops are fully overlapped, so that the magnetic flux can be canceled to the maximum extent. By ANSYS Q3D simulation, the loop inductances are still very low: 1.92nH and 5.21nH at 100MHz for the short commutation loops and long commutation loops, respectively. If wire-bonding connection are replaced by copper foil connection, the distance between the two mother DBCs and the distance between the neutral terminal and mother DBCs can be further shortened. Consequently, the loop inductances can be further reduced. Double pulse test (DPT) simulation is then carried out by LTSpice. As shown in Fig. 8, the maximum V_{ds} is 540V for the long commutation loops and 471V for the short commutation loops at a 400V DC bus voltage and 200A switch current, representing 135% and 118% of the DC bus voltage, respectively. This maximum voltage is in the safe operating region of the 650V devices.

C. Thermal Performance.

The power module is sandwiched between two cold plates and double-sided cooled as illustrated in Fig. 9. The thermal network model of the used GaN die is given in Fig. 10, the junction-to-substrate thermal resistance and junction-to-top side thermal resistance are 0.07°C/W and 0.18°C/W . Due to the small contact area between the bond wires and the

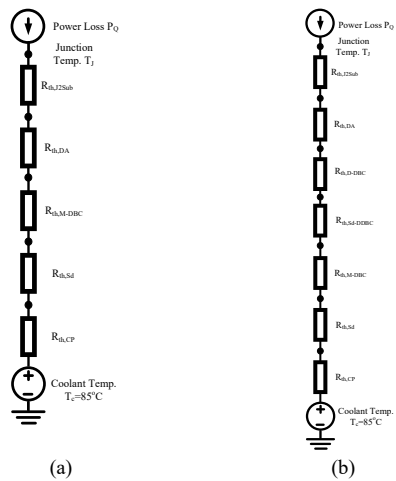


Fig. 11. (a) Thermal network model of Q1, Q2, Q3 and Q4 (b) thermal network model of Q5 and Q6. $R_{th,J2Sub}$, $R_{th,DA}$, $R_{th,M-DBC}$, $R_{th,D-DBC}$, $R_{th,Sd}$, $R_{th,CP}$ are thermal resistance of GaN die junction-to-substrate, die attachment layer, mother DBC, daughter DBC, solder layer and cold plate, respectively.

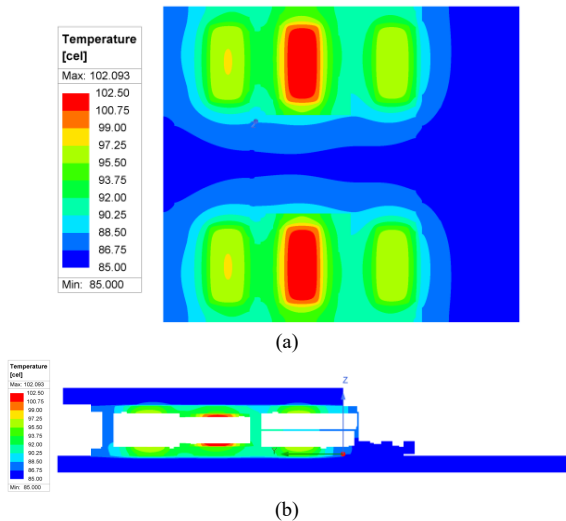


Fig. 12. Simulated power module temperature map (a) temperature map of lower mother DBC (b) temperature map of cross section of power module

die, little heat is conducted to the DBC by the bond wires. The heat is mainly dissipated through the substrate side. The junction-to-coolant thermal network model of Q1~Q4 and Q5~Q6 are given in Fig.11 (a) and (b), respectively. The die attachment layer, even very thin, can contribute significant portion of the total thermal resistance [11]. The temperature map simulated by ANSYS Icepak with 35W per die, copper cold plate thickness 5mm and constant coolant temperature at 85°C is shown in Fig. 12. The maximum junction temperatures of Q1~Q4 and Q5~Q6 are 97.9°C and 103.5°C, respectively. The simulated junction to coolant thermal resistance for Q1~Q4 and Q5, Q6 are 0.37°C/W and

0.53°C/W respectively, including an inserted 0.13°C/W die attachment layer thermal resistance [12]. The daughter DCBs introduce some extra thermal resistance, which lead to the higher junction temperature of Q5 and Q6 than that of Q1~Q4. Another benefit of the power module structure is that, even though the decoupling capacitor and DC-Link capacitor are not included in the thermal model, those capacitors can also be effectively cooled, too.

IV. CONCLUSIONS

In this paper, a 3L-ANPC phase leg power module based on GaN System E-mode 650V/10mΩ bare dies with double-sided cooling, low loop inductances and low thermal resistances and mechanical robustness is proposed for EV traction inverter applications. First, the challenges of packaging a 3L-ANPC phase leg power module are pointed out, followed by a detailed description of the proposed power module structure. Those challenges are well addressed by the proposed structure. The simulated loop inductances of the long loops and short loops are 5.21nH and 1.92nH, respectively; and the simulated the turn-off voltage spike are 540V and 471V, respectively. They are within safe operating range the 650V devices. The simulated junction-to-coolant thermal resistance are different at 0.37°C/W and 0.53°C/W for Q1~Q4 and Q5, Q6 switches, respectively. Prototyping and experimental testing will be conducted in the future work. This uneven thermal resistance will also be addressed in the future work.

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