Desat Protection With Ultrafast Response for High-Voltage SiC MOSFETs With High $dv/dt$

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ABSTRACT This article presents a desat protection scheme with the ultrafast response for high-voltage (>3.3 kV) SiC MOSFETs. Its working principle is the same as the conventional desat protection designed for high-voltage SiC MOSFETs, yet its blanking time is implemented by fully considering the influence of high negative $dv/dt$ during the fast turn-ON transient. With the same circuitry as the conventional desat protection, the proposed protection scheme can significantly shorten the response time of the desat protection when it is used to protect high-voltage SiC MOSFETs. In addition, the proposed protection scheme with ultrafast response features strong noise immunity, low-cost, and simple implementation. By taking advantage of the high $dv/dt$ during the normal turn-ON transients, the proposed protection scheme can be even faster when the MOSFET has a faster switching speed. Design details and the response speed analysis under various short circuit faults are presented in detail. A half bridge phase leg based on discrete 10 kV/20 A SiC MOSFETs is built to demonstrate the proposed protection scheme. Experimental results at 6.5 kV validate the ultrafast response (115 ns response time under a hard switching fault, 155 ns response time under a fault under load), and strong noise immunity of the proposed desat protection scheme.

INDEX TERMS High-voltage SiC MOSFETs, desat protection, ultrafast response, high $dv/dt$, noise immunity.

I. INTRODUCTION

Medium voltage (MV) converters play an indispensable role in numerous critical applications, such as MV motor drives and grid interface converters to make the grid more stable and resilient [1], [2], [3], [4]. Breakthrough performance in MV converters is expected in the near future because of the rapid development of high voltage (>3.3 kV) SiC MOSFETs with superior device performance for power electronics applications [5], [6], [7], [8], [9], [10], [11]. Compared to Si IGBTs prevalent in MV converters nowadays, high voltage SiC MOSFETs possess higher blocking voltage, faster switching transients, and lower switching loss, and hence the capability to operate with $>10\times$ higher switching frequency [6], [11], [12], [13], [14]. These device-level benefits further facilitate MV converters with higher power density, efficiency, and control bandwidth, and thus are promising to significantly expand the capabilities and applications of MV converters [5], [6], [7], [8], [9], [10], [15], [16], [17].

To make full use of the comprehensive benefits of high voltage SiC MOSFETs, numerous challenges should be tackled, especially overcurrent/short circuit protection. Typically, an attractive solution for overcurrent/short circuit protection is required to have fast response, simple and low-cost implementation, and high noise immunity simultaneously.

Compared to Si IGBTs in MV applications, it is more challenging to design the overcurrent/short circuit protection for high voltage SiC MOSFETs. High voltage SiC MOSFETs have smaller dies, higher current density, and lower thermal capacitance, and hence shorter short circuit withstand time [12], [18], [19]. Detailed thermal impact of short circuit
response time and energy loss has been presented in [18] with the focus on 10 kV SiC MOSFETs. The die temperature rises rapidly to \( \sim 500 \degree C \) within 1.2 \( \mu s \) as the short-circuit continues, which emphasizes the importance of short response time to protect high voltage SiC MOSFETs [18].

Moreover, faced with PWM voltage with higher magnitude, switching frequency, and \( \frac{dv}{dt} \), high voltage SiC MOSFETs are more likely to undergo a flashover fault, the worst type of short circuit fault caused by the insulation failure in MV converters [20], [21], [22], [23]. A flashover fault generates extremely fast transients with much higher \( \frac{di}{dt}, \frac{dv}{dt}, \frac{ds}{dt} \), and short-circuit energy than the two conventional short-circuit faults, including hard switching fault (HSF), and fault under load (FUL) [18], [22], [23], [24]. Therefore, a flashover fault requires short-circuit protection to have an even shorter response time in order to safely turn OFF the MOSFET and clear the fault [22], [23]. Meanwhile, the high blocking voltage and the noise resulting from high \( \frac{dv}{dt} \) with long duration make it difficult to achieve a protection scheme with high noise immunity and simple implementation for high-voltage SiC MOSFETs [25].

So far, the proposed overcurrent/short circuit protection methods for high-voltage SiC MOSFETs still have trouble achieving strong noise immunity, simple and low-cost implementation, and fast response at the same time. The protection method based on the current transformer requires complicated implementation when it is applied to protect high-voltage SiC MOSFET modules with one or several half bridge phase legs [23]. The reason is that high-voltage insulation design is needed in the current transformer measuring the current of the upper MOSFET in the phase leg. The method based on Rogowski coil current sensor features fast response, yet it requires a high-cost and complicated Rogowski coil design to achieve high accuracy and noise immunity [26], [27], [28].

The conventional desat protection scheme features simple implementation and high noise immunity with its noise immunity studied comprehensively [25], [29], yet its response time is limited by the blanking time requirement, which makes it less desirable for some high-voltage SiC MOSFETs requiring faster response for lower short-circuit current [29], [30], [31], [32], [33], [34]. In summary, a more thorough investigation is necessary in order to achieve a better tradeoff regarding the three factors in the protection scheme for high voltage SiC MOSFETs: response time, cost, and complexity of implementation, and noise immunity.

This article focuses on a proposed desat protection scheme with ultrafast response, which aims to achieve high noise immunity, simple implementation, and ultrafast response simultaneously. This article is an extension of part of the work in [35]. Section II provides an overview of the conventional desat protection design for high-voltage SiC MOSFETs. Section III introduces the working principles of the proposed desat protection scheme and how it can achieve ultrafast protection response. Section IV discusses the design details of the proposed protection scheme for the 10 kV/20 A SiC MOSFETs, whose ultrafast response and strong noise immunity are validated by the experimental results in Section V. Section VI discusses the advantages and limitations of the proposed protection scheme, followed by conclusions in Section VII.

II. OVERVIEW OF DESAT PROTECTION

Desat protection for high-voltage SiC MOSFETs can be implemented with the circuitry composed of discrete components or the circuitry based on an advanced gate driver IC with integrated desat protection function, as shown in Fig. 1 [30], [31], [32], [33], [34], [35]. The implementation with a gate driver IC in Fig. 1(a) supports a more compact and simpler solution, but its threshold voltage is usually lower than 10 V, which is not high enough to support a reasonable threshold current for some high-voltage SiC MOSFETs [30], [36]. Meanwhile, the desat protection circuitry based on discrete components is more flexible. Numerous parameters can be tuned to achieve a desirable threshold current and response time for various high-voltage SiC MOSFETs, although such implementation requires more components [25]. In both implementations, the desat protection only requires off-the-shelf components without any custom design. In both implementations, a clamping diode \( D_{blk} \) is often added to protect the desat comparator from overvoltage and ensure its proper operation.

The blanking time is essential in desat protection to prevent the false triggering during the turn-ON transient of the MOSFET [32]. Usually, it is assumed that \( V_{desat} \) will be dominated by the capacitive charging process during the blanking time. Take the desat protection circuitry in Fig. 1(b) for example;
based on this assumption, the waveform of $V_{\text{desat}}$ is drawn in Fig. 2. After the rising edge of $V_g$, $V_{\text{desat}}$ will still be clamped at $V_{\text{clamp}}$ for a time interval $t_{\text{cla}}$ since it takes time to turn OFF $M_{\text{cla}}$. $t_{\text{cla}}$ can be adjusted by tuning $R_{\text{goff,cla}}$, the turn-OFF gate resistance of $M_{\text{cla}}$ in Fig. 1(b). After $M_{\text{cla}}$ is fully turned OFF, $V_{\text{desat}}$ will keep increasing as the charging process goes on. The length of blanking time $t_{\text{blk}}$ can be expressed as follows:

$$t_{\text{blk}} = t_{\text{cla}} + t_{\text{RC}}$$  \hspace{1cm} (1)

In the equation, $t_{\text{RC}}$ is the time interval in which $V_{\text{desat}}$ rises from $V_{\text{clamp}}$ to the protection threshold voltage $V_{\text{desat,th}}$ as a result of R-C charging process. To avoid false triggering during the blanking time, the conventional desat protection possesses a R-C network with a large time constant so that $V_{\text{desat}}$ is always lower than $V_{\text{desat,th}}$ during the blanking time [32].

### III. WORKING PRINCIPLES

One advantage of the proposed desat protection scheme with ultrafast response is that it has the same circuitry as the conventional desat protection. In this article, to introduce the proposed scheme, as an example, it is applied to protect the discrete 10 kV/20 A SiC MOSFETs from Wolfspeed [12], [35]. Fig. 3 shows the detailed circuit diagram of the proposed desat protection with ultrafast response for the 10 kV/20 A SiC MOSFETs, the same as the conventional desat protection based on discrete components designed for high voltage SiC MOSFETs in Fig. 1(b).

#### A. IMPACT OF $dv/dt$ ON BLANKING TIME

When designing the desat protection for high-voltage SiC MOSFETs with fast turn-OFF transients and high $dv_{ds}/dt$, it is not correct to assume that $V_{\text{desat}}$ behaves like Fig. 2 during the blanking time. Normal switching transients of high-voltage SiC MOSFETs feature much higher $dv/dt$ than Si IGBTs for which desat protection was originally designed. High-voltage SiC MOSFETs can easily generate $>30$ V/ns $dv/dt$ during normal switching transients, even higher than 100 V/ns in some cases, while $dv/dt$ generated by Si IGBTs is usually less than 10 V/ns, including 6.5 kV Si IGBTs [6], [7], [8]. The effect of high $dv_{ds}/dt$ during the fast turn-OFF transients has not been considered in Fig. 2, which also plays a critical part in shaping $V_{\text{desat}}$ via the parasitic capacitance $C_{\text{desat}}$ caused by the desat diode $D_{\text{desat}}$.

To make it clear, $dv_{ds}/dt$ is defined as positive if the drain-to-source voltage $V_{ds}$ increases. Meanwhile, $dv_{ds}/dt$ is negative if $V_{ds}$ decreases. The high $dv_{ds}/dt$ during the normal turn-OFF transient is hence negative and generates the displacement current that should be sourced by the desat protection circuitry as displayed in Fig. 3. As a result, $V_{\text{desat}}$ will be heavily shaped by high negative $dv_{ds}/dt$ during the blanking time [35].

The normal turn-OFF transients of high voltage SiC MOSFETs have high $dv/dt$ for low switching loss and hence draws a large displacement current $C_{\text{desat}}dv_{ds}/dt$. Typically, the current provided by $V_{cc}$ is too low to supply the required displacement current. Once high $dv/dt$ is generated during the normal turn-OFF transients, $V_{\text{desat}}$ will reach a peak $V_{\text{desat},M}$ and start decreasing as $C_{\text{blk}}$ is discharged to provide $C_{\text{desat}}dv_{ds}/dt$, as shown in Fig. 4. Since $C_{\text{blk}}$ is small with limited stored charge, $C_{\text{blk}}$ will be discharged quickly, and the diode $D_{\text{blk}}$ will be forward biased to clamp $V_{\text{desat}}$ until the voltage fall time with high $dv/dt$ ends. As seen in Fig. 4, at the end of the voltage fall time $t_{\text{fall}}$, $V_{\text{desat}}$ is reset to $V_{\text{clamp}}$ (forward voltage drop of $D_{\text{blk}}$ neglected), before it rises again due to current from $V_{cc}$. The real blanking time after considering the effect of high $dv/dt$ is

$$t_{\text{blk}} = t_{\text{cla}} + t_{\text{m}} + t_{\text{fall}} + t_{\text{RC}}$$  \hspace{1cm} (2)
time is the voltage fall time of the drain-to-source voltage \( V_{ds} \) during the normal turn-on transients. \( t_m \) is the time interval between the end point of \( t_{cla} \) and the starting point of \( t_{fall} \).

In fact, \( V_{desat} \) will not necessarily start rising immediately after the high negative \( dv/dt \) disappears. If \( D_{blk} \) is a clamping diode with p-n junction, \( V_{desat} \) will still be clamped until the reverse recovery process is over. Also, the body diode of the MOSFET \( M_{cla} \) has a reverse recovery effect. As shown in Fig. 5, the real blanking time after considering high \( dv/dt \) will be even longer because of the reverse recovery effect

\[
t_{blk} = t_{cla} + t_m + t_{fall} + t_{rr} + t_{RC}.
\]

In the equation, \( t_{rr} \) is the reverse recovery time during which \( V_{desat} \) will still be clamped at \( V_{clamp} \). The reverse recovery process can be eliminated by selecting a Schottky diode as \( D_{blk} \) and a bipolar junction transistor as \( M_{cla} \).

**B. ANALYSIS OF WORKING PRINCIPLES**

Since the real blanking time of desat protection can be effectively prolonged by the high \( dv/dt \) and the reverse recovery process, an R-C network with a much smaller time constant can be designed to realize the desat protection with ultrafast response without false triggering issue during the normal turn-on transients. To achieve the desat protection scheme with the ultrafast response, \( R_{blk} \) and \( C_{blk} \) are selected so that \( V_{desat} \) will continue to decrease and later be clamped during the voltage fall time with high \( dv/dt \). A Si clamping diode with a p-n junction and a Si MOSFET are selected to serve as \( D_{blk} \) and \( M_{cla} \), respectively, in order to take advantage of the reverse recovery effect for longer blanking time.

During the voltage fall time with high negative \( dv/dt \), \( V_{desat}(t) \) can be analyzed with the superposition theorem. To simplify the analysis, a constant \( dv/dt \) is assumed during the voltage fall time of \( V_{ds} \). \( R_{damp} \) is also neglected because it is much smaller than \( R_{blk} \). Also, the nonlinear parasitic capacitance \( C_{desat} \) of the desat diode is modeled with its charge-equivalent linear capacitance [37]. After considering the constant dc voltage source \( V_{cc} \) and the constant dc current source \( C_{desat} \frac{dv}{dt} \), \( V_{desat} \) in \( s \) domain is expressed as

\[
V_{desat}(s) = \left( \frac{V_{cc} - V_{clamp}}{R_{blk}} + C_{desat} \frac{dv}{dt} \right) \frac{R_{blk,eq}}{1 + sC_{desat,eq}R_{blk,eq}} + V_{clamp}.
\]

\( R_{blk,eq} = R_{blk} / (R_{dI} + R_{ds}) \) is the parallel resistance of \( R_{blk} \) and the voltage divider impedance. Then, during the voltage fall time, \( V_{desat} \) in the time domain can be solved as follows:

\[
V_{desat}(t) = V_{desat,inf} + \left[ V_{desat,M} - V_{desat,inf} \right] e^{\frac{-t}{t_{blk,eq}}}.
\]

\( V_{desat,M} \) is the value of \( V_{desat} \) at the starting point of the voltage fall time. Also, the \( dv/dt \) is negative during the voltage fall time. \( V_{desat,inf} \) is the final value of \( V_{desat} \) if the voltage fall time is infinitely long, and it can be expressed as

\[
V_{desat,inf} = (V_{cc} - V_{clamp}) \frac{R_{blk,eq}}{R_{blk}} + C_{desat} \frac{dv}{dt} R_{blk,eq} + V_{clamp}.
\]

To ensure that \( V_{desat} \) can be clamped at \( V_{clamp} \), the fundamental requirement is that \( V_{desat,inf} \) should be lower than \( V_{clamp} \). The requirement can be rewritten as

\[
R_{blk} > \frac{V_{clamp} - V_{cc}}{C_{desat} \frac{dv}{dt}}.
\]

If \( R_{blk} \) cannot satisfy the requirement, \( V_{desat} \) will never drop to a voltage level lower than \( V_{clamp} \). \( C_{blk} \) only influences how quickly \( V_{desat} \) drops. Also, the higher the negative \( dv/dt \) becomes, the more quickly \( V_{desat} \) can drop during the voltage fall time, which also means \( V_{desat} \) can drop to \( V_{clamp} \) more easily.

Similar analysis can be conducted for the desat protection realized with an advanced gate driver IC shown in Fig. 1(a). If the displacement current flowing through \( C_{desat} \) is sufficiently large due to high \( dv/dt \), \( V_{desat} \) will keep dropping and finally be clamped by \( D_{blk} \). The real blanking time can be much longer due to the high \( dv/dt \) and the reverse recovery of \( D_{blk} \). In order to ensure that \( V_{desat} \) can be clamped by \( D_{blk} \) during the voltage fall time with high \( dv/dt \), the requirement is expressed as

\[
\left( C_{desat} \frac{dv}{dt} - I_{cc} \right) t_{fall} > C_{blk}(V_{desat,M} - V_{clamp}).
\]

Therefore, a smaller \( C_{blk} \) can be adopted to hasten the protection response significantly. It is not necessary to select \( C_{blk} \) based on the traditional blanking time requirement in desat protection, which does not consider the influence of high negative \( dv/dt \) on \( V_{desat} \) [32]. In fact, the smaller \( C_{blk} \), the more quickly \( V_{desat} \) will drop to \( V_{clamp} \) during the voltage fall time.

**IV. DESIGN DETAILS**

In this section, design details of the desat protection with ultrafast protection will be covered for 10 kV/20 A discrete SiC MOSFETs [12], [35]. A Si clamping diode with p-n junction is installed as \( D_{blk} \), and a Si MOSFET is installed as \( M_{cla} \). Together, they contribute to a reverse recovery time \( t_{rr} \) of 370 ns, as shown in the waveform of \( V_{desat} \) in Fig. 6.
The experimental waveform of $V_{\text{desat}}$ in Fig. 6 is obtained during the ac–dc continuous power test of the half-bridge phase leg based on 10 kV/20 A SiC MOSFETs at 6 kV. The phase leg is configured as a half-bridge inverter, and details are introduced in [38]. After high negative $dv/dt$ is generated, $V_{\text{desat}}$ is clamped by the diode $D_{\text{blk}}$ at a voltage level slightly lower than $-5\text{ V}$ $V_{\text{clamp}}$ for 500 ns, with a $t_{\text{rr}}$ of 370 ns (definition of $t_{\text{rr}}$ shown in Fig. 5). Under the same test after removing $D_{\text{blk}}$, the period during which $V_{\text{desat}}$ is clamped after the voltage fall time is reduced by 210 ns, as displayed in Fig. 7. It is hence proved that the clamping diode $D_{\text{blk}}$ plays a major role in clamping $V_{\text{desat}}$ with its reverse recovery process. As clearly presented in Fig. 7, after removing the clamping diode $D_{\text{blk}}$, $t_{\text{rr}}$ is reduced to 160 ns, which is attributed to the reverse recovery process of the body diode of Si MOSFET $M_{\text{cla}}$ (part number: BSS138). Generally, the experimental waveforms in Figs. 6 and 7 validate the analysis about the impact of negative $dv/dt$ and reverse recovery effect on $V_{\text{desat}}$ during the blanking time in Fig. 5.

Because of the installation of $D_{\text{blk}}$, a considerable $t_{\text{rr}}$ of 370 ns is achieved. Therefore, according to (3), designing an R-C network with a much smaller time constant can still result in the effective blanking time longer than 550 ns, which is required based on the switching characteristics of the 10 kV/20 A SiC MOSFET [35], [38].

### A. DESIGN DETAILS OF $R_{\text{BLK}}$

When designing the R-C network, the primary consideration is that $V_{\text{desat}}$ can drop rapidly and finally be clamped during the voltage fall time. Thus, according to (7), $R_{\text{blk}}$ can be selected based on $C_{\text{desat}}$ $\frac{dv}{dt}$ first, which is the displacement current flowing through the desat diode. As displayed in Fig. 8, turn-on $dv/dt$ of the 10 kV/20 A SiC MOSFET increases rapidly as the MOSFET switches at higher voltage levels, while $C_{\text{desat}}$, the charge-equivalent linear capacitance of the desat diode, reduces significantly as the switching voltage rises [37], [39]. As a result, the displacement current $C_{\text{desat}}$ $\frac{dv}{dt}$ increases by 237% as the voltage increases from 200 to 6500 V, as indicated in Fig. 9. To satisfy the requirement in (7) at all voltage levels under 6500 V, $R_{\text{blk,eq}}$ should be at least 1.01 kΩ. $R_{\text{blk}}$ is finally selected as 3.25 kΩ after considering 200% margin.

The margin is introduced for multiple reasons. $V_{\text{desat,inf}}$ should be much lower than $V_{\text{clamp}}$ in order to guarantee that $V_{\text{desat}}$ can drop to $V_{\text{clamp}}$ and be clamped by $D_{\text{blk}}$ before the voltage fall time of $V_{\text{ds}}$ is over, which is usually shorter than 150 ns. The forward voltage drop of $D_{\text{blk}}$ should be considered as well. The margin is also helpful in ensuring $V_{\text{desat}}$ can be clamped at $V_{\text{clamp}}$ when the MOSFET switches with lower turn-on $dv/dt$. For example, the turn-on $dv/dt$ will be lower

![Figure 6](image6.png)

FIGURE 6. Waveform of $V_{\text{desat}}$ during 6 kV ac–dc continuous test (with clamping diode $D_{\text{blk}}$, 56 pF $C_{\text{blk}}$, 6.5 kΩ $R_{\text{blk}}$, 470 Ω $R_{g,\text{cla}}$).

![Figure 7](image7.png)

FIGURE 7. Waveform of $V_{\text{desat}}$ during 6 kV ac–dc continuous test (without clamping diode $D_{\text{blk}}$, 56 pF $C_{\text{blk}}$, 6.5 kΩ $R_{\text{blk}}$, 470 Ω $R_{g,\text{cla}}$).

![Figure 8](image8.png)

FIGURE 8. Turn-on $dv/dt$ (at 5 A and 25 °C) of 10 kV/20 A SiC MOSFETs and equivalent capacitance of desat diode at different voltage levels.

![Figure 9](image9.png)

FIGURE 9. Displacement current flowing through desat diode ($C_{\text{desat}}$ $\frac{dv}{dt}$, calculated based on data in Fig. 8) at different voltage levels.
than the $dv/dt$ data in Fig. 8 if the MOSFET switches with higher gate resistance or the load current is higher than 5 A. Therefore, the 200% margin is necessary.

When selecting $R_{\text{blk}}$, it is not recommended to add too much margin, which will slow down the protection response. Also, the selection of $R_{\text{blk}}$ is heavily impacted by the switching speed of the 10 kV SiC MOSFET. Higher turn-on $dv/dt$ caused by the smaller gate resistance enables the use of a smaller $R_{\text{blk}}$ and makes protection response even faster.

B. DESIGN DETAILS OF $C_{\text{blk}}$

As for the selection of $C_{\text{blk}}$, it should be as small as possible to ensure that $V_{\text{desat}}$ is brought down to $V_{\text{clamp}}$ rapidly before the voltage fall time is over. Another important consideration is that a small $C_{\text{blk}}$ supports the fast protection response. The lower limit of $C_{\text{blk}}$ is determined by the requirement that $V_{\text{desat,M}}$ should not exceed the threshold voltage before the high negative $dv/dt$ is generated during the turn-on transient, as shown in the following equation:

$$V_{\text{desat,M}} = V_{\text{clamp}} + \frac{(V_{cc} - V_{\text{clamp}}) R_{\text{blk,eq}}}{R_{\text{blk}}} \left( 1 - e^{-\frac{t_d - t_{\text{cla}}}{R_{\text{blk,eq}}}} \right) < V_{\text{desat,th}}.$$  

(9)

$t_d$ is defined as the time interval between the rising edge of $V_{gs}$ and the starting point of the voltage fall time with high $dv/dt$. In other words, $t_d$ is the sum of $t_{\text{m}}$ and $t_{\text{cla}}$. If $V_{\text{desat,M}}$ is higher than $V_{\text{desat,th}}$ due to the small $C_{\text{blk}}$, the desat protection will be falsely triggered before the voltage fall time. The requirement for $C_{\text{blk}}$ can be rewritten as

$$C_{\text{blk}} > \frac{t_d - t_{\text{cla}}}{t_{\text{m}} R_{\text{blk,eq}} \ln \left( \frac{V_{cc} - V_{\text{clamp}} R_{\text{blk,eq}}}{(V_{cc} - V_{\text{clamp}}) R_{\text{blk,eq}} + R_{\text{blk}} (V_{\text{clamp}} - V_{\text{desat,th}})} \right)}.$$  

(10)

The lower limit of $C_{\text{blk}}$ is mainly determined by $t_d$ and $t_{\text{cla}}$. Based on measured switching transients of 10 kV SiC MOSFETs, $t_d$ is a strong function of the load current and junction temperature, as shown in Fig. 10. Higher load current leads to longer $t_d$, because of the longer current rise time during the turn-on transient [40]. At higher junction temperature, $t_d$ becomes shorter due to the lower gate threshold voltage $V_{g,\text{th}}$ and shorter turn-on delay time [18]. The dc voltage does not have a significant influence on $t_d$, as shown in the waveforms of $V_{ds}$ in Fig. 11 during the turn-on transient with dc voltage ranging from 1 to 6.5 kV at 10 A load current. As dc voltage decreases from 6.5 to 1 kV, $t_d$ only reduces by 7.6%, which could be attributed to the slightly higher $V_{g,\text{th}}$ at higher dc voltage [18]. In summary, $t_d$ is dominated by the load current and junction temperature during the normal turn-on transient of the 10 kV/20 A SiC MOSFETs.

As higher load current and lower junction temperature lead to longer $t_d$, the selection of $C_{\text{blk}}$ should be based on the maximum device current of the 10 kV SiC MOSFET and lowest device junction temperature. To support a higher load current, a higher $C_{\text{blk}}$ should be selected, and the response time to clear short circuit faults will be longer.

In fact, $C_{\text{blk}}$ in this article is the lumped capacitance between $V_{\text{desat}}$ and $V_{\text{clamp}}$. The nonlinear parasitic capacitance of $D_{\text{blk}}$ and $M_{\text{cla}}$, and the parasitic capacitance due to PCB layout, should all be included in $C_{\text{blk}}$. $C_{\text{blk}}$ brought by parasitic capacitances can be modeled with a linear capacitor, based on the waveform of $V_{\text{desat}}$ measured in the benchtop test without any capacitor populated as $C_{\text{blk}}$. The benchtop test results show that $C_{\text{blk}}$ due to parasitic capacitances can be modeled by an equivalent linear capacitance of 51.2 pF [37]. To reduce $C_{\text{blk}}$ caused by parasitic capacitances, $D_{\text{blk}}$ and $M_{\text{cla}}$ with small parasitic capacitance should be selected, and the PCB layout can be modified with the parasitic capacitance between $V_{\text{desat}}$ and $V_{\text{clamp}}$ fully considered.

$C_{\text{blk}}$ should be selected based on the maximum $t_d$ at rated device current (20 A) and the lowest operation temperature, which is 25 °C in the current article to simplify the analysis. According to measured turn-on transient waveforms of the 10 kV/20 A SiC MOSFET, the maximum $t_d$ is 235 ns at 6.5 kV/20 A. Then, if we neglect $t_{\text{cla}}$ by using a small $R_{goff,\text{cla}}$, the selected $C_{\text{blk}}$ should be 54.4 pF. In fact, $V_{\text{desat}}$ might start to rise before $V_{gs}$ starts to increase from $-5$ V $V_{\text{clamp}}$ because of the 40 ns propagation delay of the gate driver IC. So, the maximum $t_d$ we use for selecting $C_{\text{blk}}$ is increased to 285 ns, and $C_{\text{blk}}$ is finally selected as 66 pF. Considering the 51.2 pF $C_{\text{blk}}$ caused by parasitic capacitances, the installed $C_{\text{blk}}$ is
In the equation, the impact of displacement current from the desat protection design 1 with ultrafast response. In reality, measurement results show that this design has 20 ns $t_{\text{cla}}$ due to the 110 $\Omega$ $R_{\text{goff,cla}}$.

Based on (10), the lower limit of $C_{\text{blk}}$ can be smaller by selecting a higher $R_{\text{goff,cla}}$ to prolong $t_{\text{cla}}$. Adopting longer $t_{\text{cla}}$ and smaller $C_{\text{blk}}$ can speed up the response of the desat protection under a FUL and a flashover short circuit fault [31]. The protection response under a FUL or flashover fault will not be affected by $t_{\text{cla}}$, since $M_{\text{cla}}$ is already turned OFF when the two kinds of faults happen, while a smaller $C_{\text{blk}}$ will accelerate the protection response under the two kinds of faults. So, we can design the desat protection design 2 with ultrafast protection response by selecting a larger $R_{\text{goff,cla}}$ and a smaller $C_{\text{blk}}$.

In this case, we achieve the lowest feasible $C_{\text{blk}}$ by not installing any capacitor in the position of $C_{\text{Cla}}$. The equivalent $C_{\text{blk}}$ is hence 51.2 pF. Then, $t_{\text{cla}}$ should be selected based on the 285 ns maximum $t_d$ to avoid the false triggering due to the higher $V_{\text{desat},M}$. According to (10), the requirement for $t_{\text{cla}}$ can be written as

$$t_{\text{cla}} > t_d - C_{\text{blk}} R_{\text{blk},eq} \ln \left( \frac{V_{cc} - V_{\text{clamp}}}{V_{cc} - V_{\text{clamp}}} R_{\text{blk},eq} + R_{\text{blk}} (V_{\text{clamp}} - V_{\text{desat,th}}) \right). \tag{11}$$

So, $t_{\text{cla}}$ is selected as 65 ns in order to make sure that $V_{\text{desat},M}$ is still lower than the protection threshold voltage when $t_d$ is as long as 285 ns. Compared to the desat protection design 1, the desat protection design 2 with ultrafast response has longer $t_{\text{cla}}$ to enable a smaller $C_{\text{blk}}$, as shown in Table 1. $t_{\text{cla}}$ is an influencing factor of the protection response under the HSF fault, although it is independent of the protection response under a FUL and a flashover fault. Under the HSF fault, the time interval $t_{\text{HSF}}$ between the rising edge of $V_{gs}$ and the falling edge of $V_{gs}$ after the protection is triggered to clear the fault can be estimated as follows:

$$t_{\text{HSF}} = t_{\text{cla}} + C_{\text{blk}} R_{\text{blk},eq} \ln \left( \frac{V_{cc} - V_{\text{clamp}}}{V_{cc} - V_{\text{clamp}}} R_{\text{blk},eq} + R_{\text{blk}} (V_{\text{clamp}} - V_{\text{desat,th}}) \right). \tag{12}$$

<table>
<thead>
<tr>
<th>$R_{\text{goff,cla}}$ [Ω]</th>
<th>$t_{\text{cla}}$ [ns]</th>
<th>$t_{\text{cla}}$ [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured $t_{\text{cla}}$</td>
<td>20</td>
<td>65</td>
</tr>
<tr>
<td>Installed $C_{\text{eq}}$</td>
<td>15 pF</td>
<td>0 pF</td>
</tr>
<tr>
<td>Equivalent $C_{\text{eq}}$</td>
<td>66.2 pF</td>
<td>51.2 pF</td>
</tr>
<tr>
<td>$R_{\text{eq}}$ [Ω]</td>
<td>3.25</td>
<td>3.25</td>
</tr>
<tr>
<td>Calculated $t_{\text{goff}}$ [ns]</td>
<td>305</td>
<td>285 ns</td>
</tr>
</tbody>
</table>

15 pF. This is called the desat protection design 1 with ultrafast protection response. In reality, measurement results show that this design has 20 ns $t_{\text{cla}}$ due to the 110 $\Omega$ $R_{\text{goff,cla}}$.

In the equation, the impact of displacement current from $C_{\text{desat}}$ is neglected during the fault, in order to simplify the analysis. After applying the requirement in either (10) or (11) to (12), we can obtain the following result:

$$t_{\text{HSF}} > t_d. \tag{13}$$

So, no matter how $t_{\text{cla}}$ and $C_{\text{blk}}$ are designed, $t_{\text{HSF}}$ should always be longer than the maximum $t_d$. The calculated $t_{\text{HSF}}$ of the two protection designs can be seen in Table 1, both of which are longer than the maximum $t_d$. In summary, with the proposed desat protection scheme, the response under the HSF is limited by $t_{\text{cla}}$, which is determined by the turn-ON characteristic of the 10 kV SiC MOSFET. Because of the smaller $C_{\text{blk}}$, the desat protection design 2 can have a faster response to clear a FUL and a flashover fault. Yet the desat protection design 2 has almost the same response to clear the HSF fault as the desat protection design 1.

In terms of the protection response under a FUL and a flashover fault, the response time is limited by how low $C_{\text{blk}}$ can be in reality. The lowest $C_{\text{blk}}$ that can feasibly be achieved is determined by the parasitic capacitance between $V_{\text{desat}}$ and $V_{\text{clamp}}$. Then, the required $t_{\text{cla}}$ and $R_{\text{goff,cla}}$ can be selected accordingly, based on (11). The selection of $t_{\text{cla}}$ will not influence the turn-ON characteristic of $M_{\text{cla}}$, since the turn-OFF gate resistance of $M_{\text{cla}}$ is different from its turn-ON gate resistance, as shown in Fig. 3.

In addition, when designing the desat protection scheme with ultrafast response for the implementation realized with a gate driver IC shown in Fig. 1(a), $t_{\text{cla}}$ cannot be selected, since it is determined by the gate driver IC. Without this design freedom, the protection response under a FUL and a flashover fault cannot be tuned. $C_{\text{blk}}$ should be selected based on the maximum $t_d$ and the $t_{\text{cla}}$ determined by the gate driver IC.

### V. EXPERIMENTAL RESULTS

A half bridge phase leg based on two 10 kV/20 A SiC MOSFETs is built to validate the performance of the proposed desat protection scheme with ultrafast response [31]. The response time in this article is defined as the time interval between the moment when the short-circuit current exceeds the threshold current and the moment when the current starts to drop.

The desat protection design 1 in Table 1 is fully tested with short-circuit tests and ac–dc continuous switching test. HSF short circuit test result at 6.5 kV demonstrates that the HSF with a peak current of 71.2 A is cleared with a response time of 120 ns. The 120 ns response time is 65% shorter than the response time of the improved desat protection in [31] when clearing the HSF fault for the same MOSFET.

As can be seen in Fig. 12, the protection responds and initiates the soft turn-OFF process within 370 ns after $V_{gs}$ starts to rise. The measured $t_{\text{HSF}}$ is 370 ns, slightly longer than the calculated 305 ns $t_{\text{goff}}$ in Table 1. The difference is mainly due to the total propagation delay when the gate driver is trying to turn OFF the MOSFET, especially the 40 ns propagation delay in the gate driver IC. The other reason is that the low negative bias voltage...
$dv/dt$ of $V_{ds}$ during the HSF fault slows down the rise of $V_{desat}$ slightly.

FUL short-circuit test of the lower MOSFET in the phase leg is also conducted at 6.5 kV, as displayed in Fig. 13. The FUL short-circuit is generated by turning on the upper MOSFET of the half-bridge phase leg when the lower MOSFET is fully ON. Thus, the lower MOSFET will experience the FUL. The response time is 215 ns after the device current reaches the threshold current. In fact, the device current continues increasing after the soft turn-OFF process is initiated, until it reaches the peak current of 80 A. The detection time before triggering the soft turn-OFF process is only 95 ns, as shown in Fig. 13.

In addition to the ultrafast protection response, the strong noise immunity of the desat protection design 1 with ultrafast response is fully validated with the ac–dc continuous power test at 6.6 kV. During the ac–dc continuous test, the protection was never falsely triggered. The waveforms captured during the continuous test can be seen in Figs. 14 and 15. When the load current is positive, the lower MOSFET cannot achieve ZVS turn-ON and serves as the active switch in the phase leg. The magnitude of $V_{desat,M}$ becomes considerable, and $V_{desat,M}$ has a sinusoidal shape because higher device current leads to longer $t_d$. The magnitude of $V_{desat,M}$ in Figs. 6 and 7 is low due to the large time constant of the R-C network and the large $R_{goff,cla}$ (470 $\Omega$). As shown in the zoom-in waveform with $\sim$5.5 A load current in Fig. 15, because of the small $R_{goff,cla}$, $V_{desat}$ rises almost immediately after $V_{gs}$ starts to rise. $V_{desat}$ exceeds 10 V before quickly dropping to $\sim$−5 V because of the high negative $dv/dt$ during the fast turn-ON transient, which also supports the analysis in Fig. 5.

The desat protection design 2 with ultrafast response is also validated with a series of short circuit tests and ac–dc continuous test. With the desat protection design 2 with ultrafast response, HSF short-circuit test result at 6.5 kV proves that the HSF fault with a peak current of 68 A is cleared with a response time of 115 ns, as displayed in Fig. 16. The HSF short-circuit test setup is the same as the desat protection design 1 with ultrafast response. The measured $t_{HSF}$ is 358 ns, still slightly higher than the calculated 285 ns $t_{HSF}$ in Table 1, which is similar to the case in protection design 1.

Although the test setup generating a flashover fault is not available in the laboratory, the FUL test setup can be adjusted...
to generate a FUL, which is similar to a flashover fault. In the phase leg, the upper MOSFET used to generate a FUL has 15 Ω turn-on gate resistance. To make the FUL closer to a flashover fault, the turn-on gate resistance of the upper MOSFET is reduced to 3 Ω, resulting in higher \( \frac{di}{dt} \) during the fault. The FUL short-circuit fault is successfully cleared at 6.5 kV with the desat protection design 2 with ultrafast response. With an R-C network with a smaller time constant, \( V_{\text{desat}} \) can follow \( V_{ds} \) with a shorter delay. The response time is further reduced to 155 ns, and the detection time before triggering the soft turn-OFF process is only 82 ns, which is also reduced compared to the desat protection design 1. To continue reducing the detection time and response time, \( C_{\text{blk}} \) caused by parasitic capacitances should be minimized, as discussed in Section IV. Regarding response time, Table 2 summarizes the detailed comparison of the desat protection design 1 and design 2 with ultrafast response.

<table>
<thead>
<tr>
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<th>Desat protection design 1</th>
<th>Desat protection design 2</th>
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<tbody>
<tr>
<td>Response time under HSF fault</td>
<td>120 ns</td>
<td>115 ns</td>
</tr>
<tr>
<td>Response time under FUL fault</td>
<td>215 ns</td>
<td>155 ns</td>
</tr>
</tbody>
</table>

The detailed waveforms can be seen in Fig. 17. Because of the higher \( \frac{di}{dt} \) of the short-circuit current (0.26 A/ns), the peak short-circuit current is higher than 80 A, although the desat protection design 2 with ultrafast response has shorter response time than the desat protection design 1. After the fault is generated, the measured \( V_{gs} \) reaches 18 V, higher than the spike in Fig. 13. This is attributed to the higher voltage drop on the common source inductance of the MOSFET due to 53% higher \( \frac{di}{dt} \). In fact, there is considerable common source inductance in the discrete 10 kV SiC MOSFETs due to the lack of Kelvin source terminal [18]. The noise immunity of the protection design 2 is also fully validated with the ac–dc continuous power test at 6.6 kV, during which the protection was never falsely triggered. Even though \( C_{\text{blk}} \) is completely realized by parasitic capacitances, strong noise immunity is still achieved by following design guidelines in [25]. Because of the larger \( R_{\text{goff,cla}} \) (348 Ω) and longer \( t_{\text{cla}} \), \( V_{\text{desat,M}} \) is reduced substantially compared to the desat protection design 1 under the same test condition (6.6 kV, 0.55 modulation index). With longer \( t_{\text{cla}} \), \( V_{\text{desat,M}} \) still has a sinusoidal shape with the ac load current whose fundamental component has a peak value of ~6 A, as can be seen in Fig. 18. The zoom-in waveform in Fig. 19 confirms that \( V_{\text{desat}} \) is clamped at ~5 V after \( V_{ds} \) of the lower MOSFET starts to fall with high \( \frac{dv}{dt} \). Fig. 19 also reveals that \( t_{\text{cla}} \) in desat protection design 2 is significantly longer than \( t_{\text{cla}} \) in desat protection design 1. In summary, both strong noise immunity and ultrafast response of the desat protection design 2 are demonstrated with experimental results at rated voltage. Both HSF and FUL can be cleared with a response time of <160 ns. To the best of the authors’ knowledge, this is the fastest response achieved by a protection scheme based on desat protection for a discrete 10 kV SiC MOSFET.

VI. DISCUSSION

Both theoretical analysis and experimental results have proven that proposed desat protection design 2 with ultrafast response...
FIGURE 19. Zoom-in waveforms captured during 6.6 kV ac–dc continuous test with desat protection design 2 with ultrafast response.

FIGURE 20. Flowchart of the design process of proposed desat protection with ultrafast response.

FIGURE 21. Typical waveforms of $V_{ds}$ under HSF, FUL, and flashover short circuit fault.

has an even faster response under the FUL and flashover faults than desat protection design 1, while they have almost the same response time under the HSF fault. Based on the design details of the desat protection design 2, therefore, the detailed design process of the proposed ultrafast desat protection is summarized in the design flowchart in Fig. 20.

First, the clamping diode $D_{blk}$ and Si MOSFET $M_{cla}$ should be selected, whose reverse recovery process can prolong the effective blanking time. Then the design flowchart starts with six given parameters: $V_{cc}$, $V_{clamp}$, required blanking time $t_{blk}$, max $t_d$, the displacement current $C_{desat}dv/dt$, and minimum $C_{blk}$. Minimum $C_{blk}$ is the effective parasitic capacitance between $V_{desat}$ and $V_{clamp}$, hence it is determined by $D_{blk}$, $M_{cla}$, and parasitics. Using minimum $C_{blk}$ without adding any $C_{blk}$ capacitor on purpose is key to ensuring ultrafast response. Two decision points are designed in the flowchart to ensure that ultrafast response is realized without any false triggering during normal operation of high voltage SiC MOSFETs, including the experimental validation. Also, the design process in Fig. 20 can be applied to various gate driver designs leading to different switching speed, although different gate driver designs will impact the starting point of the design process, especially the max $t_d$ and $C_{desat}dv/dt$.

The proposed desat protection scheme in this article features several advantages in terms of protecting high voltage SiC MOSFETs. To start with, it possesses an ultrafast protection response and strong noise immunity simultaneously. Although the desat protection circuitry has an R-C network with a small time constant, design guidelines in [25] can be applied to ensure that the noise immunity will not be sacrificed. The ultrafast protection response can effectively help reduce the short-circuit current and energy loss of both discrete devices and modules.

Furthermore, the implementation of the desat protection scheme with ultrafast response is as simple as the conventional desat protection design. Compared to the conventional desat protection design, no additional circuitry and components are required. Moreover, the circuitry of the desat protection scheme with the ultrafast response is compatible with that of the conventional desat protection design. The conventional desat protection design can be easily modified to switch to the proposed desat protection design with ultrafast response, without ordering a new PCB. In the implementation in Fig. 1(b), only $R_{blk}$, $C_{blk}$, and the clamping diode $D_{blk}$ need to be replaced. Also, the proposed desat protection scheme with ultrafast response is effective for both mainstream implementations for high voltage SiC MOSFETs in Fig. 1.

Under the overcurrent or short-circuit fault with very low $dv/dt$ during the conduction state of the high-voltage SiC MOSFET, the proposed ultrafast desat protection can respond like the conventional desat protection but respond much faster, because the proposed method can have $V_{desat}$ follow $V_{ds}$ with shorter delay since the proposed desat scheme has R-C network with a smaller time constant. The limitation of the proposed desat protection scheme with ultrafast protection is that it cannot have the ultrafast response in short-circuit faults with high negative $dv/dt$. In normal turn-ON transients with high negative $dv/dt$, it takes advantage of the negative $dv/dt$ to effectively prolong the blanking time. As a result, if high negative $dv/dt$ is generated during the short-circuit fault, it will take a long time for $V_{desat}$ to reach the protection threshold $V_{desat,th}$, leading to a much longer response time than the cases without high negative $dv/dt$. If the negative $dv/dt$ is extremely high with a long voltage fall time during the short circuit
fault, the protection could be too slow to protect the MOSFET. However, it is not common to have high-negative \( \frac{dv}{dt} \) during the short circuit and overcurrent conditions, as shown in Fig. 21. During a FUL and a flashover fault, the waveform of \( V_{ds} \) is dominated by a high positive \( \frac{dv}{dt} \). During an HSF, usually \( V_{ds} \) only experiences a small dip with a low negative \( \frac{dv}{dt} \) for a short time, which results in a small displacement current.

**VII. CONCLUSION**

A desat protection scheme with ultrafast response is proposed for high-voltage (>3.3 kV) SiC MOSFETs that possess strong noise immunity and simple implementation. The proposed protection scheme has the same fundamental working principle and circuitry as the conventional desat protection. However, the blanking time requirement is satisfied by fully taking advantage of the high negative \( \frac{dv}{dt} \) during the turn-off transient and the reverse recovery effect of the clamping diode. Therefore, a much smaller blanking capacitor \( C_{bk} \) and an R-C network with a much smaller time constant can be used, leading to ultrafast protection response under various short circuit and overcurrent conditions. Hence, higher \( \frac{dv}{dt} \) can be leveraged in design of the proposed desat protection scheme to further accelerate the response. The proposed protection scheme is demonstrated to safely protect discrete 10 kV SiC MOSFETs. The ultrafast response and strong noise immunity of the proposed protection scheme are validated in comprehensive tests at 6.5 kV. The proposed method can clear an HSF with a response time of 115 ns and a FUL with a response time of 155 ns, which is the fastest reported response for a protection scheme based on desat protection when protecting a discrete 10 kV SiC MOSFET. In the future work, this method with high \( \frac{dv}{dt} \) fully considered can be extended to the desat protection design for other types of power semiconductor devices with high \( \frac{dv}{dt} \).

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