Medium-Voltage Isolated Auxiliary Power Supply Design for High Insulation Capability, Ultra-Low Coupling Capacitance, and Small Size

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***Abstract*—To fully utilize the benefits of medium-voltage (MV) silicon carbide (SiC)-based converter and achieve high power density, the isolated auxiliary power supply (IAPS) needs to be as small as possible. However, the high insulation and low coupling capacitance requirements, considering the high voltage and high *dv*/*dt*, are constraints of size reduction. This article proposes an MV IAPS design for high insulation capability, ultra-low coupling capacitance, and small size. The topology selection, efficiency, load regulation, coupling capacitance, and size reduction considerations are discussed. A 2.5 W MV IAPS is designed and built for a 10 kV SiC MOSFET-based 13.8 kV/100 kW three-phase converter, achieving a partial discharge (PD) inception voltage of higher than 15 kV rms, ultra-low coupling capacitance of 1.03 pF, and smaller size than that of the commercial products as well as the state-of-art research prototypes. Experimental results of PD test, 10 kV SiC MOSFET-based half-bridge test, and 13.8 kV/100 kVA three-phase converter full rating test are conducted for design validation.**

***Index Terms*—Coupling capacitance, isolated auxiliary power supply (IAPS), medium voltage (MV), partial discharge (PD), silicon carbide (SiC).**

I. Introduction

BECAUSE of their high blocking voltage, low switching loss, high junction temperature, and fast switching speed, medium-voltage (MV) silicon carbide (SiC) devices provide promising solutions for MV grid power electronics with converter-level benefits, such as high efficiency and high power density, and system level-benefits, for example, better grid support functions [1], [2], [3], [4], [5]. However, there are still many challenges to fully realizing these benefits of MV SiC devices, and the MV ($\geq$10 kV) isolated auxiliary power supply (IAPS) design is one of them [6].

To fully utilize the benefits of MV SiC devices and achieve high power density, the IAPS, which is commonly used to supply the gate drive (GD) and sensors, needs to be designed as small as possible. However, the high-voltage application requires high insulation capability of the IAPS, which requires sufficient insulation distance. Besides, the low coupling capacitance is required for the IAPS to limit the common mode (CM) current caused by the high *dv*/*dt* of the MV SiC devices, preventing the converter from high CM noise [7], [8]. Nevertheless, the high insulation and the low coupling capacitance requirements are two main constraints for the size reduction of the IAPS.

The MV IAPS design has been discussed in the literature. Based on the insulation approaches between the primary side and the secondary side, this design can be divided into four categories.

The first category is air-insulated design, in which the voltage is fully or partially stressed on the air gap [9], [10], [11], [12], [13], [14], [15], [16]. This type of design can easily achieve a small coupling capacitance because of the low dielectric constant of air. However, due to the low dielectric strength of air, the clearance distance needs to be sufficiently large to achieve the required insulation capability. As a result, the size of the IAPS is large [17]. Besides, a sufficient creepage distance is also required, depending on the surface material and the application environment, to avoid corona discharge. The creepage distance is generally achieved by three approaches: putting the primary side and the secondary side away from each other [9], [11], using a long MV cable as one side winding wire [10], [12], [13], and adding groove on the path between the two sides [14]. Compared to the first two approaches, the third approach can help to reduce the size. Therefore, this approach is more suitable for lower voltage applications or applications where the power density is not concerned.

The second category is PCB-based insulation design, which means the high voltage is fully stressed on the PCB substrates. The isolated transformer windings are located on the two sides of a PCB [18]. The main advantage of this type of design is that it is easy to achieve an insulation capability because of the high electrical strength, and it does not require any potting process.

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Also, the manufacturing of the transformer and windings are easy. However, the partial discharge (PD) performance highly relies on the PCB quality (cavities and bubbles). Besides, the high dielectric constant of the PCB material (e.g., FR4 is around 3.8 to 4.8) leads to a high coupling capacitance. For example, the coupling capacitance of the IAPS designed in [18] is around 8–14 pF due to the thin PCB thickness and high dielectric constant of FR4. To get a low coupling capacitance, the PCB thickness must be large, which increases the cost. Therefore, this approach has many limitations for use.

The third category is optical fiber-based insulation design, which theoretically eliminates the coupling capacitance, and can achieve high insulation capability. However, the main drawback is the low power rating (0.5 W) and low efficiency (24%) [19].

The fourth category is the silicone or epoxy encapsulation-based method [10], [20], [21], [22], [23], [24]. This approach is more suitable for higher voltage applications because of the high electrical strength of the insulation material. However, compared to air, these materials have a higher dielectric constant (usually between 2 and 4), which results in a large coupling capacitance. For example, in [10], the PD inception voltage (PDIV) of the silicone encapsulated solution is 11.6 kV rms, and it is only 3.87 kV rms in the air-based solution; the coupling capacitance of the silicone solution is 3.61 pF, while that of the air solution is only 1.86 pF. Therefore, to reduce the coupling capacitance, a larger distance between the windings and between the winding and the core may need to be designed [20], which increases the size of the power supply.

For MV, high *dv*/*dt*, and high power density applications, insulation capability, coupling capacitance, and the size of the IAPS need to be considered. However, the size reduction usually means a shorter distance for insulation and higher coupling capacitance. Therefore, tradeoffs need to be made in the design. Besides, other power supply performances, such as efficiency and load regulation, also need to be considered.

Based on the above review and analysis, this article proposes the design of an MV IAPS to have high insulation capability, ultra-low coupling capacitance, and small size. Also, considerations of the topology, efficiency, and load regulation are discussed. The rest of this article is organized as follows. In Section II, the design requirements and topology considerations are discussed. Then, the electrical design considerations are introduced in Section III, followed by the transformer design considerations in Section IV. An IAPS design example for a 10 kV SiC MOSFET-based 13.8 kV/100 kW three-phase converter is provided in Section V, and experimental test results are given in Section VI. Finally, the article is concluded in Section VII.

II. MV IAPS Design Requirements and Topology Considerations

The IAPS generally consists of the primary-side circuitry, secondary-side circuitry, and the isolated transformer, and its design needs to consider electrical, insulation, and noise immunity requirements.

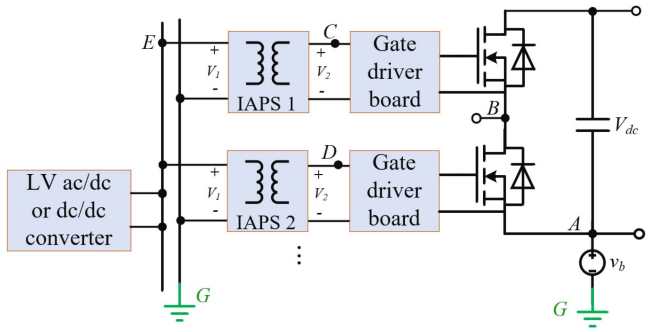


Fig. 1. IAPS connection in a half-bridge unit of the VSC.

A. Electrical Performance Requirements

The electrical requirements of the IAPS generally include the requirements for input voltage, power rating, output voltage, load regulation, efficiency, and protection. The input voltage, output voltage, and power rating are determined by the converter, GD, and sensor design. Although the IAPS power rating is low, mostly a few watts, it is necessary to have a higher efficiency to limit the loss, especially for converters with many devices. Commonly, the efficiency of low-voltage (LV) dc/dc power supply rated at a few watts is in the range of 80%–90% at the heavy load range. The load regulation defines the output voltage change range as the load changes. In many MV IAPS applications, it is not required to have a strong and accurate output load regulation because other dc/dc converters are adopted on the GD board to convert the IAPS output voltage to other voltage levels, such as +15, 5, and −5 V. Therefore, the IAPS output voltage is allowed to be in a range that the GD board dc/dc converters can operate properly. In addition, short circuit or overcurrent (OC) protection is widely adopted so that the fault on the GD can be isolated.

B. Insulation Requirements

The insulation requirements consist of the insulation voltage requirement and the coupling capacitance requirements. A basic unit in the voltage source converter (VSC) is the half-bridge circuit. As shown in Fig. 1, in MV applications, the two devices are, respectively, supplied with two MV IAPS, and their primary sides are supplied by the same LV dc power supply. To fully stress the high voltage on the MV IAPS and avoid high-voltage stress on the front-end LV ac/dc or dc/dc converter, the primary side of the IAPS is commonly grounded.

The voltage stress applied on the IAPS, V_{IAPS}, equals the voltage difference between the secondary-side and the primary-side voltages, i.e.

$$\begin{cases} V_{\mathrm{IAPS1}} = V_{CG} - V_{EG} = V_2 + V_{\mathrm{dc}} + v_b - V_1 \\ V_{\mathrm{IAPS2}} = V_{DG} - V_{EG} = V_2 + v_b - V_1 \end{cases} \quad (1)$$

where V_{CG}, V_{DG}, and V_{EG} are the voltages of points *C*, *D*, and *E* to the ground, respectively; V_2 and V_1 are the secondary-side and primary-side voltage of the IAPS, respectively; V_{dc} is the

dc-link voltage; and v_b is the voltage of the dc-link negative terminal, to the ground.

Since V_1 and V_2 are small, the main voltage stress on the IAPS is determined by $V_{\rm dc}$ and v_b. In most cases, $V_{\rm dc}$ is constant, but v_b could vary in different half bridges in a converter, depending on the topology and grounding configuration of the main power loop. The insulation requirement of the IAPS is determined by the highest voltage stress. Different from the conventional low-frequency (50/60 Hz) equipment, the voltage stress applied on the IAPS in the MV VSC converter is high-frequency PWM voltage. If PD occurs, the insulation material will be degraded quickly due to the high-frequency voltage stress, and eventually, it leads to breakdown. Moreover, the voltage stress is clamped by the dc-link capacitors, so it is almost constant, which is also different from the grid applications, where temporary and surge overvoltage may occur. Therefore, the PDIV is a much stricter requirement than the breakdown voltage, and the PDIV should be at least higher than the highest voltage stress. Also, some margin is necessary to ensure the reliability of long-term operations.

C. Noise Immunity Requirements

Although there has been some discussion about the IAPS CM noise [25], no clear requirements for the IAPS coupling capacitance are concluded. A larger coupling capacitance results in a larger CM current, flowing through the GD and the IAPS. Nevertheless, if the GD and the IAPS circuitry have sufficient noise immunity capability, the converter can still operate. On the other hand, a smaller IAPS coupling capacitance helps reduce CM current and thus reduces the effort on the GD and controller noise immunity design.

D. Topology Discussion

Many topologies used in the LV isolated dc/dc converter can be adopted for the MV IAPS with an MV isolated transformer. Based on the load regulation method, these topologies can be divided into three categories: open-loop regulated (OLR), secondary-side regulated (SSR), and primary-side regulated (PSR). OLR does not require feedback control, but the load regulation could be worse. The SSR requires an MV isolated signal feedback path from the secondary side to the primary side, which can be realized through an additional feedback winding or fiber optic, increasing either the coupling capacitance or the IAPS size and cost. The PSR is conducted by detecting the secondary side reflected voltage at the primary side, and thus it is simple to implement. However, depending on the topology, the PSR-based voltage sampling could be sensitive to the CM noise, and thus the IAPS control is impacted.

In [20], a flyback-based PSR MV IAPS is designed. The topology scheme is shown in Fig. 2. Since the voltage sampling point does not have any filter capacitor, it is sensitive to the CM current transferred from the secondary side. Experimental waveforms of the switching node voltage, the CM current, and the power stage PWM voltage of the MV IAPS designed in [20] are shown in Fig. 3. The CM current is obtained by measuring the net current of the positive and negative power wires of the IAPS,

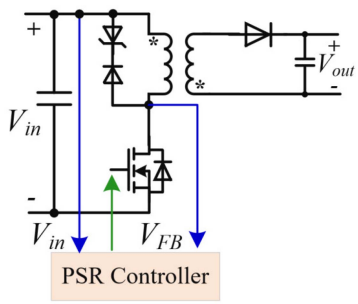


Fig. 2. Flyback converter topology.

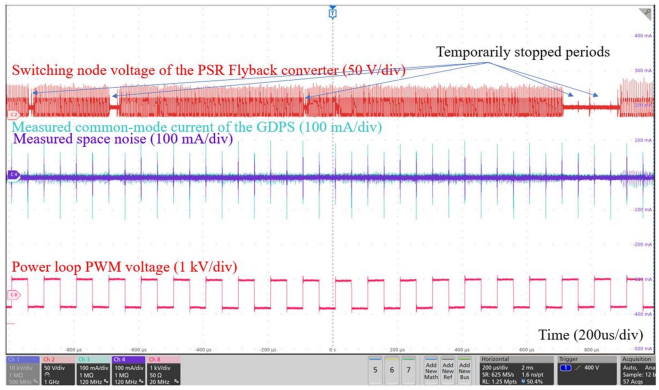


Fig. 3. Experimental waveforms showing the impact of CM on the PSR flyback converter.

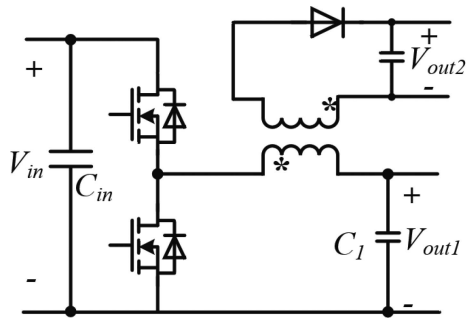


Fig. 4. Topology of the flybuck converter.

and the space noise is measured with a same current probe at the same location. The CM current spikes align with the rising and falling edges of the PWM voltage, corresponding to switching actions of devices. The flyback converter should have continuous switching actions and constant switching frequency during the steady state. However, in the test, the switching node voltage of the flyback converter is temporarily stopped, which is because the feedback voltage, V_{FB}, is affected by the CM current.

Compared to the PSR flyback, the PSR flybuck converter is more robust to the CM noise. As shown in Fig. 4, the flybuck converter has a primary-side output, $V_{\rm out1}$, and a secondary-side output, $V_{\rm out2}$. By regulating $V_{\rm out1}$, $V_{\rm out2}$ can also be regulated [26]. Since the feedback voltage is the voltage on capacitor C_1, the feedback is not sensitive to the CM current. With the CM

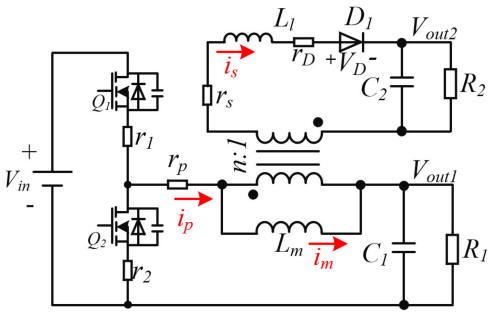


Fig. 5. Detailed flybuck converter topology.

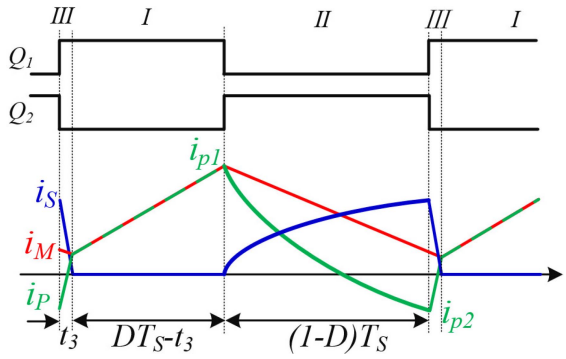


Fig. 6. Operating diagram and states of the flybuck converter.

current superimposed on the load current, the IAPS OC protection can be falsely triggered. This can be solved by increasing the OC threshold value to leave more margin. Also, reducing the coupling capacitance can help to reduce the impact of CM current.

Therefore, this article selects the PSR flybuck converter as the MV IAPS topology, and the efficiency, load regulation, size, insulation voltage, and coupling capacitance are the major design considerations to be discussed.

III. Electrical Design Considerations

A. State-Space Model of the Flybuck Converter

State-space model is used for the converter voltage and current waveform solving so that the efficiency and load regulation can be evaluated. The detailed topology is shown in Fig. 5: Q_1 and Q_2 are the upper and lower devices, respectively; r_1 and r_2 are the ON-resistance of Q_1 and Q_2, respectively; r_p and r_s are the primary-side and secondary-side transformer winding resistances, respectively; L_m and L_l are the magnetizing inductance and leakage inductance equivalented to the secondary side, respectively; C_1 and C_2 are the capacitance at the primary-side output and secondary-side output, respectively; R_1 and R_2 are the load resistance at the primary-side output and secondary-side output, respectively; n is the turn ratio of the primary side winding to the secondary winding; D_1 is the secondary-side diode; and r_D and V_D are ON-resistance and voltage drop of the diode, respectively.

The flybuck converter has three operation states, as shown in Fig. 6, in which T_s is the switching cycle and D is the duty cycle of Q_1. In state I, Q_1 is ON and Q_2 is OFF, the magnetizing current i_M increases with the primary-side current i_p, and D_1 is reversely clamped so that i_s is 0. In state II, Q_1 is OFF and Q_2 is ON, D_1 is forward conducted, and i_s increases. In state III, Q_1 is ON and Q_2 is OFF, and i_p increases and decreases. When i_s becomes zero, the converter transfers to state I. Using i_M, i_S, V_{out1}, and V_{out2} as state variables, the state-space equations can be expressed as

$$\begin{bmatrix} \frac{di_M}{dt} \\ \frac{di_s}{dt} \\ \frac{dV_{\text{out1}}}{dt} \\ \frac{dV_{\text{out2}}}{dt} \end{bmatrix} = \boldsymbol{A} \begin{bmatrix} i_M \\ i_s \\ V_{\text{out1}} \\ V_{\text{out2}} \end{bmatrix} + \boldsymbol{B} \begin{bmatrix} V_{\text{in}} \\ V_D \end{bmatrix} \tag{2}$$

where $\boldsymbol{A}$ and $\boldsymbol{B}$ are the state matrixes, and in the three different states, they are, respectively

$$A_1 = \begin{bmatrix} -\frac{r_1+r_p}{L_m} & \frac{(r_1+r_p)}{nL_m} & \frac{-1}{L_m} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & \frac{-1}{nC_1} & \frac{-1}{C_1R_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_2R_2} \end{bmatrix};$$

$$B_1 = \begin{bmatrix} \frac{1}{L_m} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3}$$

$$A_2 = \begin{bmatrix} -\frac{r_2+r_p}{L_m} & \frac{(r_2+r_p)}{nL_m} & \frac{-1}{L_m} & 0 \\ \frac{r_2+r_p}{nL_l} & -\left(\frac{r_2+r_p}{n^2L_l}+\frac{r_s+r_D}{L_l}\right) & \frac{1}{nL_l} & \frac{-1}{L_l} \\ \frac{1}{C_1} & \frac{-1}{nC_1} & \frac{-1}{C_1R_1} & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{C_2R_2} \end{bmatrix};$$

$$B_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{L_l} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{4}$$

$$A_3 = \begin{bmatrix} -\frac{r_1+r_p}{L_m} & \frac{(r_1+r_p)}{nL_m} & \frac{-1}{L_m} & 0 \\ \frac{r_1+r_p}{nL_l} & -\left(\frac{r_1+r_p}{n^2L_l}+\frac{r_s+r_D}{L_l}\right) & \frac{1}{nL_l} & \frac{-1}{L_l} \\ \frac{1}{C_1} & \frac{-1}{nC_1} & \frac{-1}{C_1R_1} & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{C_2R_2} \end{bmatrix};$$

$$B_3 = \begin{bmatrix} \frac{1}{L_m} & 0 \\ -\frac{1}{nL_l} & \frac{-1}{L_l} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{5}$$

With the state-space equations, the steady-state voltage and current waveforms can be solved. Then, the converter loss and the averaged output voltage can be easily calculated.

B. Load Regulation Consideration

The leakage inductance impacts the load regulation. As shown in Fig. 7, a larger leakage inductance leads to a slower secondary-side current ramp rate. Then, as the leakage inductance increases,

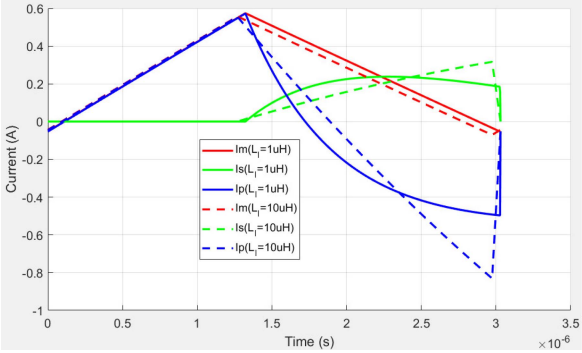


Fig. 7. Current waveforms in one switching cycle with different leakage inductances.

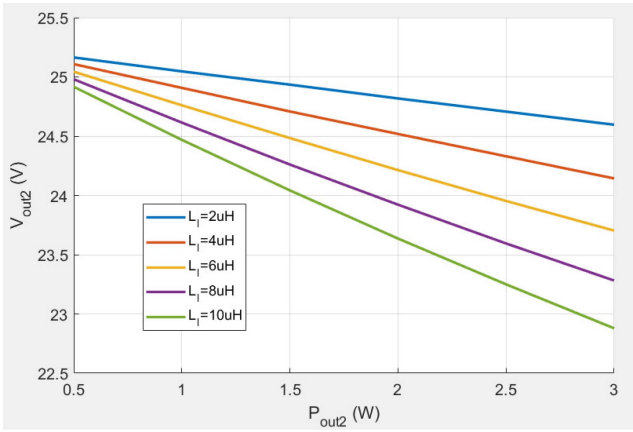


Fig. 8. Load regulation comparison among different leakage inductances with $V_{\text{in}} = 24$ V, $V_{\text{out1}} = 10.5$ V, $n = 5/12$, f_s= 330 kHz, and L_m= 28.3 μH.

the secondary-side output capacitance is less charged, and thus a less output voltage occurs.

A load regulation curve comparison among different leakage inductances is shown in Fig. 8. With a certain leakage inductance, the output voltage drops because that larger current leads to a higher voltage drop on the diode, winding resistance, and leakage inductance. For the same output power, a larger leakage inductance results in a lower output voltage.

The load regulation comparison among different switching frequencies is shown in Fig. 9. A higher switching frequency results in a lower output voltage. This is because it takes a certain time for the secondary-side current to ramp, and with a short switching period, the effective output capacitor charging time is reduced.

However, to achieve the high insulation capability and low coupling capacitance, the two windings are located away from each other, which increases the leakage inductance. Therefore, the transformer winding location and the switching frequency need to be properly designed so that the load regulation can meet the requirement.

C. Efficiency Estimation

The IAPS loss includes device loss, transformer loss, secondary-side diode loss, and control circuit loss. The device

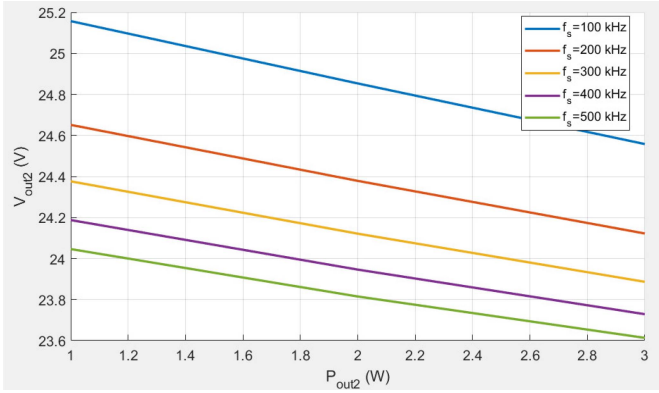


Fig. 9. Load regulation comparison among different switching frequencies with $V_{\text{in}} = 24$ V, $V_{\text{out1}} = 10.5$ V, $n = 5/12$, L_m= 28.3 μH, and $L_l = 10$ μH.

loss consists of switching loss and conduction loss; the transformer loss includes copper loss and core loss. With the current waveforms solved with the state-space mode, all the losses can be calculated.

Depending on the current direction at the moment of device switching, zero-voltage switching could be realized. The device switching loss can be estimated as

$$P_{\text{sw}} = \begin{cases} \frac{V_{\text{in}} i_p^2(t) t_r}{2 I_{\text{test}}} + \frac{V_{\text{in}}^2 i_p(t) t_f}{2 V_{\text{test}}} & \text{hard switching} \\ 0 & \text{soft switching} \end{cases} \tag{6}$$

where t_r and t_f are the current rise time and voltage falling time, respectively; and I_{test} and V_{test} are the test conditions for t_r and t_f, respectively. The device conduction losses are

$$P_{Q1\_\text{cond}} = \frac{1}{T_s} \int_0^{DT_s} i_p(t)^2 r_1 dt \tag{7}$$

$$P_{Q2\_\text{cond}} = \frac{1}{T_s} \int_{DT_s}^{T_s} i_p(t)^2 r_2 dt \,. \tag{8}$$

The transformer core loss can be estimated with Steinmetz's Equation

$$P_{\text{core}} = k f_s^{\alpha} B^{\beta} \tag{9}$$

where k, α, and β are the three coefficients in the Steinmetz's equation; f_s is the switching frequency; and B is the maximum flux density. The copper loss can be calculated as

$$P_{\text{copper}} = \frac{1}{T_s} \left(\int_0^{T_s} i_p(t)^2 r_p dt + \int_0^{T_s} i_s(t)^2 r_s dt \right) . \tag{10}$$

The secondary-side diode loss is

$$P_D = \frac{1}{T_s} \int_0^{T_s} i_s(t) \left(i_s(t) r_D + V_D \right) dt \,. \tag{11}$$

Then, the total converter loss is

$$\begin{aligned} P_{\text{loss}} = {} & P_{Q1\_\text{sw}} + P_{Q2\_\text{sw}} + P_{Q1\_\text{cond}} + P_{Q2\_\text{cond}} \\ & + P_{\text{core}} + P_{\text{copper}} + P_D + P_{\text{other}} \end{aligned} \tag{12}$$

where P_{other} includes the control circuit loss and some LED indicator circuit loss (if any).

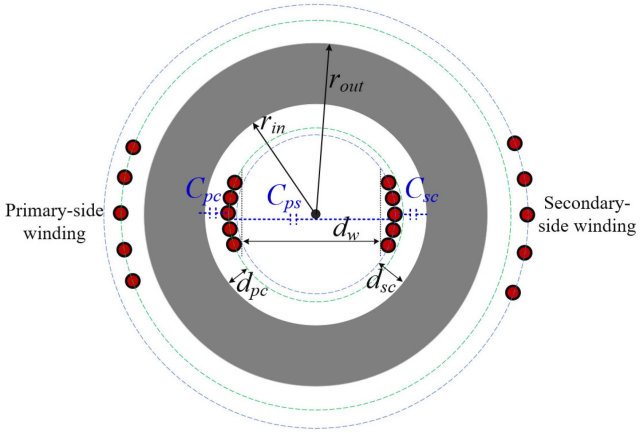


Fig. 10. Commonly used winding structure of the toroid core-based transformer.

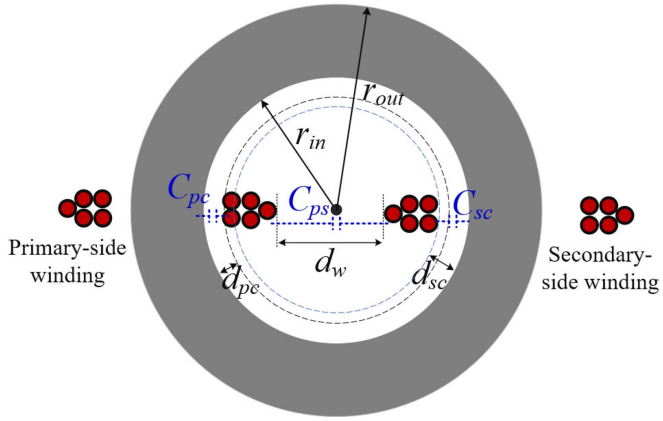


Fig. 11. Proposed winding structure.

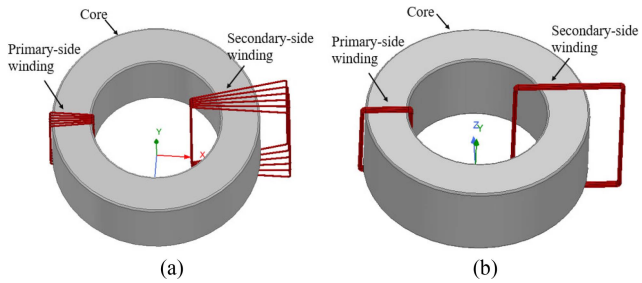


Fig. 12. Ansys/Maxwell3D simulation model of (a) conventional winding structure and (b) proposed winding structure.

Therefore, the efficiency is

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\% . \tag{13}$$

IV. Isolated Transformer Design Considerations

Many types of cores, including EI core, C core, UI core, and toroid core can be used for the IAPS transformer design. Considering the ease of mechanical support and no need for the air gap, the toroid core is adopted in this article. However, the analysis process can also be extended to other core types.

A. Proposed Winding Structure

The commonly used winding structure of the toroid core-based transformer is shown in Fig. 10. To minimize the coupling capacitance, the primary-side winding and the secondary-side winding are located at opposite sides of the core. Although the core could be coated, since its insulation capability is low, the core is considered to be an electrically conductive part in MV application. Therefore, to achieve the required insulation capability, at least one winding needs to be insulated from the core. The distance between the core and the primary-side winding and the secondary-side winding is d_{pc} and d_{sc}, respectively, which are provided by supporting structures, such as bobbins.

The coupling capacitance consists of three parts: the capacitance between the primary-side winding and the secondary-side winding C_{ps}, the capacitance between the primary-side winding and the core C_{pc}, and the capacitance between the secondary-side winding and the core C_{sc}. The total coupling capacitance is

$$C_p = C_{ps} + C_{pc} // C_{sc} . \tag{14}$$

Following three approaches can be adopted to reduce the capacitance between two electrical parts:

1) Reduce the effective area between them.
2) Increase the distance between them.
3) Decrease the dielectric constant of the material between them.

Increasing the distance leads to a large size, and decreasing the dielectric constant requires better material. Therefore, reducing the effective area between the two windings and between the winding and the core is a better approach to reducing the coupling capacitance.

The proposed winding structure is shown in Fig. 11, and the primary-side and secondary-side windings are grouped to reduce the effective area. Also, the outside winding turns form a shielding layer for the inner winding turns, and therefore the capacitance between the inner winding turns and the core or the other side winding is significantly reduced.

It is more accurate to estimate the capacitance using the finite-element method (FEM) than using theoretical equations. The Ansys/Maxwell3D simulation models for the commonly used and proposed winding structures are shown in Fig. 12(a) and (b), respectively. The comparison of the coupling capacitance between the two winding structures, with $d_{pc} = 0.1$ mm, AWG 32 wire, 6 primary-side turns, 6 secondary-side turns, B64290A0719X049 ferrite core, and air as the medium, is shown in Fig. 13. The comparison between C_{pc_1} and C_{pc_2} and between C_{sc_1} and C_{sc_2} show that by putting the winding turns together, capacitances between the winding and the core are reduced because of the smaller effective area. As a result, the total coupling capacitance of the proposed winding structure (C_{p_2}) is smaller than that of the commonly used winding structure (C_{p_1}). In addition, as the distance between the secondary-side winding and the core increases, the capacitance between them

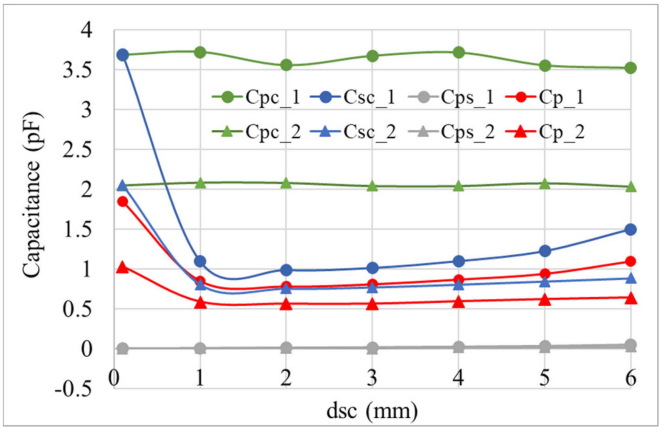


Fig. 13. Parasitic capacitance comparison between the conventional winding structure (labeled with _1) and the proposed winding structure (labeled with_2) with $d_{pc} = 0.1$ mm, AWG 32 wire, primary-side turn = secondary-side turn = 6, and B64290A0719X049 ferrite core with air as the medium.

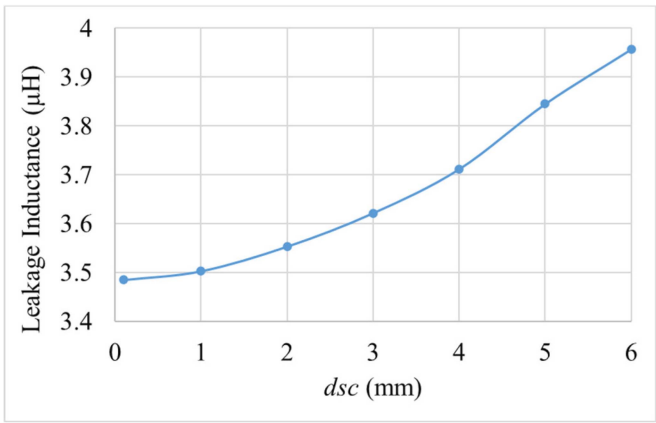


Fig. 14. Leakage inductance at the primary side in terms of different d_{sc} with $d_{pc} = 0.1$ mm, AWG 32 wire, primary-side turn = secondary-side turn = 6, and B64290A0719X049 ferrite core with air as the medium.

decreases at the beginning and then increases. This is because as the distance increases, the winding length increases, and so as the effective area also increases.

Therefore, the proposed winding structure significantly decreases the coupling capacitance C_p. To further reduce the C_p, the distance between the primary-side winding and the core can also be increased so that C_{pc} can be reduced, which is adopted in the following design.

B. Leakage Inductance

To achieve high insulation and low coupling capacitance, the winding is located at a certain distance from the core and the other side winding, which results in a large leakage inductance. With FEM, leakage inductance can also be estimated. As shown in Fig. 14, the total leakage inductance at the primary side increases with the distance between the winding and the core. However, when $d_{sc} = 0.1$ mm, the leakage inductance is already 3.5 μH, which means the main contribution of the leakage inductance comes from the opposite location of the two windings.

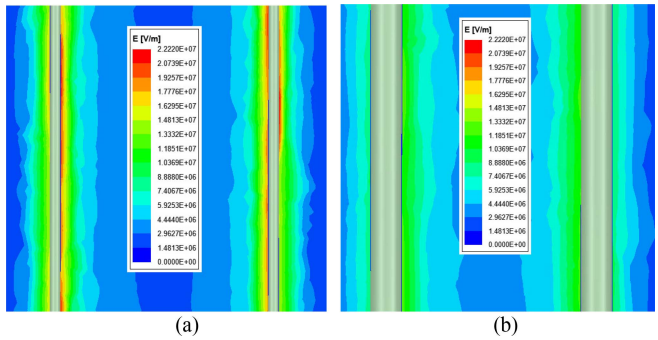


Fig. 15. Electrical field between two wires with 10 kV voltage stress and 2 mm distance and wire diameter of (a) 0.1 and (b) 0.3 mm.

C. Magnetic Wire and Electrical Field

First, the magnetic wire selection needs to consider the skin effect caused by the high-frequency current ripple. Increasing the switching frequency results in the use of thinner wire, and thus the wire loss increases. To reduce the wire loss, multiple wires can be paralleled or Litz wire can be used. Second, a thick wire leads to a larger surface area, and thus a larger coupling capacitance. Third, a thin wire results in a higher electrical field around the wire. As shown in Fig. 15(a) and (b), with the same distance and voltage stress, when the wire diameters change from 0.1 to 0.3 mm, the electrical field reduces from around 20 to 13 kV/mm.

D. Mechanical Design

The mechanical design of the transformer can be divided into two parts: one is the internal part and the other is the external part.

The internal mechanical design needs to consider the mechanical support of the core and the winding. Bobbins need to be designed to maintain the distance between the winding and the core and the distance between two windings. The core and bobbins must be reliably fixed, so that they will not move or deform, especially during the potting process with vibration.

The external mechanical design needs to consider three aspects. First, the creepage distance between the primary side and the secondary side needs to be sufficient for the maximum operating voltage. Some safety standards, such as IEC 61800-5-1, can be followed to determine the creepage distance based on the material category and the application environment. In the literature, the creepage distance is realized by three approaches: separating the primary-side and secondary-side winding terminals at least the creepage distance [20], using a long MV wire as one winding [10], and adding grooves on the path between the two sides [14]. Compare the first two approaches, the third approach helps to reduce the size of the transformer. Second, the connection between the transformer and the primary-side and the secondary-side circuitries needs to be reliable, and the connection must not result in shorter clearance or creepage

TABLE I
MV IAPS INSULATION MATERIAL COMPARISON

Material	Electrical strength (kV/mm)	Mixed viscosity @ 25 °C (mPa.s)	Dielectric constant	Thermal conductivity (W/mK)
Epoxy (50-3170)	18.9	15,000	3.4	1.73
Silicone elastomer (TC 4605)	24.0	1,900	4.1 (@50 kHz)	1.00
Silicone gel (SilGel 613)	23.0	180	2.9 (@10 kHz)	0.2

distances. Third, the mechanical support of the IAPS transformer and the circuitries needs to be designed so that the IAPS can be properly mounted in the MV converter.

E. Insulation Material

The widely used potting material for MV components includes epoxy, silicone elastomer, and silicone gel. There are three critical characteristics. First, the electrical strength needs to be high, so that the insulation capability can be high with constant distance, or the distance can be reduced to achieve the same insulation capability. Second, the viscosity needs to be low so that deairing can be easily conducted in the vacuum, which is an important process to achieve PD-free performance. Third, the dielectric constant needs to be low so that the coupling capacitance can be minimized. Some other characteristics, such as thermal conductivity, also need to be considered, but they may not be critical for the IAPS since the loss of the transformer is usually low.

The main characteristics of three insulation material examples, epoxy 50-3170, silicone elastomer TC4605, and Silicone gel SilGel 613, are listed in Table I. Among them, SilGel 613 is a better choice because of its high electrical strength, low viscosity, and low dielectric constant, and thus is used in the following design.

V. DESIGN EXAMPLE

Iterations are needed to achieve the design requirements and minimize the size. To simplify the design, some variables, such as the topology, controller IC, insulation material, core type, and winding structure, are determined at the beginning. The main design parameters are the switching frequency, core size, the distance between windings, and the distance between the winding and the core. To minimize the whole size, the smallest core should be used. Meanwhile, the insulation capability, efficiency, load regulation, and coupling capacitance requirements should be achieved. The main design procedure is shown in Fig. 16. The switching frequency is first assumed. Then, the smallest core is selected, followed by the transformer electrical design and converter power loss estimation. If the converter efficiency does not meet the requirement, a smaller switching frequency or a larger core will be considered to reduce the loss. After the efficiency requirement is achieved, the distance between the two windings and the distance between the winding and the core are determined to meet the load regulation, coupling capacitance, as

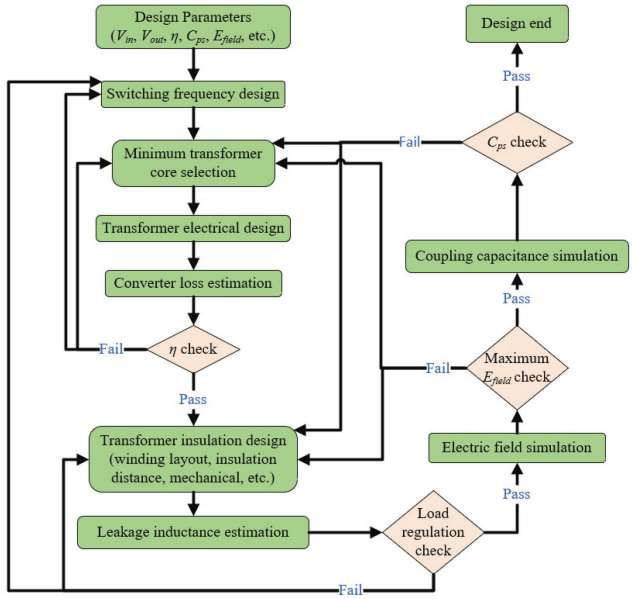


Fig. 16. IAPS optimal design procedure to realize small size and also meet the requirements.

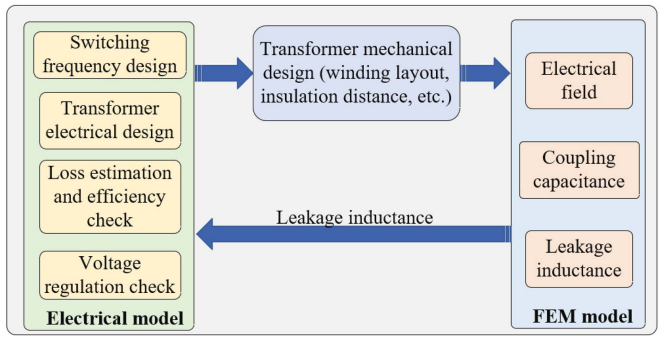


Fig. 17. IAPS design diagram.

well as electric field requirements. A smaller distance between windings helps to reduce the leakage inductance and therefore achieve better load regulation. The switching frequency affects the voltage drop on the leakage inductance and so as the output voltage, so the switching frequency may need to be adjusted to meet the load regulation requirement. A large distance between the windings and the core leads to a small coupling capacitance and small electric field, however, the size of the core is also increased. Therefore, after meeting all the requirements, the result is the design with a minimal core, and the total IAPS size is minimized.

To realize the optimal design procedure, the state-space-based electrical model and FEM simulation model are developed. As shown in Fig. 17, the electrical model evaluates the efficiency and load regulation based on the electrical design parameters and the leakage inductance from the FEM model simulation, and the FEM model evaluates the electrical field, coupling capacitance, and leakage inductance. Also, the transformer electrical design results provide inputs for its mechanical design, and the mechanical design results are the input of the FEM model.

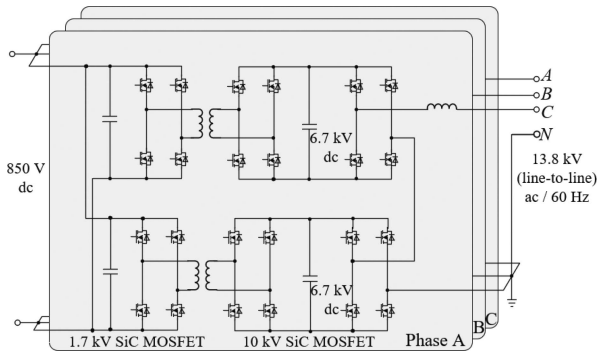


Fig. 18. MV PCS converter topology.

TABLE II
DESIGN REQUIREMENTS OF THE MV IAPS

Parameter	Value	Parameter	Value
Input voltage	24 V	Output voltage	24 V
Maximum output power	2.5 W	Coupling capacitance	<1.5 pF
Efficiency	≥80% at [2W, 2.5W] output range	Insulation requirement	PDIV ≥ 10 kV rms
Load regulation	≤26 V at 20% load (0.5 W) ≥22 V at 100% load (2.5 W);		

In the following subsections, the final MV IAPS design results for a 10 kV SiC MOSFET-based 13.8 kV/100 kW three-phase converter are discussed.

A. Design Requirements

The three-phase four-wire MV dc/ac converter topology is shown in Fig. 18. The design requirements of the MV IAPS are summarized in Table II. The input and output voltages are both 24 V. The maximum output power is 2.5 W, and the coupling capacitance needs to be smaller than 1.5 pF to limit the CM current caused by the high dv/dt. The efficiency at 2 to 2.5 W output needs to be higher than 80%. Each phase has two MV dc links, and each is rated at 6.7 kV. Considering ±5% voltage ripple, the maximum voltage stress applied on the MV IAPS is 14 kV based on (1). Therefore, the MV IAPS needs to be PD free at least 14 kV peak (10 kV rms). Since there are other nonisolated dc/dc converters on the GD board to convert the 24 V to +30, +15, and −5 V, the IAPS output voltage is allowed to vary within [26 V, 22 V] in the load range of [20%, 100%].

B. Electrical Design Results

The electrical design results are summarized in Table III. The Texas Instruments synchronous buck/fly-buck converter IC LM5160 is utilized for the primary-side control and regulation. The integrated FETs, soft startup, undervoltage lockout, and peak current limiting protection of the IC provide a simple design. The primary-side voltage is determined at 10.85 V. Ferrite core B64290A0719X049 is selected considering its dimensions, permeability, and core loss. The primary-side and secondary-side winding turns are 5 and 12, respectively, which results in a primary-side magnetizing inductance of 28.3 μH. The switching frequency is determined at 330 kHz considering the efficiency and load regulation, and AWG 32 magnetic wire is used.

TABLE III
ELECTRICAL DESIGN RESULTS OF THE MV IAPS

Parameter	Value	Parameter	Value
IC	LM5160	V_{out1}	10.85 V
Core	B64290A0719X049 (r_{in}=13.7 mm; r_{out}=22.1 mm)	Primary winding	Five turns
Secondary winding	12 turns	Magnetizing inductance (primary side)	28.3 μH
Switching frequency	330 kHz	Magnetic wire	AWG 32

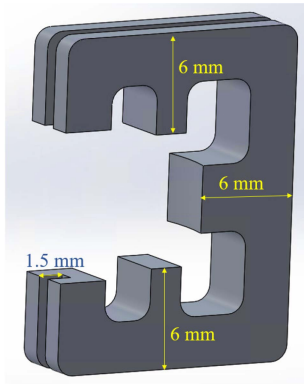


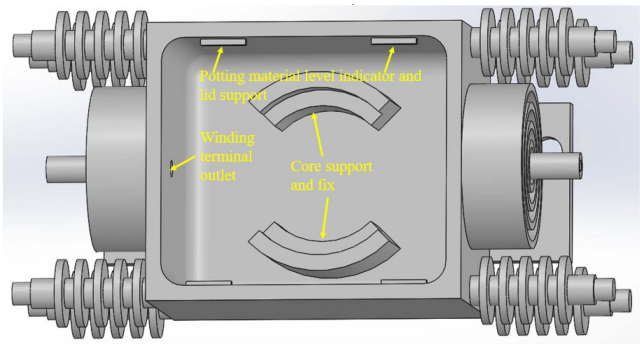
Fig. 19. Transformer bobbin design.

C. Transformer Mechanical Design

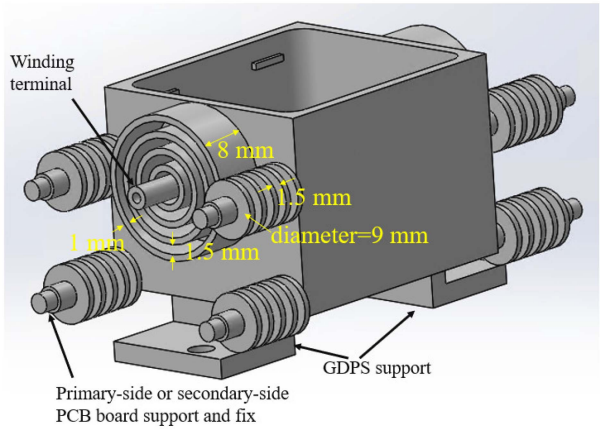
To achieve the insulation and minimize the coupling capacitance, $d_{sc} = d_{pc} = 4.5$ mm, and the distance between the two windings is around 4 mm. Considering the flexibility of the design, the transformer bobbin, lid, and enclosure are all three-dimensional (3-D) printed with Nylon 12.

The transformer bobbin shown in Fig. 19 is designed. It can be directly clipped on the core, and a thin layer of epoxy glue can be used to enhance the connection.

Fig. 20(a) shows the top view of the designed transformer enclosure. A support structure is designed in the center to support and fix the core. The primary-side and secondary-side windings are led out from two opposite sides. On two inner side panels, support structures are designed for the lid. They are also used as an indicator to ensure sufficient potting material. The side view of the enclosure is shown in Fig. 20(b). Four standoffs are designed on the two sides, respectively, to support and fix the primary-side and the secondary-side PCB boards. Based on IEC 61800-5-1: 2007, the required creepage distance for 14 kV, considering pollution degree 2 and material group I (nylon 12: comparative tracking index is 600), is 70 mm. Bushing design is adopted on the PCB standoff and surrounding the



(a)



(b)

Fig. 20. (a) Top view and (b) side view of the transformer case design.

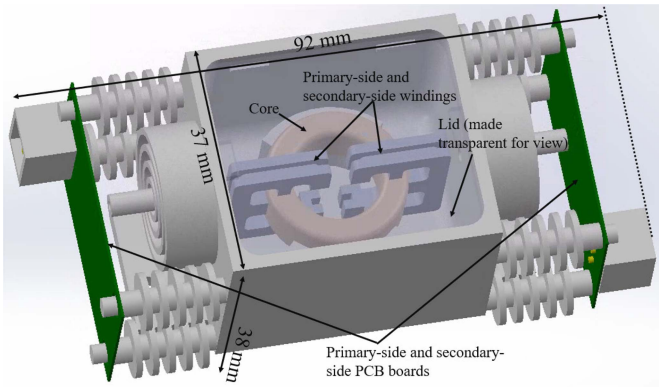


Fig. 21. IAPS assembly.

terminal outlet, achieving a minimum creepage distance of 133 mm.

The assembly of the IAPS, including the bobbins, core, enclosure, enclosure lid, and PCB boards, is shown in Fig. 21. The IAPS dimensions are 92 mm × 37 mm × 38 mm (3.82 inches × 1.46 inches × 1.50 inches).

D. Electric Field

The electric field of the IAPS is estimated with Ansys/Maxwell3D with electrostatic simulation, as shown in

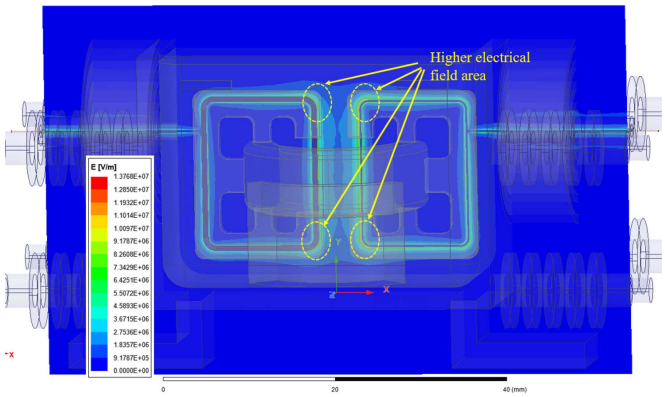


Fig. 22. Electrical field simulation results of the designed IAPS.

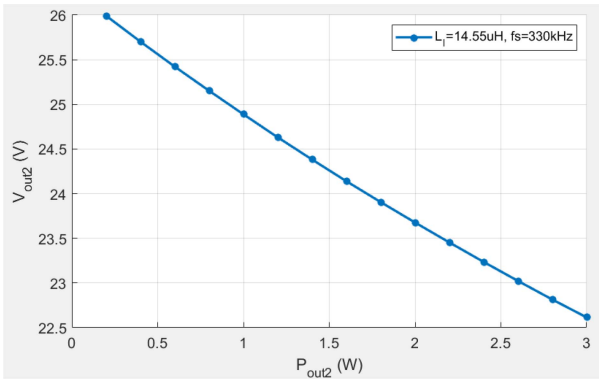


Fig. 23. Load regulation solved with the electrical model.

Fig. 22. The winding corner areas between the primary-side winding and the secondary-side winding have a higher electrical field than other locations. The maximum electrical field is less than 14 kV/mm, which is much lower than the dielectric strength of the insulation material (23 kV/mm).

E. Estimated IAPS Performances

The coupling capacitance and the leakage inductance are estimated to be 1.1 pF and 14.55 μH (secondary side), respectively, based on the Ansys Maxwell3D simulation results. With this leakage inductance, the load regulation curve is drawn in Fig. 23, which meets the design requirements. The efficiency curve is shown in Fig. 24, which also meets the requirement.

VI. Experimental Results

The IAPS designed in Section V is built, and the picture is shown in Fig. 25. It is potted with SilGel 613 in the vacuum process. It is fully tested, as discussed in following subsections.

A. Transformer Test

First, the coupling capacitance of the IAPS transformer is measured with an impedance analyzer E4990A. The impedance analyzer is set in the capacitance–resistance measurement mode, the sweep frequency range is from 10 kHz to 20 MHz. Before

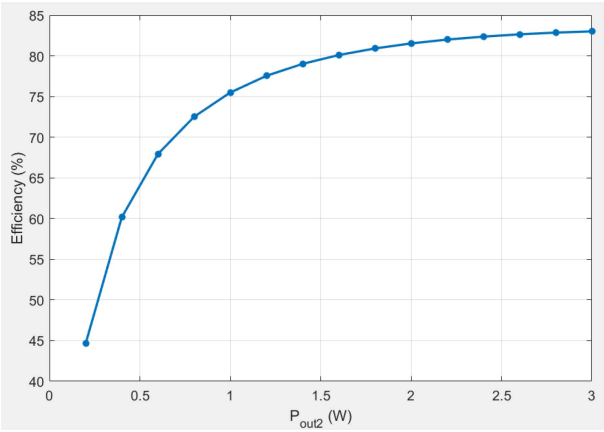


Fig. 24. Estimated efficiency curve.

Fig. 25. Picture of the built IAPS.

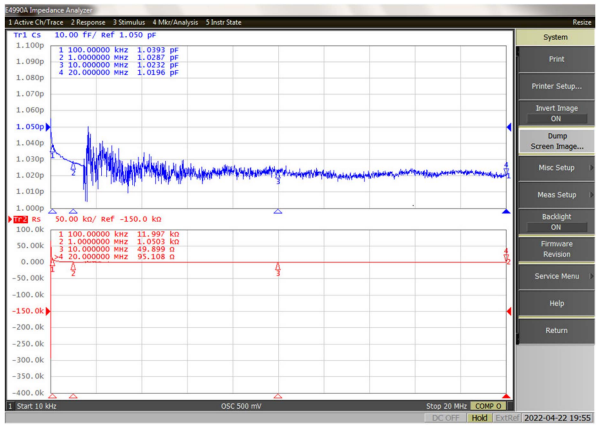
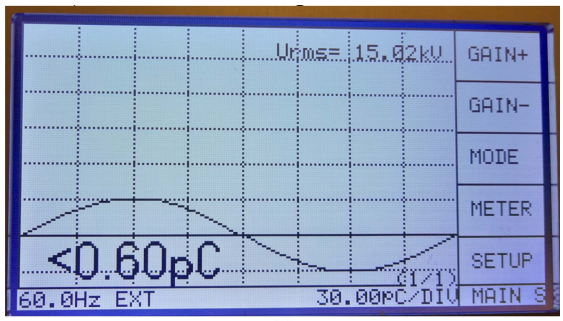
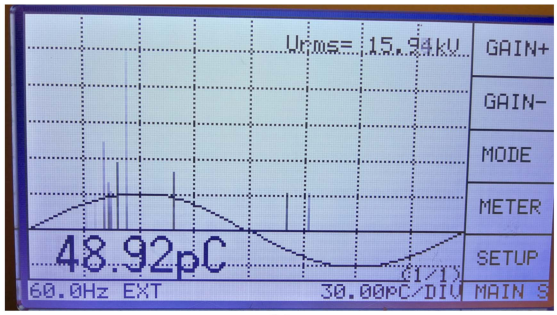


Fig. 26. Measured coupling capacitance of the IAPS transformer.

tests, the equipment is calibrated with short connection and open connection individually. Since the transformer winding terminals are short and cannot be connected to the impedance analyzer directly, two short electrically conductive pins are, respectively, used to connect the transformer's primary and secondary winding terminals to the two connectors of the impedance analyzer. The capacitance only with the two pins is measured, which gives the impact from the two pins. Then the transformer is connected, and the capacitance is measured again. Since the capacitance introduced by the two short pins is quite small (∼20 fF, 0.02 pF), and therefore it is neglected. The measured transformer's coupling capacitances in terms of different frequencies are shown in Fig. 26, and the coupling capacitance is around 1.03 pF.



(a)



(b)

Fig. 27. PD test waveforms of the IAPS transformer with (a) PD free and (b) 48.9 pF PD level.

Then, the PD performance of the transformer is tested with PHENIX PD tester 6CP30/15-3, which can generate a 60 Hz high-voltage waveform up to 30 kV rms. Although the real voltage stress on the transformer is high-frequency high *dv*/*dt* voltage, using a 60 Hz PD tester is still a good and simple choice since a PD tester for high-frequency and high *dv*/*dt* applications is not commercially available yet. Moreover, the PDIV and the PD extinction voltage (PDEV) tested with the 60 Hz PD tester are close to the values with high-frequency and high *dv*/*dt* tester. As discussed in [27], high-frequency high *dv*/*dt* PWM waveforms lead to a slightly lower PDIV (7 vs. 7.6 kV) but a much higher PD charge than that with 60 Hz voltage. In addition, the PDEV of the high-frequency voltage case is close to that of the 60 Hz voltage case. Therefore, using PDIV and PDEV as the insulation capability can ensure the insulation performance of the transformer in real applications.

As shown in Fig. 27(a), the transformer is PD free (<0.6 pC) at 15. 02 kV rms, which corresponds to 21.2 kV peak. It has a PD level of 48.92 pC at 15. 94 kV rms, as shown in Fig. 27(b). The maximum voltage stress on the IAPS transformer is the total dc-link voltage, whose maximum voltage is 14 kV dc, and it corresponds to 10 kV rms. Therefore, the designed transformer meets the insulation design requirement (PD free at 10 kV rms) and has a 50% margin.

B. IAPS Performance in Half-Bridge Test

Two IAPS are used to supply two 10 kV SiC MOSFETs in a half-bridge circuit, and an LR load is connected between the half-bridge and the middle point of the dc-link. The dc-link voltage is 6.7 kV, and it is supplied by an MV dc power supply. Waveforms of the low-side device's gate-source and drain-source voltages,

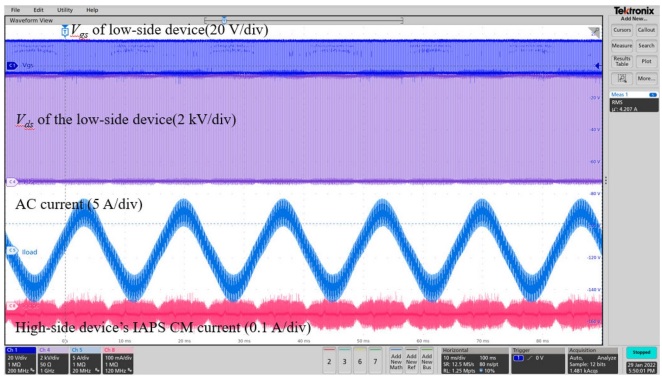


Fig. 28. Voltage and current waveforms in the MV half-bridge test.

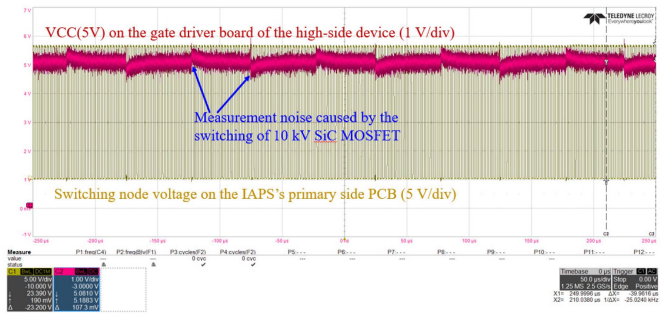


Fig. 29. Waveforms of the high-side gate drive board voltage and IAPS primary-side PCB voltage.

the ac side current, and the high-side IAPS's CM current are shown in Fig. 28. The IAPS's CM current is measured with a current probe by clamping both the positive and negative input power wires. The CM current peak is about 60 mA, and the *dv/dt* of the 10 kV SiC MOSFET is around 56 kV/ns, which verifies that the coupling capacitance is around 1 pF.

As shown in Fig. 29, the 5 V power rail on the high-side GD board is stable, and the voltage spikes are measurement noise caused by the switching transient of the 10 kV SiC MOSFET. Also, the switching node voltage of the IAPS's primary-side PCB is stable, which means the IAPS is not impacted by the CM current.

C. IAPS Test in the Three-Phase Converter

A total of 55 IAPS are built following the same design for the three-phase 13.8 kV/100 kW converter. Their coupling capacitances, measured with impedance analyzer E4990A, are shown in Fig. 30. Most of them have a coupling capacitance of around 1.05 pF, and the minimum is 1.03 pF. Since the windings are made by hand, the tightness of wiring could be different, which results in different distances between windings. Besides, the locations of the wire inside the bobbin slot are slightly different. These could result in different coupling capacitances.

The PD test results are shown in Fig. 31. The PDIV values are all above 15 kV rms, and the lowest PDEV level is around 14.7 kV rms. The different insulation performances could be caused by the different quality of deairing and the windings distances.

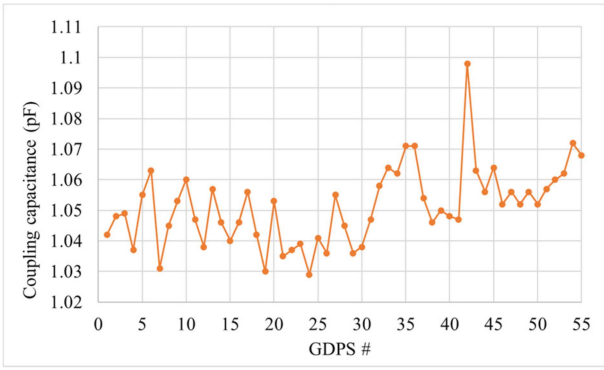


Fig. 30. Coupling capacitance of the 55 IAPS at 1 MHz.

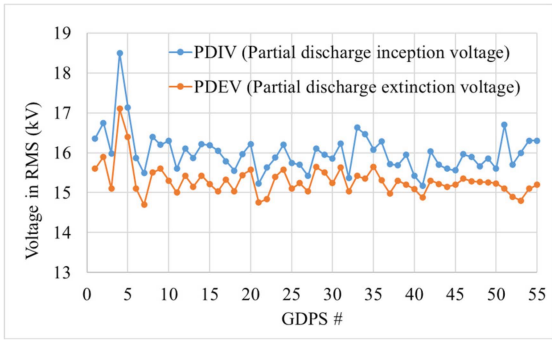


Fig. 31. PD results of 55 IAPS.

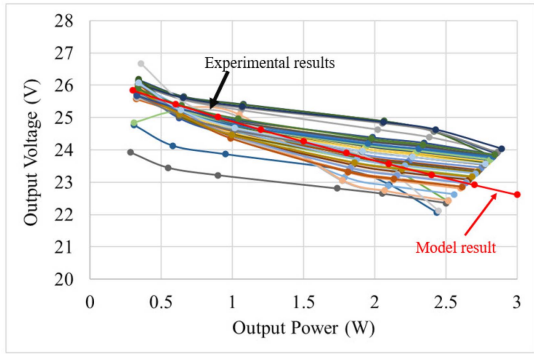


Fig. 32. Tested load regulation curves of 55 IAPS and the model results.

The comparison between the tested load regulation curves of the 55 IAPS and the model-predicted curve is shown in Fig. 32. Because of the leakage inductance, the voltage drop is relatively large. However, this still meets the design requirements. Because there are other nonisolated dc/dc converters on the GD board, which convert the output of the IAPS to +15, +5, and −5 V, respectively. These nonisolated dc/dc converters stabilize the voltage on the GD board, and they have a large input voltage tolerance ($\geq \pm 10\%$). In addition, the static power consumption (without high-frequency switching) of the GD circuit is around 1 W. With high-frequency switching, the power rating is between 1 and 1.5 W. Therefore, the actual IAPS output voltage change in the real converter is quite small (<0.5 V, 2%), and the isolated

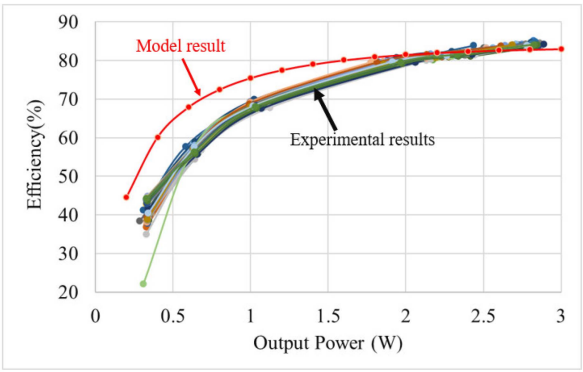


Fig. 33. Tested efficiency curves of the 55 IAPS and the model estimated curve.

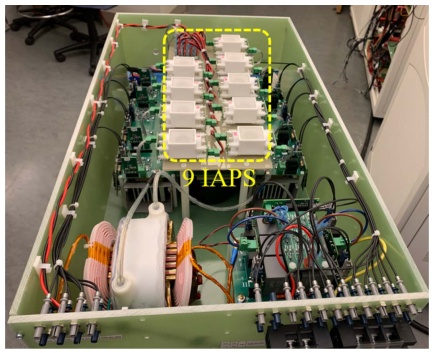


Fig. 34. Picture of one power unit.

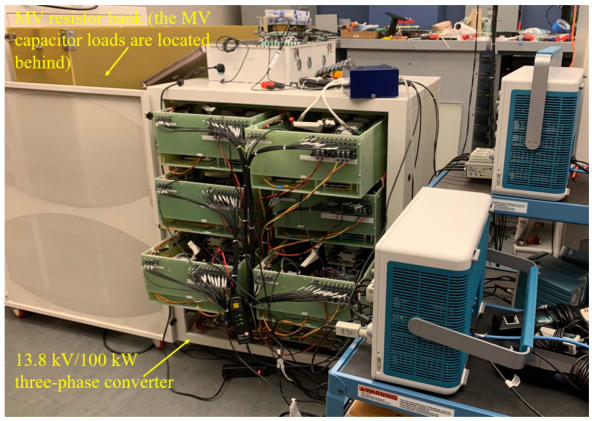


Fig. 35. Picture of the three-phase converter test setup.

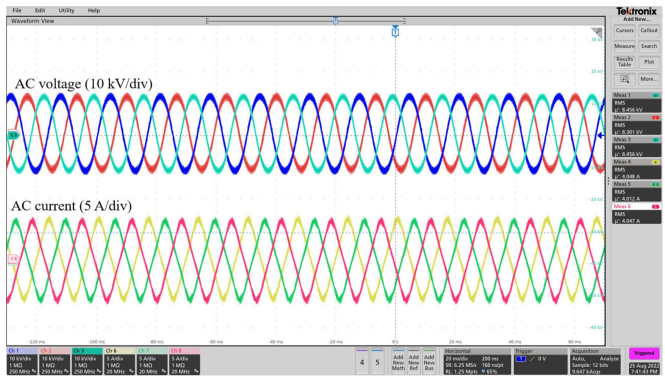


Fig. 36. MV ac side voltage and current waveforms at 13.8 kV/100 kVA.

power supply is good to use for the GD system. Moreover, the comparison between the tested curves and the model curve shows that the model-predicted curve matches most of the tested IAPS curves. The tolerance of resistors for the feedback circuit and the switching frequency and the winding turn error caused by hand-made lead to the curve difference among the 55 IAPS.

To test the efficiency under different output power conditions, different power resistors are used as the load individually. The IAPS is supplied by a Keithley 2230-30-1 dc power supply, which has an output voltage accuracy of 0.03% and current accuracy of 0.1%. The input power is calculated based on the voltage and current reading of the dc power supply, and the output power is calculated based on the output voltage, which is measured with a Fluke 117 multimeter (60 V range, 0.01 V accuracy) at the output terminal of the IAPS, and the load resistance measured with the same multimeter (600 Ω range, 0.1 Ω accuracy). Therefore, the theoretical accuracy of the power measurement is around 0.14%. However, the main limitation of the efficiency measurement is that all measurement equipment is not calibrated before tests, and therefore, theoretical accuracy may not be achieved. The tested efficiency curves are shown in Fig. 33, together with the model estimated one. It is shown that all 55 IAPS has an efficiency of $\geq$80% at the [2 W, 2.5 W] range. There is some discrepancy between the model estimated curve and the tested curves at the low power range. This could be due to the deviation of the core loss estimation and the fly-buck IC loss.

Modular design is adopted in the 13.8 kV/100 kW three-phase converter, and one power unit is shown in Fig. 34. It consists of a dual active bridge based dc/dc stage and an H-bridge in the dc/ac stage, as shown in Fig. 18. Therefore, each phase has two power units, and the three-phase converter has six power units. In each power unit, there are 9 IAPS, supplying 810 kV SiC MOSFETs and 1 dc-link voltage sampling. The three-phase converter is tested with a three-phase R-C load at the MV ac side, and the converter is supplied from the LV dc side with an LV dc power supply.

The setup picture is shown in Fig. 35. The converter is tested from 5% of the rated voltage to the rated voltage with a voltage step of around 12%. At each voltage level, the test was conducted for around 10 min. The ac side voltage and current waveforms at the rated voltage (13.8 kV, line-to-line) and power (100 kVA) are shown in Fig. 36. In addition, other tests under the rated voltage condition are also conducted to verify the converter design. The longest single test is more than 30 min to verify the thermal of magnetics, and the accumulated time is more than 10 h, which verifies the long-term reliability of the IAPS.

D. Comparison With Existing Work

The comparison between this article and some existing research work and the commercial product [28] is shown in

TABLE IV
COMPARISON AMONG THE COMMERCIAL PRODUCT, EXISTING WORK, AND THIS WORK

Developer	Topology	Pmax	Peak eff	Insulation material	PDIV (rms)	Coupling capacitance	Size
Product ISO5125I-120 [28]	NA	5 W	NA	NA	≥9.4 kV	4 pF	411 cm^3
ETH, 2015 [17]	LLC	30 W	NA	Air	15.9 kV	NA	>1099 cm^3
ABB, 2016 [24]	Wireless power transfer	250 W	86%	Polyurethane (PU)	>100 kV	NA	NA
OSU, 2016 [19]	Power over fiber	0.5 W	24%	Fiber	>20kV	0	NA
ETH, 2018 [23]	Series-series compensated resonant converter	2 W	NA	Silicone elastomer, TC 4605 HLV	No PD test 20 kV dc hi-pot	4.1 pF	NA
GE, 2018 [16]	Full-bridge resonant converter	30 W	NA	Air	NA	5 pF	NA
NCSU, 2019 [9]	Single active bridge (SAB)	NA	NA	Air	No PD test 20 kV dc hi-pot	2.5 pF	~295 cm^3
NCSU, 2019 [14]	NA	10 W	NA	Air	7.5 kV	1 pF	188 cm^3
UTK, 2020 [20]	PSR-flyback	2.4 W	80%	Silicone gel 613	10 kV	1.85 pF	465 cm^3
CPES, 2020 [13]	LCCL-LC	10 W	86%	MV cable and air	8 kV	1.67 pF	NA
UT Austin, 2020 [12]	LLC	10 W	72%	Air	4.6 kV	3 pF	NA
NTNU, 2020 [18]	LLC	15 W	81%	FR4	NA	7-18 pF	NA
CPES, 2021 [11]	Wireless power transfer	120 W	92.78%	air	27 kV	2.76 pF	NA
UT Dallas, 2021 [21]	Wireless power transfer	1.8 W	49 %	Epoxy and air	NA	2.29 pF	NA
CPES, 2022 [10]	LCCL-LC	20W	NA	Silicone gel 612	11.6 kV	2.27 pF	55 cm^3 (only transformer)
FSU, 2022 [22]	Class-E resonant flyback	1.67 W	76%	Silicone gel, RF PCB	16.4 kV	5.85 pF	NA
NCSU, 2022 [15]	Series-series compensation circuit	20 W	77.1%	Rubber tape and air	20.6 kV	2.1 pF	~411 cm^3
UTK, 2022 (This work)	**PSR-flybuck**	**2.5 W**	**85%**	**Silicone gel 613**	**≥15 kV**	**1.03 pF**	**129 cm^3**

Table IV. The coupling capacitance of the designed IAPS is one of the smallest two, which reduces the efforts for CM noise immunity design and helps to reduce the power loss caused by parasitic capacitances [29]. In addition, this article shows better insulation capability than most of the existing work, and the overall IAPS size is also smaller than that of the existing designs, which have their sizes provided, and the commercial product. Two existing designs have a higher PDIV and reasonable coupling capacitance, but their volumes are much larger than that of the proposed design—although their exact volume values are not given.

VII. CONCLUSION

This article proposes the design of MV IAPS to achieve high insulation capability, ultra-low coupling capacitance, and small size. The topology considerations are first discussed, and the PSR flybuck is less sensitive to CM current than the PSR flyback converter. Then, the flybuck converter state-space model is adopted as the electrical design tool, and the FEM method is used to do the transformer mechanical design considering the leakage inductance, coupling capacitance, and electrical field. To reduce the coupling capacitance, the winding turns are combined together, which significantly reduces the effective area between the winding and the core and between the two windings. The 3-D printed transformer enclosure is designed to maintain the inner insulation distances between the winding and the core and the outside creepage distance. Also, a compact connection between the primary-side and secondary-side PCBs and the transformer is designed to shrink the overall IAPS size. The IAPS for a 10 kV SiC MOSFET-based 13.8 kV/100 kW three-phase converter is designed following the design considerations. They are tested to have a PDIV higher than 15 kV rms, coupling capacitance of 1.03 pF, and size of 129 cm^3, which are superior to the commercial product and the existing research design. Also, the designed IAPS is fully tested in the three-phase converter test with the rated voltage and power rating, i.e., 13.8 kV/100 kVA.

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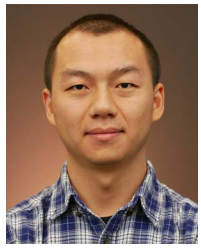

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