An Ultra-Light Tightly-Integrated Modular Aviation Transportation Enabling Solid-State Circuit Breaker (ULTIMATE-SSCB)

Project Lead: Fred Wang (UTK), Kevin Bai (UTK), Zheyu Zhang (RPI), Ruirui Chen (UTK) **Graduate Students and Research faculty/associates:** Jimmy Yang (UTK)
Project Duration: 7/2021 – 6/2025
Funding Source: ARPA-E

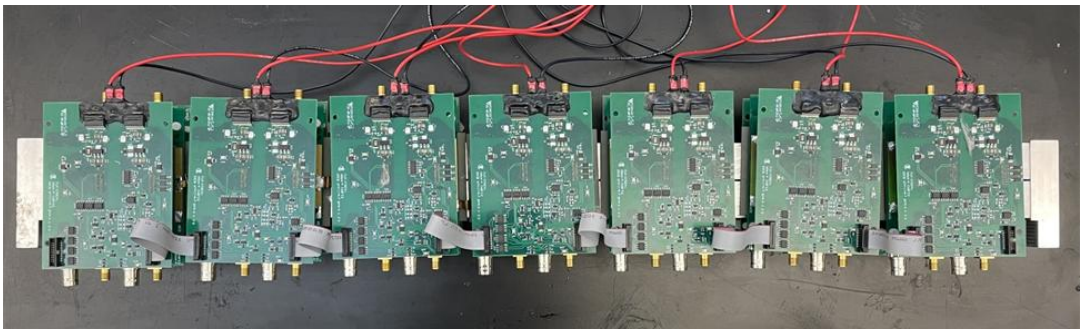
Summary

The project aims at developing and testing in simulated flying environment an ultra-light tightly-integrated modular aviation-transportation enabling solid-state circuit breaker (ULTIMATE-SSCB). The proposed ULTIMATE-SSCB will meet several objectives important for future electrified aircraft propulsion (EAP) systems: extremely light, efficient, fast, reliable, suitable for future medium voltage EAP system at >10 kV DC, taking advantages of cryogenic cooling enabled by liquified natural gas (LNG) or liquid hydrogen fuel of future EAP system. The developed SSCB will be highly flexible with modular structure, intelligent and easy for protection coordination and system integration, with built-in directional function, and current limit function.

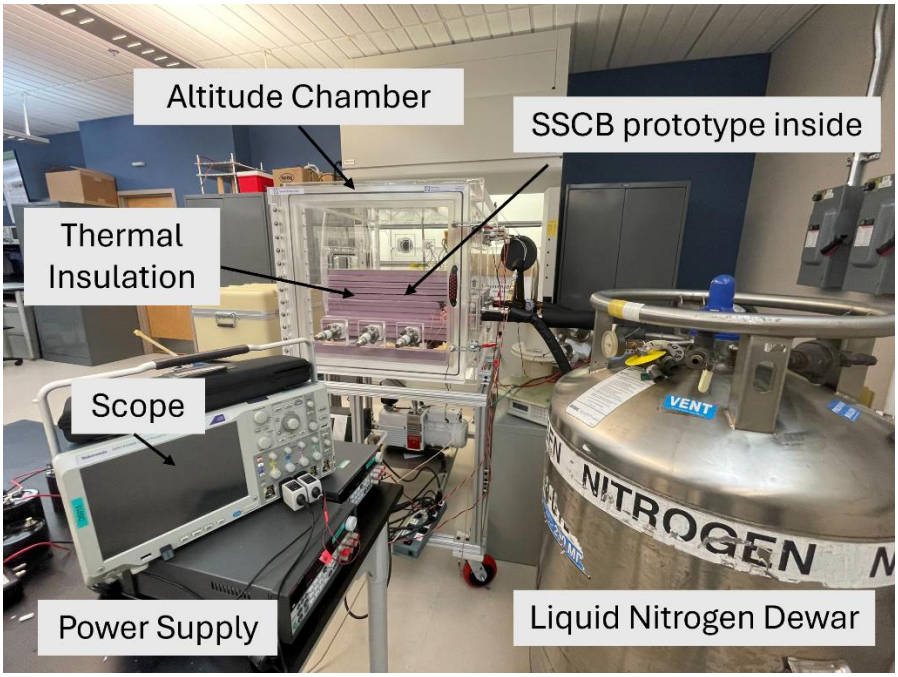
In phase I of the project, the team identified the specification and requirements of the 10 kV, 100A SSCB and completed conceptual design of the SSCB using cryogenically cooled GaN devices and key components testing. The SSCB is designed to interrupt up to 10x current during fault. Design of modularized SSCB, sensors, intelligent gate driver, control and communication strategy have been developed. A notional electrified aircraft propulsion architecture is identified and investigated with simulation to determine capability requirement of SSCB and to validate the protection and co-ordination strategy.

In phase II of the project, the team has developed a 750V, 100A SSCB module that can be used in 5 kV unipolar or a 10 kV bipolar MVDC system. A series combination of 14 such modules will meet the requirements of 10 kV, 100A SSCB for future EAP system. A liquid Nitrogen based cooling system is developed and the module is successfully tested to interrupt a fault current of 1 kA. A cryogenic packaging for the module is developed and the module is successfully achieved high efficiency (>99.96%), compact (255.22 kW/L), light(350.95 kW/kg) and highly integrated with embedded functions including gate-drive based protection and current limiting. The module is also designed for high-altitude operation and successfully tested in an emulated high-altitude test setup.

In phase III of the project, the team has constructed the 5kV, 100A SSCB prototype using 7 of 750V, 100A SSCB modules. The prototype successfully interrupted 10X fault current (1kA) and achieved >99.96% of the efficiency with cryogenic cooling. The prototype also successfully passed the insulation test in the simulated high-altitude environment with cryogenic cooling. The 5kV prototype is verified to withstand 8 kV at emulated 40,000 ft environment.



(a)



(b)

Figure 1: (a) 5kV, 100A prototype, (b) High altitude test setup

A UNIVERSAL (Ultrafast, Noise-Immune, Versatile, Efficient, Reliable, Scalable, and Accurate Light-controlled) Switch Module

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Graduate Students and Research faculty/associates: Yang Xu (UTK), Xingyue Tian (UTK), Samuel Klein (UTK), Shahabuddin Khan (RPI), Yongji Wu (Clemson), Nicholas Tomlinson (Clemson), Haonan Song (Lehigh)

Project Duration: 5/2024 – 5/2027

Funding Source: ARPA-e

Summary

This project aims to develop and test an ultrafast, noise-immune, versatile, efficient, reliable, scalable, and accurate light-controlled (UNIVERSAL) switch module. The proposed UNIVERSAL switch (US) module will be designed to provide fast protection meeting several key performance targets: 1) 20 kV/250 A ratings and LEGO-like scalability for higher voltage and current ratings. 2) 10X peak current capability and >99.9% efficiency using wide bandgap power semiconductors. 3) EMI noise-immune design with gate driving and sensing via optical means. 4) 500 V/ns and >200 A/ns ultrafast triggering slew rates. 5) ⩾30,000 cycles lifetime operation and (N-2) fault-tolerant capability at full power using natural cooling and a redundant submodule design.

The project has three budget periods, each planned for 12 months. Tasks for the first budget period have been successfully completed. In Year 2 of the project, the primary focus will be on the design and testing of the US module's voltage and current sensors. The electrical and mechanical designs of the US module will be verified, and the designed components and key functional blocks will be experimentally integrated and validated within the SM, encompassing all electrical, thermal, mechanical, and optical aspects. The required SM-level di/dt and dv/dt performance targets will be achieved during this period. For the T2M activities, efforts will continue to refine the commercialization plan by mapping technical capabilities, identifying potential applications, and advancing the intellectual property strategy. The plan will be regularly updated to reflect progress, including engagement with prospective customers and reporting to ARPA-E on customer requirements and market insights.

The team is currently continuing low-power functional testing of the SM and US module-level sensors to validate the analysis. In parallel, work progressed on fabrication of the optical power supply, and preliminary test results have been obtained. Assembly of the SM, integrating components provided by different project partner organizations, is ongoing, and dynamic testing of the quarter-SM has been completed. Under the Technology-to-Market (T2M) activities, application scenario analysis was continued, demonstrating the feasibility of deploying the US module in next-generation power architectures, with specific emphasis on medium-voltage (e.g. 13.8 kV AC) data center distribution systems.

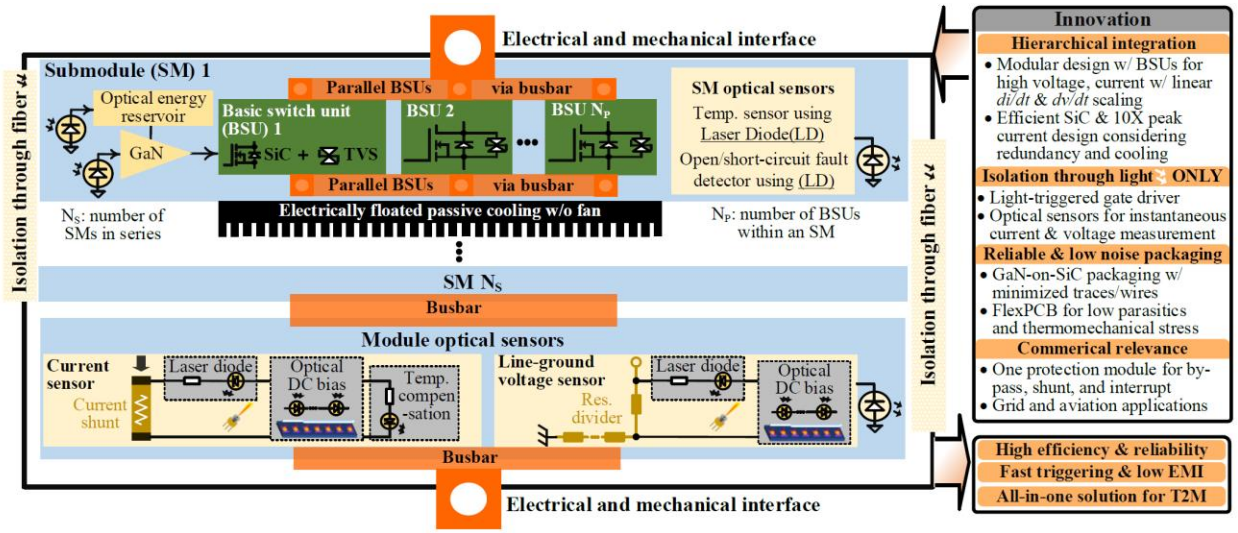

Fig. 1. Proposed US module with optical gating & sensing, passive air-cooling, & electrical/mechanical connection

SiC Based Modular Transformer-Less MW-Scale Power Conditioning System andController for Flexible Manufacturing Plants

Project Lead: Fred Wang (UTK), Yilu Liu (UTK), Leon Tolbert (UTK)， Kevin Bai (UTK), Ruirui Chen (UTK)

Graduate Students and Research associates: Yang Xu (UTK), Jingxin Wang (UTK), Zihan Gao (UTK), Min Lin (UTK)

Project Duration: 10/2020 – 12/2025

Funding Source: DOE

Summary

The objective of this project is to develop a 10 kV SiC MOSFET-based 1 MW bi-directional power conditioning system (PCS) for manufacturing plants, consisting of back to back 13.8 kV AC/DC converetrs and a 200 kW isolated DC/DC converter connected to the PCS MV DC bus. The proposed PCS converter will meet performance targets including >99.4% power efficiency, <0.3 m^3/MW volumetric density, >10% dispatchability, <$30/kW cost (excluding SiC die cost), > 10 years lifetimes, 300 Hz voltage control bandwidth and >1 kHz current control bandwidth, and grid supporting functions.

Fig. 1-1 shows the PCS architecture. It serves as the interface between a 13.8 kV AC distribution grid and a manufacturing plant power system to enable various FMP architectures. With the PCS, an FMP power system can be operated as one or more AC asynchronous microgrid. With DC/DC converters ports interfacing directly with DC-fed loads and source, the FMP can also be operated as one or more hybrid AC asynchronous and DC microgrids. BP1 of this project has been completed in 2022, which focus on the design of this PCS and FMP controller. BP2 of this project has been completed in 2024, and the focus is to build and test one phase of the designed 1 MW back to back AC/DC/AC converter and one module of the designed 200 kW DC/DC converter.

During 2025-2026, all four 50 kW modules of the 10 kV SiC discrete device based 200 kW DC/DC converter are built and tested at rated volatge and power. All three phases of the 10 kV SiC module based 1 MW eight-level flying capacitor DC/AC converter are built. One phase-leg of the new Powex packaged 10 kV SiC module based fivel-level flying capacitor DC/AC converter is built and tested to 23 kV rated voltage. The materials for building another two phase-legs are prepared. The PCS integration strategy with MV testing platform and testing scenarios are determined.

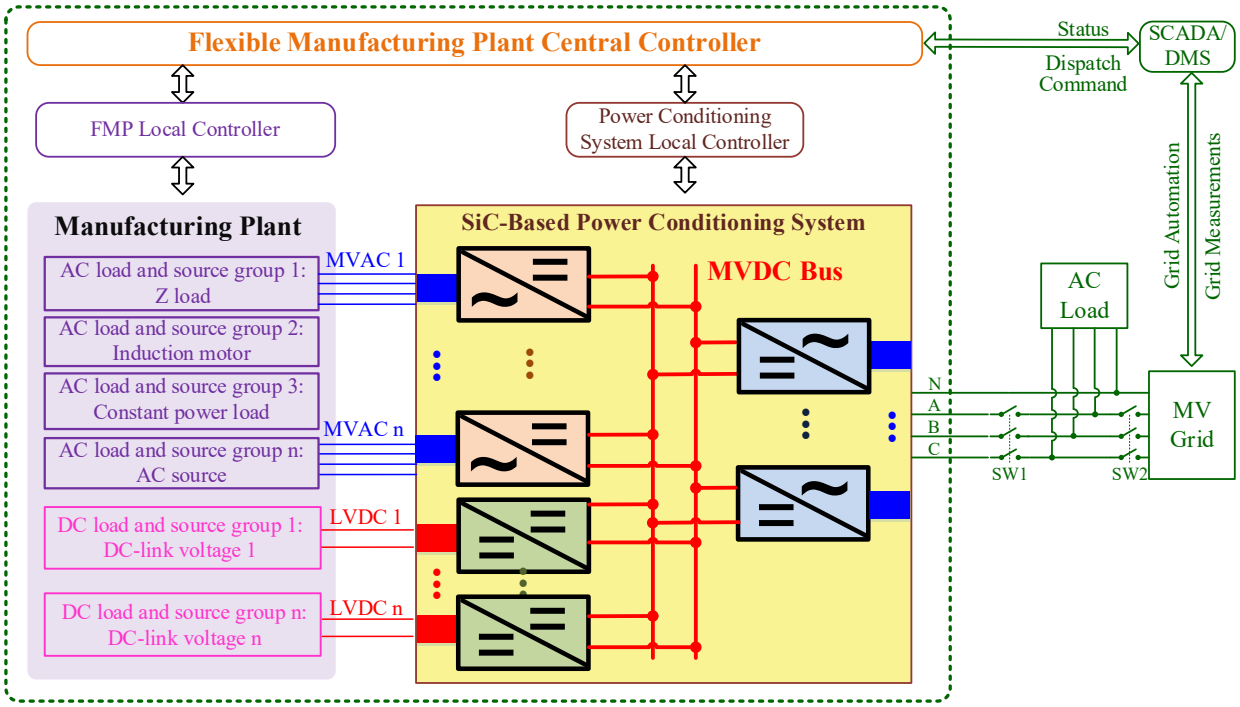

Fig. 1-1. PCS architecture for FMP system.

High Performance Isolated Dc/Dc Converter For Future Hvdc Data Center Application

Project Lead: Fred Wang (UTK) **Graduate Students and Research faculty/associates:** Yanda Lyu (UTK)
Project Duration: 10/2025 – 9/2026
Funding Source: ABB

Summary

The project focuses on developing a high-efficiency, high–power-density isolated DC–DC converter for next-generation HVDC data center systems. The converter operates from a high-voltage DC input and delivers a nominal low-voltage output with large voltage ratio, targeting at high efficiency, high power density, and good transient performance.

Multiple converter topologies were evaluated, with emphasis on efficiency, scalability, and implementation complexity. Among the candidates, the LLC resonant converter was selected due to its inherent soft-switching capability, reduced component count, and suitability for high-frequency operation, all of which support high efficiency and compact design.

To meet system-level voltage and power demands, a modular input-series-output-parallel (ISOP) architecture based on LLC converters was adopted. This approach enables effective handling of high input voltage while maintaining manageable device stress and supporting scalable power integration.

A central challenge in this work is maintaining output voltage stability during fast load transients, given the unregulated nature of the LLC converter working as a DC transformer. The project therefore investigates both control and design-level approaches to mitigate transient deviations while preserving efficiency.

The work will proceed toward prototype implementation and experimental validation, along with a systematic assessment of performance trade-offs to determine the suitability of the proposed architecture for future HVDC data center applications.