2022 IEEE Design Methodologies Conference (DMC) | 978-1-6654-7999-8/22/$31.00 ©2022 IEEE | DOI: 10.1109/DMC55175.2022.9906473

Broad-Scale Converter Optimization Utilizing Discrete Time State-Space Modeling

Jared A. Baxter and Daniel J. Costinett
The Bredesen Center
The University of Tennessee, Knoxville
Knoxville, Tennessee, USA
Email: jbaxte24@vols.utk.edu, daniel.costinett@utk.edu

***Abstract*—Schematic-level optimization and steady-state loss modeling play a vital role in the design of advanced power converters. Recently, discrete time state-space modeling has shown merits in rapid analysis and generality to arbitrary circuit topologies but has not yet been utilized under rapid optimization techniques. In this work, we investigate methods for the incorporation of rapid gradient-based optimization techniques leveraging discrete time state-space modeling and showcase the utility of the approach for use in the converter design process.**

I. Introduction

Currently the process of designing a power electronics converter is constrained by initial topology selection, analysis, and design. The design process of a power converter often utilizes several iterations of broad steady-state converter modeling or simulation of many converter topologies, discrete components, magnetics, and frequencies to achieve the goal performance, as shown in Fig. 1. The design begins with application-based specifications and constraints that should be adhered to in any viable design and objectives that dictate the relative merit of valid design candidates. Typical constraints include input and output voltage, current, and power levels, as well as physical restrictions such as the maximum size or height. Objectives are the metrics used to compare different designs if the constraints are met, such as efficiency, power density, or specific power. From the constraints and objectives, a set of possible topologies, operating methods, devices, and control strategies is analyzed to determine an optimal schematic-level design. The final design performance will be constrained by how broad the initial selections of topologies and devices are and the accuracy of the modeling and assessment of each design candidate. Within a reasonable design time and effort, this scope and accuracy are then determined by the speed and fidelity of the modeling and optimization framework used in the power converter design problem.

Recent work has shown that discrete time state-space modeling reduces simulation time while maintaining results with high fidelity [1], [2]. However, even with this decreased simulation time, design and optimization across many continuous variables and discrete topology/device selections can be complex and computationally expensive even with advanced computational power [3], [4]. Brute force approaches sweep

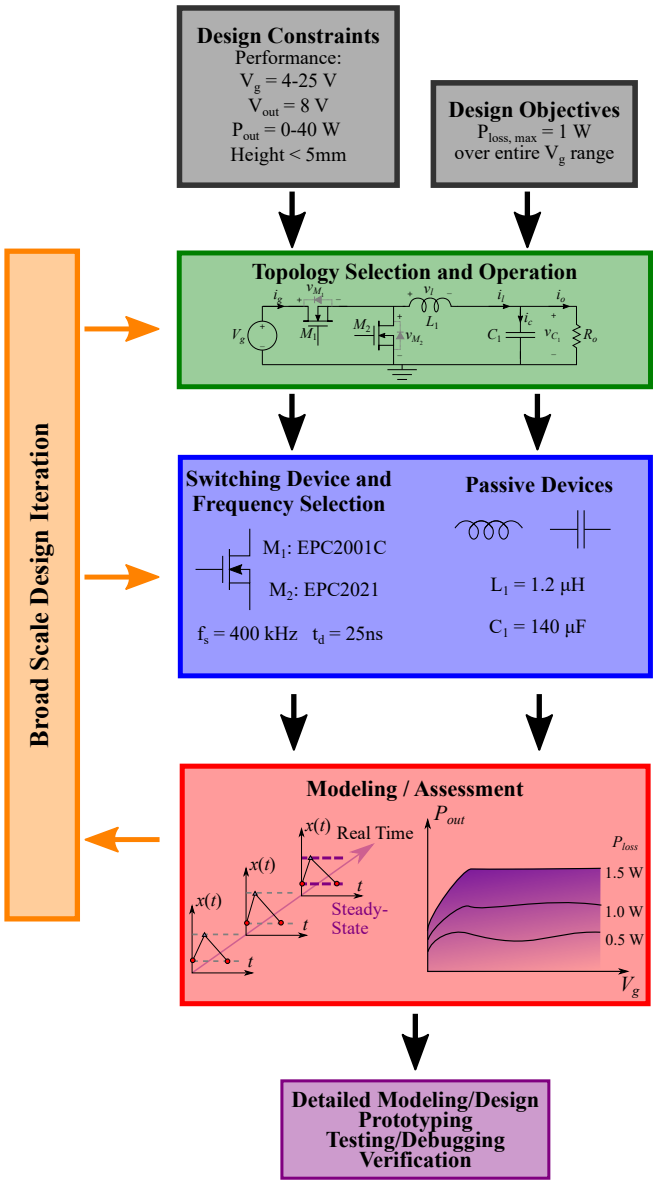


Fig. 1. Overview of the broad scale optimization process in the early design stage of power electronics.

978-1-6654-7999-8/22/$31.00 ©2022 IEEE

multiple parameters at a time through the design space, solving the converter performance under each combination, to find an optimal combination. While useful for understanding how a variable affects converter performance, this and related techniques are computationally taxing when used to optimize all the variables in a converter design. Metaheuristic techniques, such as genetic or particle swarm algorithms, are also very popular to optimize converters but may also be time-consuming for large-scale problems [5].

This work gives a framework to optimize converters utilizing rapid discrete time state-space modeling and adapting gradient optimization techniques for discrete component selection. The remainder of the paper is organized as follows. Section II reviews discrete time state-space modeling and its ability to rapidly model switching power converters. Section III provides an overview of the component selection method. Section IV demonstrates the utility of the design method through an experimentally-verified design optimization. Section V concludes the work.

II. Discrete Time State-Space Modeling

Discrete time state-space modeling is a generalized analysis framework for both steady-state and dynamic modeling of switched circuits [4], [6]–[10]. Switched mode power supplies are modeled using discrete time state-space equations, approximating the converter as a linear equivalent circuit within each switching interval i, defined by the state of each switching element,

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}_i \boldsymbol{x}(t) + \boldsymbol{B}_i \boldsymbol{u}(t) \tag{1}$$

$$\boldsymbol{y}(t) = \boldsymbol{C}_i \boldsymbol{x}(t) + \boldsymbol{D}_i \boldsymbol{u}(t), \tag{2}$$

where $\boldsymbol{A}_i$ and $\boldsymbol{B}_i$ are the constant state matrix and input matrix, respectively. During any interval, the solution for the state vector containing capacitor voltages and inductor currents is

$$\boldsymbol{x}(t) = \mathrm{e}^{\boldsymbol{A}_i t}\boldsymbol{x}(0) + \boldsymbol{A}_i^{-1}[\mathrm{e}^{\boldsymbol{A}_i t} - \mathbf{I}]\boldsymbol{B}_i \boldsymbol{u}, \tag{3}$$

assuming all input sources are constant and all $\boldsymbol{A}_i$ are invertible. Iterating through the different linear equivalent models captures the switching dynamic behavior of the converter. By solving the state-space equation over the set of linear equivalent circuits for a converter, the periodic steady-state solution is

$$\boldsymbol{X}_{ss} = \left[\mathbf{I} - \prod_{i=n}^{1} \mathrm{e}^{\boldsymbol{A}_i t_i}\right]^{-1} \times \sum_{i=1}^{n}\left[\left(\prod_{k=n}^{i+1} \mathrm{e}^{\boldsymbol{A}_k t_k}\right)\boldsymbol{A}_i^{-1}[\mathrm{e}^{\boldsymbol{A}_i t_i} - \mathbf{I}]\boldsymbol{B}_i \boldsymbol{u}\right], \tag{4}$$

where t_i is the length of the i^{th} interval.

Some limitations associated with discrete time state-space modeling have been addressed in prior work while continuing to show rapid modeling of switch-mode power supplies [1]. This includes eliminating the requirement that all state matrices $\boldsymbol{A}_i$ be invertible [8], [10], and determining the length of each switching interval t_i before solving (4) [2].

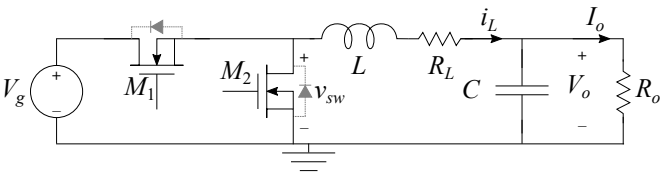


Fig. 2. Synchronous buck converter used in Fig. 1 and Fig. 4.

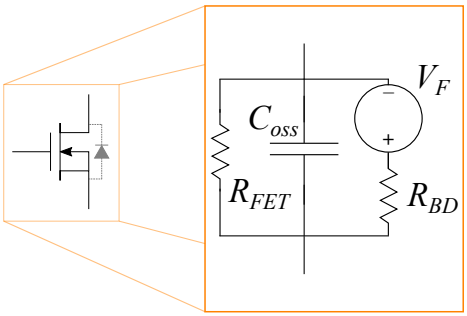


Fig. 3. Transistor equivalent model.

A. Diode Error Correction

At the end of each switching interval, the linear equivalent of the circuit changes, and a switching action occurs. Independent switching actions occur at planned instances during the switching period, such as an external signal driving the gate of a transistor. Dependent switching actions occur when the state variables of the converter dictate a switching action is required, such as a diode conducting when its forward bias is reached. A state-dependent switching action results in

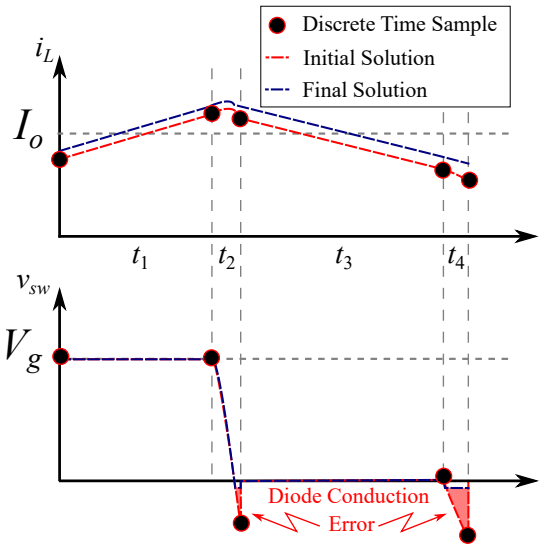


Fig. 4. Waveform of a synchronous buck converter after the high side device turns off. The initial guessed dead time length is too long between active switching actions.

TABLE I
BUCK CONVERTER DEADTIME SOLUTION

Inital Solution						
Time Interval	t_1	t_2		t_3	t_4	
Circuit Model	$\boldsymbol{A}_1$	$\boldsymbol{A}_2$		$\boldsymbol{A}_3$	$\boldsymbol{A}_4$	
Conducting Devices	M_1	—		M_2	—	
Final Solution						
Time Interval	t_1	t_2		t_3	t_4	
Circuit Model	$\boldsymbol{A}_1$	$\boldsymbol{A}_2$	$\boldsymbol{A}_2^*$	$\boldsymbol{A}_3$	$\boldsymbol{A}_4$	$\boldsymbol{A}_4^*$
Conducting Devices	M_1	—	$M_{2,BD}$	M_2	—	$M_{2,BD}$

a nonlinear state-space description due to the time t_i being dependent on instantaneous state values.

An example of independent and dependent switching is shown in Fig. 4. During the dead times of the converter, the switch node voltage crosses the forward voltage of the M_2 body diode. The final steady-state solution, as shown in Table I, shows the insertion of two additional switching actions to correctly simulate how a physical circuit would behave.

An example approach to finding the duration and location of dependent switching actions is presented in [2], using successive approximate steady-state solutions to converge to an error-free switching sequence that solves the converter steady-state operation.

III. OPTIMIZED COMPONENT SELECTION

The rapid converter steady-state modeling enabled by discrete time state-space modeling enables new modeling approaches to broad-scale optimization of power converters. While the rapid modeling allows brute force methods to cover a broader scope and metaheuristic optimization methods to perform faster, there are formal techniques that take advantage of the modeling framework.

As shown in Fig. 1, each of the design objectives used in the optimization are outputs of the converter modeling, such as power loss or power density. The inputs to the modeling process include variables of a converter, such as the selection of semiconductor and passive devices, topology, and switch modulation strategy.

Approaches to optimize converters are already used within the discrete time state-space modeling process itself. For example, in order to account for state-dependent switching, a first-order approximation is used to identify and correct forward voltage or body diode violations iteratively to find the converters steady-state [2]. A similar gradient-based approach is used in this work to examine selection of discrete devices.

An example of a continuous space is shown in Fig. 5 for the conduction resistance and output capacitance of a power transistor. For some hypothetical converter, contours of constant power loss are represented by the solid lines with the gradient shown via the purple hue. The arrows point in the direction of steepest descent.

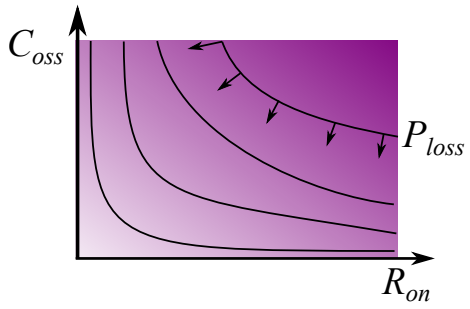


Fig. 5. Continuous representation of a transistor power loss swept across output capacitance and conduction resistance.

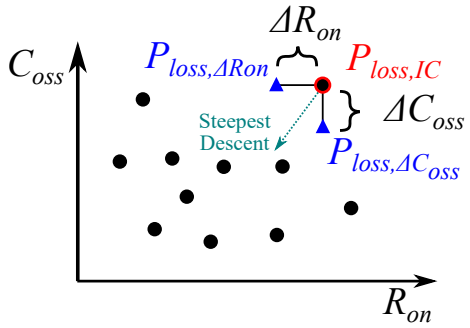


Fig. 6. Gradient method for a transistor optimization overlaid with discrete devices.

While the gradient-based approach can be used, there are additional constraints that must be considered. Many input variables to the modeling are not continuous and/or are unordered, such as the selection of converter topology. The selection of power devices among discrete transistors, in contrast, can be arranged into a pseudo-ordered multivariable space of the individual device parameters where gradient-based methods may be used.

An example of a gradient-based, discrete optimization approach is shown in Fig. 6. An initial discrete point is chosen and modeled to assess the converter's power loss $P_{loss,IC}$. The

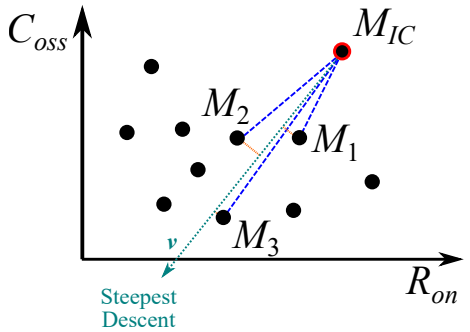


Fig. 7. Steepest descent line compared to discrete devices within the design space.

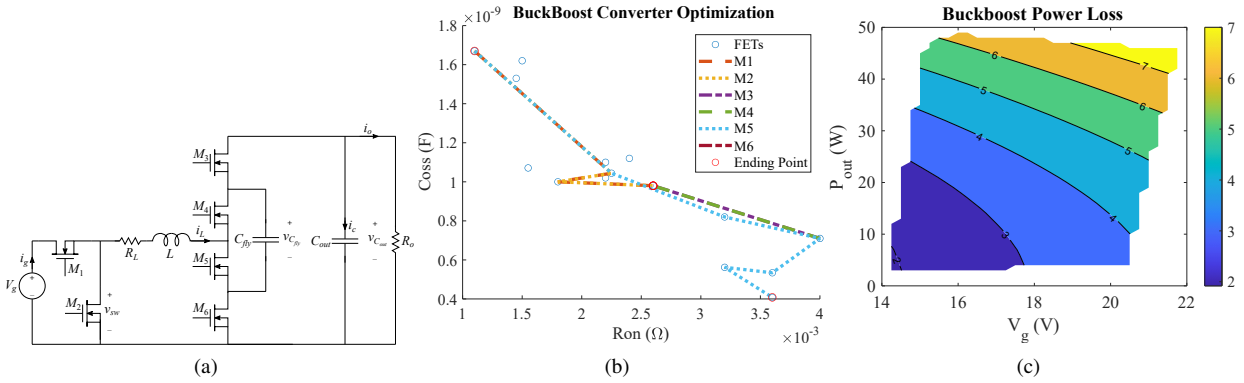


Fig. 8. Buck-boost converter schematic (a) optimization process (b) modeled results (c).

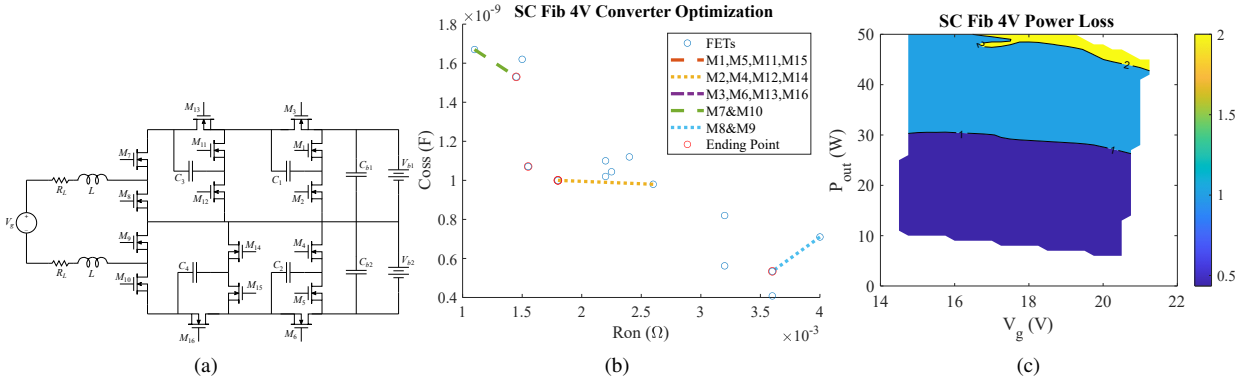


Fig. 9. 4V switched capacitor Fibonacci sequence schematic (a) optimization process (b) modeled results (c).

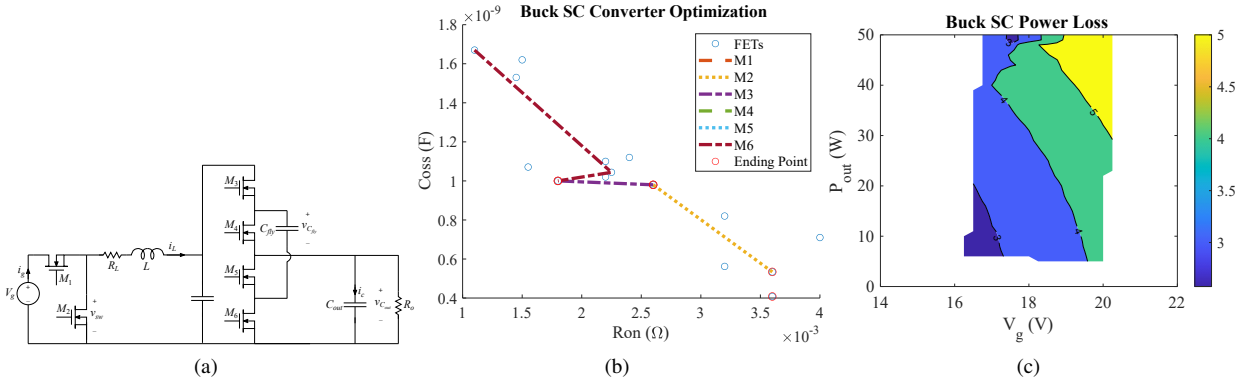


Fig. 10. Buck Switched Cap schematic (a) optimization process (b) modeled results (c).

parameters of the converter semiconductors are then perturbed by ΔR_{on}, ΔC_{oss} to determine their effect on the converter's performance, $P_{loss,\Delta x}$. The perturbations, however, are not discrete points defined by other semiconductor devices, but rather scaled to accurately estimate the steepest gradient of the converter power loss at the initial condition. The perturbed performance metrics, $P_{loss,\Delta R_{on}}$ and $P_{loss,\Delta C_{oss}}$, are solved using discrete time state-space modeling. The vector of steepest descent is then approximated by solving for the slope of the output perturbation over the input perturbation,

$$m_{gd} = \left. \frac{\frac{\Delta P_{loss,\Delta C_{oss}}}{\Delta C_{oss}}}{\frac{\Delta P_{loss,\Delta R_{on}}}{\Delta R_{on}}} \right|_{M_{IC}} . \tag{5}$$

In this example, the vector of steepest descent, v, is a line with the slope from (5) through the initial device M_{IC} with power loss $P_{loss,IC}$. This methodology can be expanded to higher orders to account for multiple input and output modeling variable possibilities.

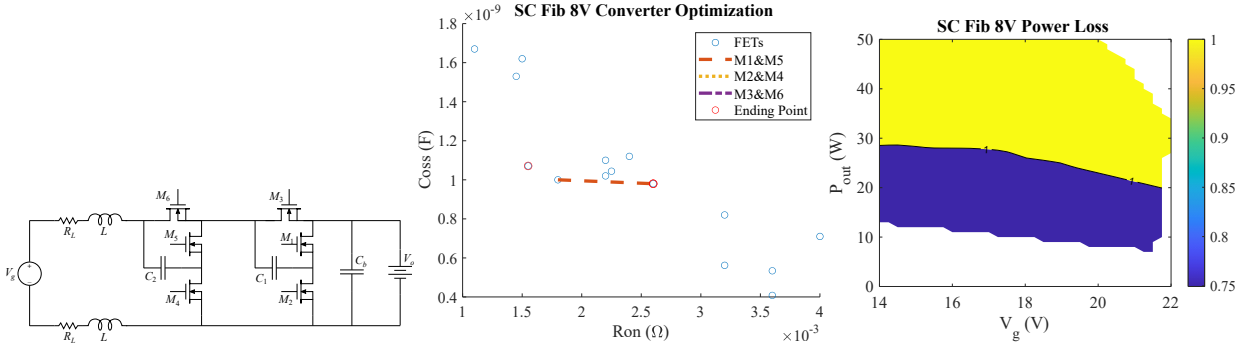


Fig. 11. 8V Switch capacitor Fibonacci sequence schematic (a) optimization process (b) modeled results (c).

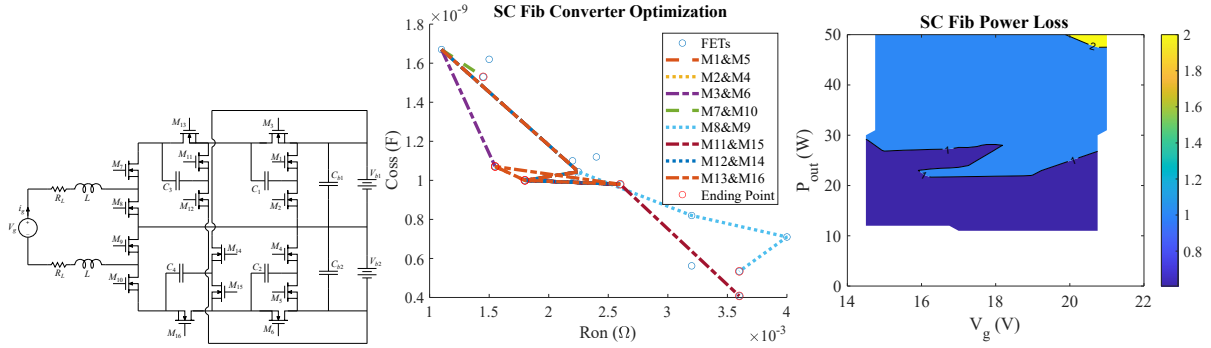


Fig. 12. Switched capacitor Fibonacci sequence schematic (a) optimization process (b) modeled results (c).

The next transistor to be modeled must now be selected from the direction of steepest descent. However, stepping too far from the initial condition will result in large potential error from the localized approximation in (5). Therefore, the selected device for the next iteration is the device with the minimum distance, $d()$, from M_{IC} plus the minimum distance to the steepest descent vector $\boldsymbol{v}$ using m_{gd} as shown in Fig. 7,

$$M_{IC+1} = \min[e_{IC} d(M_{IC}, M_i)] + e_{\boldsymbol{v}} d(M_i, \boldsymbol{v})]. \quad (6)$$

The variables e_{IC} and $e_{\boldsymbol{v}}$ are weighting coefficients that shift the next selection to be closer to M_{IC} or $\boldsymbol{v}$. To help speed up the optimization, the five closest points according to (6) are approximated using projections from $P_{loss,\Delta x}$. The most efficient device is chosen for the next iteration.

IV. Example Design Optimization

The proposed modeling and optimization techniques are used to design an example converter for battery charging applications. In order to verify the proposed method, several topologies are designed to find an optimal converter with a 16-20 V input and up to a 40 W, 8 V output showcasing the discrete time state-space models and the optimization framework for discrete transistors.

A. Modeling

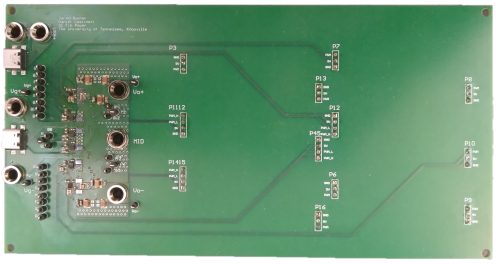
Five topologies shown in Fig. 8-12 showcase the optimization process. Each of the transistors within the converter are optimized to reduce P_{loss}. Each figure shows the topology schematic, the iteration path of the transistor selection, the process for a common database of commercial transistors, and the resulting steady-state efficiency at a range of power levels and input voltages.

B. Experimental

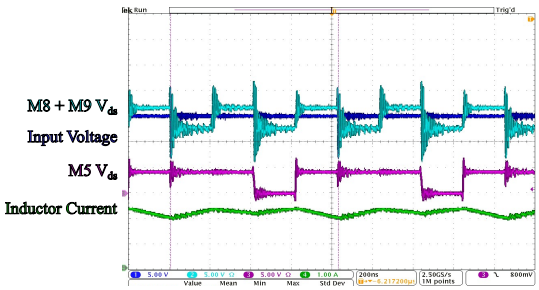
The switched capacitor Fibonacci converter shown in Fig. 13 is selected to experimentally validate the modeling method. For the prototype, the design was constrained to have all the same transistors, rather than optimizing each device individually as in the previous section. The transistor EPC2055 was chosen via a sweep of the design space, as shown in Fig. 14. Additional converter parameters are given in Table II. As shown in Fig. 13, the broad steady-state modeling matched experimentally-measured power loss with acceptable error.

V. Conclusion

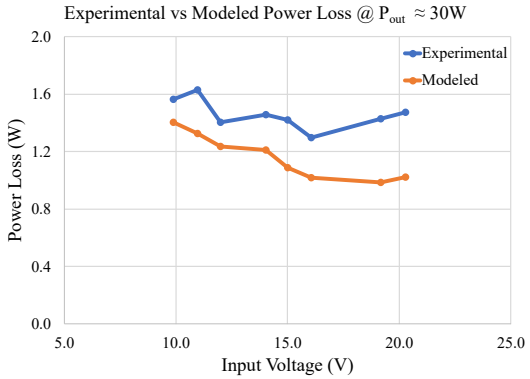
This work proposes a method to quickly optimize power converters by leveraging discrete time state-space modeling. A gradient-based optimization method is used to rapidly solve discrete converter parameters across a wide input voltage and



(a)



(b)



(c)

Fig. 13. Switched capacitor Fibonacci prototype (a) experimental waveforms (b) modeled vs experimental results at 30 W output power (c).

TABLE II
SWITCH CAPACITOR FIBONACCI CONVERTER PARAMETERS

L	0.65 µH	P_o	0-40 W
C_{1-4}	10 µF	$C_{oss,M1-16}$	408 pF
R_L	10 mΩ	R_{ds}	3.6 mΩ
V_g	16-20 V	f_s	1.2 MHz

power range, as well as numerous topologies. The design framework was also experimentally verified using a switched capacitor Fibonacci converter.

ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under Grant Number 1751878.

This work made use of Engineering Research Center shared facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

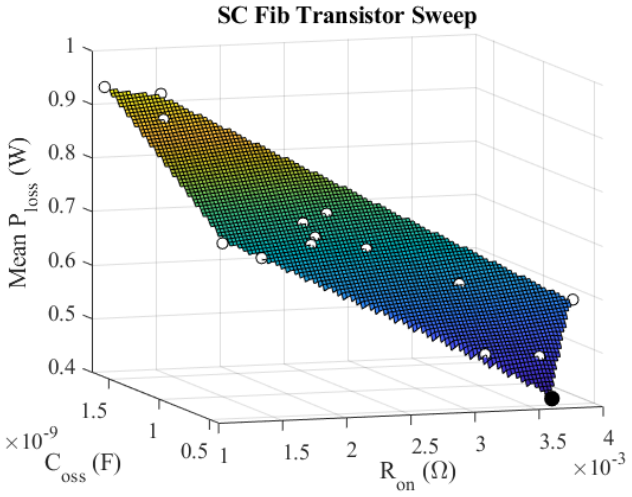


Fig. 14. Switched capacitor Fibonacci transistor design space where all converter transistors are the same. The optimal point, shown by the black circle, is the EPC2055 transistor. P_{loss} is a weighted mean of hundreds of simulations for each transistor between the input voltage and output power range .

REFERENCES

[1] J. A. Baxter and D. J. Costinett, "Converter analysis using discrete time state-space modeling," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2019, pp. 1–8.

[2] J. A. Baxter and D. J. Costinett, "Steady-state convergence of discrete time state-space modeling with state-dependent switching," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Nov. 2020, pp. 1–8.

[3] K. Hermanns, Y. Peng, and A. Mantooth, "The increasing role of design automation in power electronics: Gathering what is needed," *IEEE Power Electronics Magazine*, vol. 7, no. 1, pp. 46–50, March 2020.

[4] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.

[5] F. Wang, G. Chen, D. Boroyevich, S. Ragon, M. Arpilliere, and V. R. Stefanovic, "Analysis and design optimization of diode front-end rectifier passive components for voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2278–2289, 2008.

[6] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A general approach to sampled-data modeling for power electronic circuits," *IEEE Transactions on Power Electronics*, vol. 1, no. 2, pp. 76–89, 1986.

[7] D. J. Costinett, "Analysis and design of high efficiency, high conversion ratio, dc-dc power converters," Ph.D. dissertation, University of Colorado at Boulder, 2013.

[8] H. R. Visser and P. P. J. van den Bosch, "Modelling of periodically switching networks," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, June 1991, pp. 67–73.

[9] F. C. Y. Lee, R. P. Iwens, Y. Yu, and J. E. Triner, "Generalized computer-aided discrete time-domain modeling and analysis of dc-dc converters," *IEEE Transactions on Industrial Electronics and Control Instrumentation*, vol. IECI-26, no. 2, pp. 58–69, May 1979.

[10] A. Kumar, J. Lu, and K. K. Afridi, "Enhanced-accuracy augmented state-space approach to steady-state modeling of resonant converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–6.