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Compact Three-Level GaN Power Module Suitable for Active-Neutral-Point-Clamped (ANPC) Three-Level Converter

Ziwei Liang
Department of Electrical Engineering and Computer Scienec
University of Tenneessee
Knoxville, TN, USA
Knoxville, USA
zliang7@utk.edu

Liyan Zhu
Department of Electrical Engineering and Computer Scienec
University of Tenneessee
Knoxville, TN, USA
Knoxville, USA
liyan@utk.edu

Hua Bai
Department of Electrical Engineering and Computer Scienec
University of Tenneessee
Knoxville, TN, USA
Knoxville, USA
hbai2@utk.edu

Yue Sun
Department of Electrical Engineering and Computer Scienec
University of Tenneessee
Knoxville, TN, USA
Knoxville, USA
ysun79@vols.utk.edu

***Abstract*—This paper presents a compact three-level (3L) Gallium Nitride (GaN) power module with low parasitic parameters. The power loop, gate loop and PCB layout are designed and optimized carefully to achieve: 1) low parasitic parameters; 2) good thermal performance; 3) compact size and high integration; 4) easy utilization on building 3L ANPC converter. To achieve higher power rating, for two high-frequency (HF) switch legs, three GaN Systems' GS665016T are paralleled and for the low-frequency pair, two switches are paralleled considering the much lower switching loss. The decoupling capacitors, driver circuits and auxiliary power supplies are all integrated into the module for the easy utilization and small parasitics. Double-pulse test (DPT) is applied to test the electrical characteristics and a bidirectional three-phase 3L ANPC converter is built using the proposed modules to verify the electrical performance and thermal performance.**

Keywords—Three-level power module, GaN devices, integrated gate drive, decoupling cap

I. INTRODUCTION

Compared with the Si devices, the wide-bandgap (WBG) GaN power high electron mobility transistors (HEMTs) can help to increase the power density significantly with the advantages of smaller size, lower $R_{ds,on}$ and faster switching speed[1]. Since the GaN HEMTs are very sensitive to the parasitic parameter and the heat dissipation, some two-level (2L) half-bridge GaN based power modules have been proposed to maximize the switching and thermal performance[2-3]. Reference [2] offers an double-sided cooling design for better thermal performance. Reference [3] integrate the decoupling cap, gate driver and the auxiliary power supply together to have a compact design and supply simpler interface for user.

So far, the maximum blocking voltage of mature GaN HEMTs which are introduced on the market is around 650V, such as 650V GaN transistor from GaN System. Such devices can only serve for two-level(2L) converters with DC voltage lower than 600V considering the enough marge of the Safe Operation Area (SOA). For any application with DC voltage over 600V, it is usually recommended to use 900-1200V SiC MOSFETs [4]. To employ GaN HEMTs in such higher voltage application, one of solution is series two 650V GaN devices. However, such structure requires great simultaneity of two series devices to ensure the balanced voltage distribution. Another solution is to use the multi-level structure yielding the lower voltage stress of switches, lower current ripple and reduction of the filter size [4-7]. One of the most popular three-level topology for the Grid-connection high-power application is 3L-ANPC [6, 8].

Combining the good electrical characters of GaN HEMT and the benefits of 3L-ANPC, a compact 3L GaN based power module with integrated gate drive, auxiliary power supply and decoupling caps is proposed in this paper by using GaN Systems' 650V/60A device (GS66516T). The simple interface makes it convenient to be used to build a high-performance and compact 3L-ANPC converter.

In this paper, Section II describes the PCB design considerations, including the power loop design , gate loop design. Section III introduces the thermal simulation and parasitic simulation. Section IV shows the DPT and bidirectional power experiment results to verify the electrical and thermal performance of the proposed power module.

II. PCB DESIGN

A. Schematic of 3L-ANPC Phase Leg

The schematic of one 3L-ANPC phase leg is shown in Fig.1. It consists of six switches. Based on the modulation proposed in [9], switch S1-S4 will switch with high frequency (HF) and S5 and S6 will switch with grid frequency which means that the switching loss of S5 and S6 will be much lower than the switching loss of S1-S4.Terminal $+V_{dc}$, V_{dc_mid} and $-V_{dc}$, will be connected to the active , neutral point and negative DC bus. v_{sw} will be connected to the grid side.

To enhance the power capability, three GaN devices are paralleled for the high-frequency switch and two GaN devices are paralleled for the low-frequency switch considering the different loss dissipation. Paralleled devices can reduce the on-state resistance and share the switching current. The diagram of

higher HF switch leg including the integrated gate driver, auxiliary power supply and decoupling cap is shown in Fig.2. The other two switch legs have the similar structure.

B. Integrated Gate Drive Circuit

Isolated gate driver and isolated auxiliary power supply are the key components for the gate driver circuit. Based on the gate drive circuit guidance from GaN System [10], each group of paralleled GaN devices will co-share 1) one-channel isolated gate driver, Si8271AB-ISR; 2) Turning on and off resistor, R_{on} and R_{off}; 3) Gate-source resistor R_{gs}; 4) Isolated power supply. Additionally, one gate resistor R_g and one source resistor R_s are added for each GaN HEMT for the paralleled GaN HEMTs [10]. To reduce the negative V_{gs} spike, R_{on} and R_{off} are optimized and set to 13Ω and 0Ω respectively. R_g and R_s are both 1Ω and R_{gs} is 4.7kΩ.

A negative V_{gs_off} can help to enhance the system stability in real application, -3V_{gs_off} is used for this design. To provide +6 and -3V for the isolated gate drivers, a 12V-9V isolated DC-DC module (PDS1-S12-S9-M-TR) and a following voltage divider is used as the auxiliary power supply. +6V and -3V is generated by connecting a 6V Zener diode and a 1kW resistor in series on the output of the isolated DC-DC module. The main components used in the integrated power module are summarized in TABLE I.

Gate loop design is important for GaN based power module since the GaN HEMTs are sensitive to the gate loop parasitic inductance. Multi-layer PCB is adopted in this design to realize flux canceling [11-12]. Additionally, to minimize the gate loop area and gate loop distance, gate drivers should be put close to the GaN devices. The turn-on gate loop of the paralleled GaN device S2 is shown in Fig. 3. In Fig.3, yellow line represents the shared gate loop and blue, green and black lines represents the gate loops for three GaN HEMTs S2-1, S2-2, S2-3 respectively. Solid line shows the gate current loop from gate driver to the GaN HEMTs, and the dashed line shows the gate current loop back to gate driver. From Fig.3, we can find that, by using the multi-layer PCB, gate current flows through top layer and returns through the internal layer 1, the vertical structure is formed, which can help to reduce the gate loop area and realize flux canceling. Therefore, low gate-loop parasitic inductance can be achieved.

C. Power loop design.

The parasitic inductance of the power loop has a lot of effects on the switching performance, such as voltage spike on gate drive loop, voltage overshoot on Vds and voltage ringing across decoupling cap [13]. Therefore, it's important to reduce the power loop inductance. Similar to the gate loop design, vertical structure is also adopted to the power loop by using multi-layer PCB. To increase the current capability and reduce the conducting loss, eight-layer PCB is employed in the power module design. Eight-layer PCB also enables the possibility of simple interface by putting all HV terminal to one side of the module, which can simplify the employment of such power module in 3L-ANPC converter design.

The top view and bottow view of the proposed GaN power module are shown in Fig. 4. From Fig.4, we can find that the

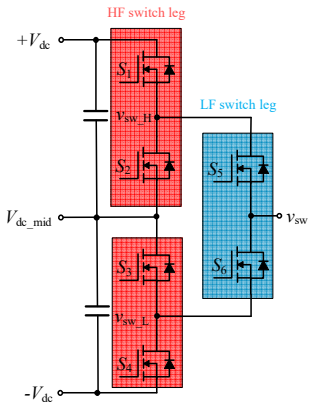


Fig. 1 Schematic of one 3L-ANPC phase leg.

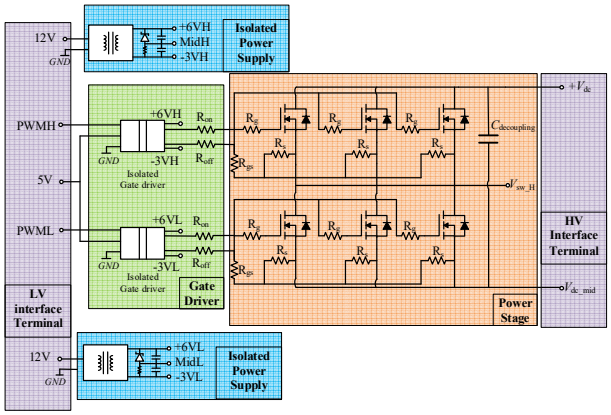


Fig. 2 Diagram of higher HF switch leg.

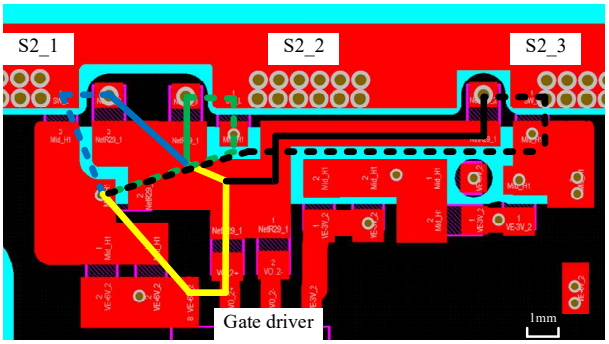


Fig. 3 Turn-on gate loop for paralleled GaN HEMTs.

TABLE I. MAIN COMPONENTS

Component	Part Number	Value
Isolated gate driver	Si8271AB-ISR	--
Isolated power supply	PDS1-S12-S9-M-TR	--
Decoupling cap	C2220X124KDRAC 7800	2*4*0.12μF
GaN HEMT	GS66516T	--

double-side layout is adopted in this module. All the GaN devices are assembled on the bottom layer, and the integrated gate driver, auxiliary power supply and the decoupling cap are assembled on the top layer. The power loops are on internal layers. Specifically, the power loops of two HF switch legs distribute symmetrically on the PCB and have the similar structure. The side view of the PCB and the power loop of one HF switch leg is shown in Fig.5 where the thickness of PCB is scaled up for demonstration purpose. Two groups of LF switches, S_5 and S_6 locate on the two edges of PCB as shown in Fig. 4.

To achieve better thermal performance, an air-cooling heat sink is customized and optimized to match the size of PCB as shown in Fig. 6.

III. Simulation Verification

A. Thermal Simulation

With the custom heat sink, the thermal simulation is conducted based on the assumption that the average loss of each GaN device is 6.5W. High-speed Fan, OD6038 - 12HHBXC01A, is used for cooling the module. A simplified thermal simulation model is built and imported into Ansys Icepack. In the simulation, airflow is set to 0.037 m^3/s based on the fan's parameter and the ambient temperature is set to 70℃ for potential EV on-board charger application. As shown in Fig.7, the simulation result shows that highest temperature is 95.3 ℃, which means the maximum junction-to-case thermal resistance is 0.27 ℃/W.

B. Parasitic Parameter Extraction

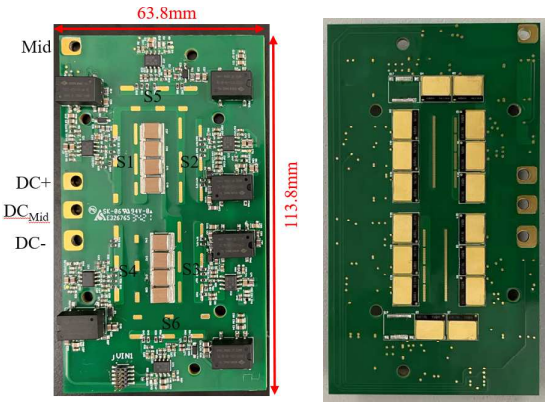
To analyze the parasitic parameters caused by the PCB layout, a simplified power loop is modeled in the ANSYS Q3D to extract the power loop parasitic inductance as shown in Fig. 8. The power loop inductance based on the Q3D analysis is 1.27nH. The comparison between the proposed power loop inductance and the power loop inductance in previous literatures is provided in TABLE II. This result verified that a small power loop inductance is introduced by such PCB layout, which can help to reduce the overshoot on drain-source voltage during turning-off process.

IV. Experiment Verification

A. DPT

DPT test is conducted separately for two HF switch legs to verify the HF switching performance. The test diagram is shown in Fig. 9. One 200μH inductor is used as the load inductor. From Fig. 9, we can find that the corresponding LF switch is also included in the test setup, and during the DPT, the LF switch will keep on state to keep consistent with the ANPC control schematic.

The DPT test results are shown in Fig. 10. Based on the test results, the overshoots on drain-source voltage at 350V/42A are 4.3% and 5% for higher and lower HF switch leg respectively. Similar overshoots verified that the symmetrical design of two HF switch legs. Small overshoots verified that low power loop parasitic inductance is achieved.



(a) Top View (b) Bottom View

Fig. 4 Proposed GaN power module.

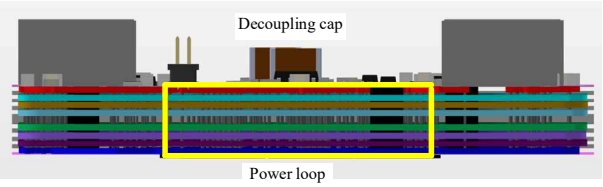


Fig. 5 Power loop of one HF switch leg.

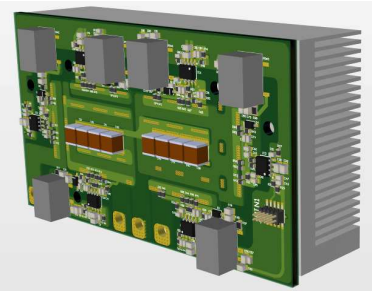


Fig. 6 GaN module with installed custom heatsink.

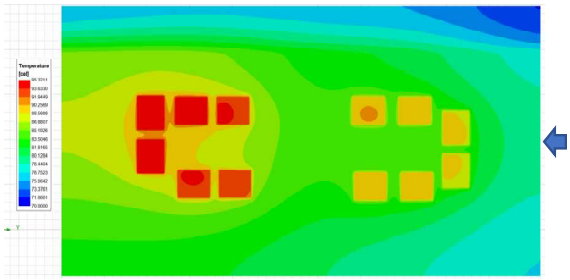


Fig. 7 Thermal simulation result @ Ploss_ave = 6.5W per GaN.

B. Conveter power test

To verify the electrical and thermal performance, a bidirectional three-phase 3L ANPC converter is built. The bidirectional power test results of the 3L converter is shown in

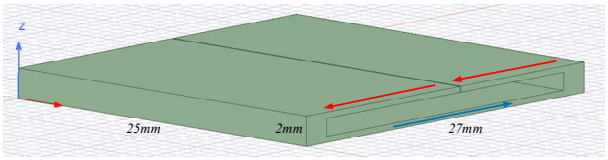


Fig. 8 Simulation model of power loop.

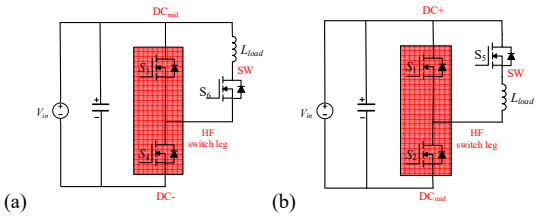


Fig. 9 Schematic of the DPT for the HF switch legs in the 3L modules (a) lower switch leg ; (b) higher switch leg.

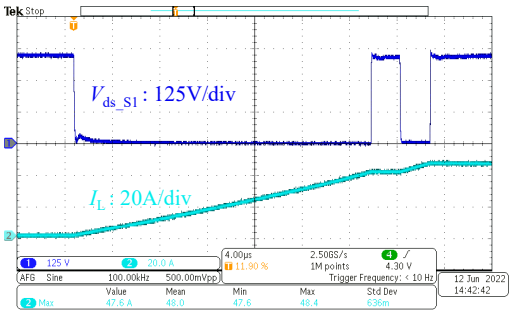


Fig. 10 DPT test waveform @ 350V/42A.

TABLE II. COMPARISON OF POWER LOOP INDUCTANCE

Reference	Layout	Loop Inductance(nH)
[2]	Vertical	1.7-2.4
[3]	Vertical	0.77
[4]	Vertical	1.2
[14]	Lateral	5
This paper	Vertical	1.27

Fig. 11. Fig. 11(a) shows the 7.2kW PFC mode with three-phase 220V_{phase} AC input and 620V DC bus voltage output. Highest temperature is 46°C with around 20°C ambient temperature. Fig.11(b) shows the 8kW inverter mode test result with 600V DCbus voltage input and 180V_{phase} AC output. Only 5% overshoot voltage in 350V/42A DPT test and the bidirectional 3L converter-based power test with the maximum efficiency up to 99% verified the electrical and the thermal performance of the proposed GaN module.

V. CONCLUSION

This paper proposed an integrated 3L GaN power module to employ the 650V GaN deivces in the over-600V converters.

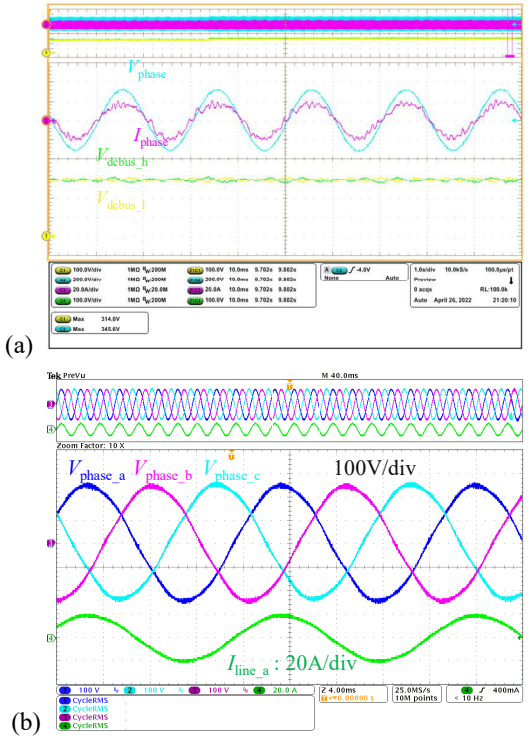


Fig.11 3L converter power test: (a) PFC mode @7.2kW; (b) inverter mode @8kW.

High-compactness is achieved by the integration of the isolated gate drivers, isolated auxiliary power supply and the decoupling cap together. Gate driver circuit is carefully designed to ensure the successful operation of paralleled GaN HEMTs. Low power-loop parasitic inductance and simple interface are achieved, which benefits from the optimized power loop design. The electrical and thermal performance has been verified by the DPT and bidirectional power test based on the three-phase 3L-ANPC converter, which is built by using the proposed GaN module. The experiment results show that the proposed GaN module could be a good candidate to employ the GaN HEMTs in the over 600V 3L converter design.

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