Intelligent Gate Drive for Cryogenic Solid-state Circuit Breaker with Current Limitation Capability for Aviation Application

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***Abstract*—To increase the current interrupting capability for the DC solid-state circuit breaker (DC-SSCB), power semiconductors need to possess a higher pulse current. Moreover, for the power electronics protection system, it is also important to enable the system with a fault current limitation capability. Accordingly, this paper aims to design an intelligent gate drive for DC-SSCB, which can operate in cryogenic conditions to increase interrupting capability of the SSCB. Meanwhile, the proposed intelligent gate drive also enables the SSCB to operate in the current limitation mode to limit the overcurrent in the aviation system. The current limitation mode can help the aviation system limit the inrush current during startup and realize fault ride-through for the healthy part when the fault occurs. Finally, test results based on a 200V/150A SSCB with the current limitation mode prototype verify the proposed intelligent gate drive design for SSCB with cryogenic cooling.**

***Keywords*—Solid-state circuit breaker (SSCB), cryogenic, current limitation, aviation**

I. Introduction

The weight-energy tradeoff is an obstacle to limiting the development of the electrified aircraft propulsion (EAP) system. The EAP-related batteries, cables, converters., etc., can take a large proportion of the takeoff weight of the electrified aircraft. Accordingly, the medium voltage direct current (MVDC) system can be an appropriate solution for the EAP system power configuration to reduce the aircraft's weight [1]. As the critical component of the MVDC protection system, a safe and reliable DC solid-state circuit breaker (DC-SSCB) with a fast response time is of vital significance. The current limiting inductor-free DC-SSCB topology is shown in Fig.1. The system fault current is interrupted by turning off the power semiconductor. Transient voltage suppression (TVS) diode and snubber RC circuit cooperate with each other to absorb the extra energy during the turn-off interval of the SSCB.

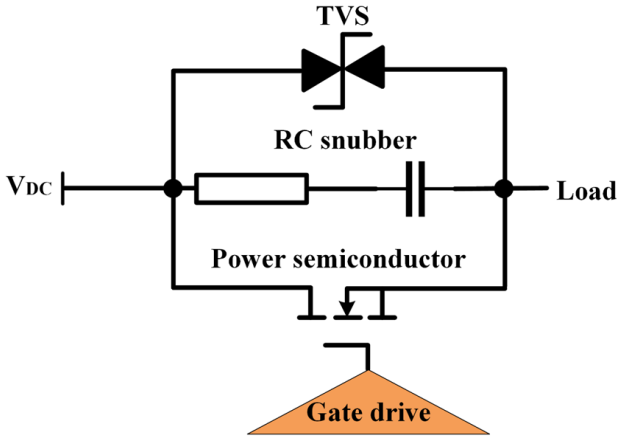

Fig. 1. Topology of the SSCB.

Recently, the cryogenically cooled EAP attracted increasing attention in the aviation industry [2]. From the system level, the supportive power systems for the superconducting motors and generators [3] will become essential. Then, combining superconductive systems with cryogenic power electronics [4] can reduce the complexity of the system and improve power density by removing the extra thermal insulation and temperature regulation system. From the converter level, the performance of the power semiconductor can be improved with cryogenic cooling by decreasing on-state resistance and increasing switching speed. Secondly, the

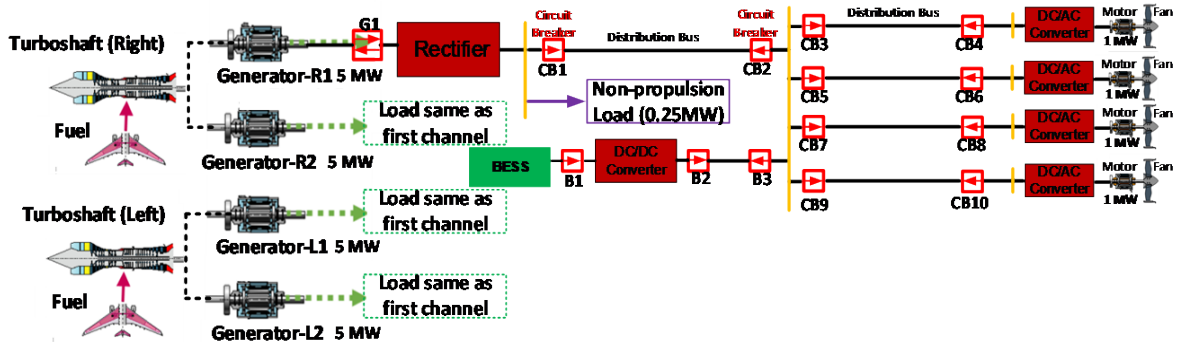

Fig. 2. System configuration of the electrified aviation system.

resistivity of conductors which are utilized as the winding of the inductor reduces with the decrease of the temperature. Additionally, cryogenic cooling provides a low ambient temperature to allow higher temperature rising and less heat removal. Therefore, to improve the performance of the SSCB and the integration of the EAP system, it is significant to develop an SSCB that can leverage the advantages of the cryogenic cooling system. For the SSCB, most papers focus on the topology, current interruption strategy, voltage clamping circuit, etc. [5]. Few papers study the SSCB with cryogenic cooling. The superconducting technology is only applied to the traditional mechanical circuit breaker [6].

This paper is organized as follows: Section II presents the necessity of the breaker and limiter in the EAP protection control system. The proposed intelligent gate drive for SSCB enables the SSCB with current limitation capability. Section III discusses the intelligent gave drive circuit detail design for breaker mode and limiter mode, respectively. Section IV verifies the function of the intelligent gate drive design with cryogenic cooling. Finally, Section IV derives the conclusion of the digest and the future work.

II. Gate Drive Consideration For SSCB In Aviation System

Fig. 2 illustrates the basic MVDC system configuration for the aviation system [7]. Circuit breakers are located at both ends of the distribution bus to interrupt the short circuit fault from the motor side or the generator side. In the past decades, there are few research on an equipment with breaker and limiter function at the same time. Breaker and limiter [8] are controlled separately to protect the power system. The current limiter can be leveraged to limit the inrush current during the system startup, and limit the short circuit current, or overload current. Meanwhile, the breaker is utilized to interrupt the short circuit fault current. For a traditional EAP system, the breaker and the limiter are two different components. However, this paper proposes a new intelligent gate drive circuit for the SSCB which enables the SSCB with current limitation capability.

The proposed intelligent gate drive circuit for SSCB with current limitation capability can decrease the complexity, weight, and cost of the EAP protection system. The intelligent gate drive circuit schematic is shown in Fig. 3 and Fig. 4. With the control of the mode selection signal, the SSCB can operate in the traditional breaker mode or the current limiter mode. The breaker mode can help SSCB realize the fundamental fault current interruption function; the limiter mode can help aviation system to limit the inrush current during the startup and realize fault ride-through for the healthy part when the fault happens.

III. Design Of The Intelligent Gate Driver For The Proposed SSCB

A. Breaker mode

Fig. 3 shows the schematic of the breaker mode gate drive circuit. When the mode selection signal is low, the SSCB will operate in the breaker mode. The grey circuit part is for the limiter mode, and it does not work in the breaker mode. The breaker mode gate drive circuit is composed of the detection circuit, fault comparison circuit, fault keeping and reset circuit, and soft turn-off circuit.

Breaker protection is triggered by desaturation protection [9]. The detection circuit for SSCB could sense the drain-source voltage v_{ds}. In the fault comparison circuit, the sensed v_{ds} need to compare with the threshold voltage for limiter mode. When v_{ds} indicates that the power semiconductor has left its normal working region and entered the active region, the fault pulse signal produced by the comparator will be sent to the fault keeping and reset circuit. The latch-up circuit can keep the fault pulse signal and send it to the soft turn-off circuit. The reset function is realized by clearing the fault signal through an RC delay circuit with the latch-up circuit. Finally, breaker mode can interrupt the fault by turning off the power semiconductor through the soft turn-off circuit. The typical simplified waveform for the breaker mode is demonstrated in Fig. 5. There is a short circuit fault that occurs at t_0. At t_1, the desaturation voltage V_{desat} is higher than the threshold voltage, and the protection will be triggered. Then, during the time interval t_1 to t_4, v_{gs} decreases from turn-on voltage to turn-off voltage, and the system fault current is interrupted. Ref. [10] demonstrates the detail from t_0 to t_4.

B. Limiter mode

When the mode selection signal is high, the SSCB will operate in the limiter mode. In the limiter mode, the power semiconductor volt-ampere (V-I) curve characteristic is utilized to limit the system current. As illustrated in Fig. 6, the

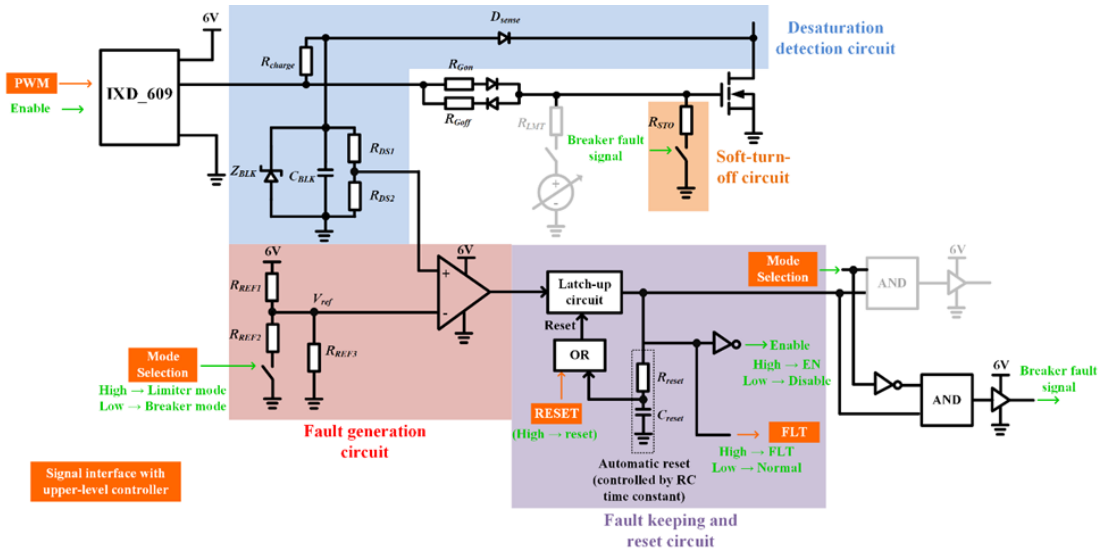

Fig. 3. System configuration of the electrified aviation system.

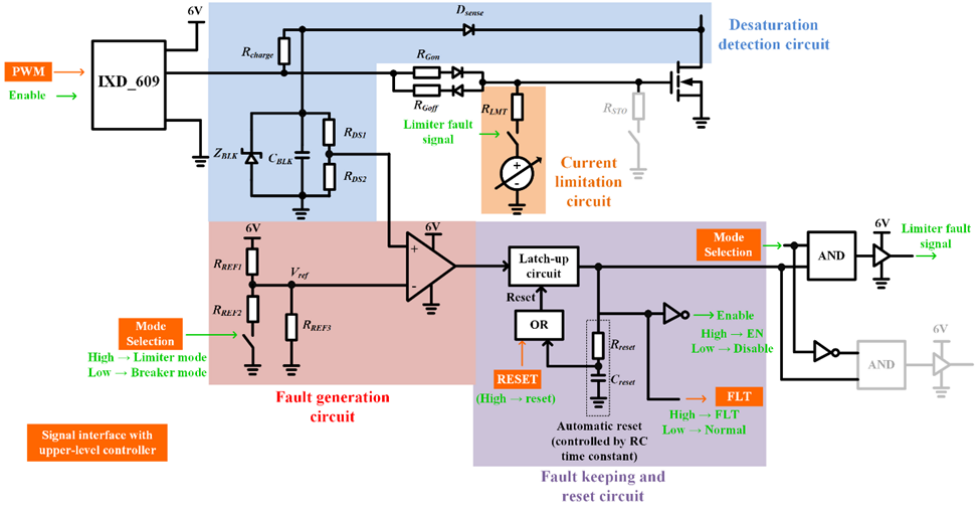

Fig. 4. System configuration of the electrified aviation system.

power semiconductor can operate in the linear region, active region, and cut-off region. Thus, when the overcurrent occurs, the gate voltage decreases to current limitation gate voltage, and the system current forces the power semiconductor to operate in the active region to limit the system current. Additionally, the saturation current I_{sat0}, I_{sat1}, and I_{sat2} are related to the gate voltage, which means that the current limitation level can be tuned by the current limitation gate voltage. Fig. 4 shows the schematic of the limiter mode gate drive circuit. The grey circuit part is for the breaker mode, and it does not work in the limiter mode. The limiter mode gate drive circuit is composed of the detection circuit, fault comparison circuit, fault keeping and reset circuit, and adjustable VEE circuit.

Like the breaker mode, the desaturation detection is leveraged to detect the overcurrent event. If the detected v_{ds} is higher than the threshold voltage for the limiter mode, the fault pulse will be delivered to the fault keeping and reset circuit. Then the fault signal produced by the latch-up circuit will control the adjustable VEE circuit to decrease the v_{gs} to limit the system current. And the current limitation level is decided by the output voltage of the adjustable VEE circuit. The simplified waveform for the limiter mode is demonstrated in Fig. 7. The overcurrent event happens at t_0, and the overcurrent is detected by the limiter mode at t_1. From t_0 to t_1, v_{gs} keeps at the turn-on value. Then, during the time interval t_1 to t_3, v_{gs} is controlled by the adjustable VEE and v_{gs} decreases to the current limitation voltage. In this scenario, the power semiconductor operates in the active region. Because the

system current is limited by the V-I curve characteristic, the system current limitation value can be tuned by v_{gs}. At t_3, the fault current limitation ends and the SSCB is turned off.

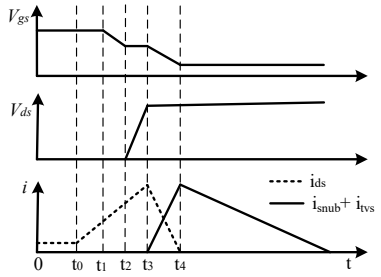

Fig. 5. Simplified waveform for breaker mode.

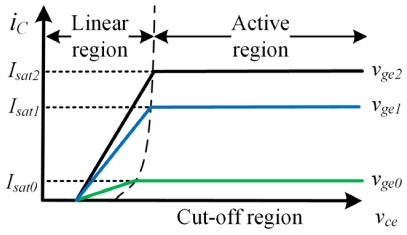

Fig. 6. Typical V-I curve for power semiconductors.

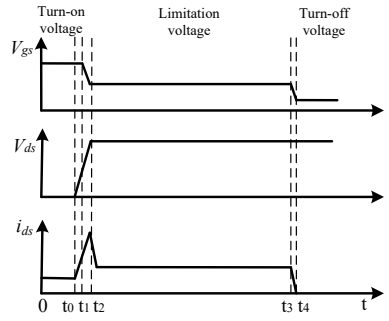

Fig. 7. Simplified waveform for limiter mode.

C. *Adjustable VEE circuit*

Considering that the requirement for limiting current varies with different scenarios, it is essential to change v_{gs} online to turn the current limitation level for the modern DC distribution system. Fig. 8 shows the current limitation circuit's online adjustable gate voltage implementation circuit. The online adjustable gate voltage implementation circuit consists of one digital potentiometer and an LDO with adjustable output. Most digital potentiometers are built from a resistor ladder integrated circuit shown in Fig. 9. The digital potentiometer's internal topology consists of a simple serial string of resistors with digitally addressable electronic switches between the wiper and these resistors. The wiper locates between the point of A (POA) and the point of B (POB). The input of the digital potentiometer determines the address of the wiper. For the digital potentiometer in Fig. 9, to control the location of the wiper, the upper-level controller sends the address of the wiper to the digital potentiometer through the serial peripheral interface (SPI) communication. SPI communication relies on the chip selection (CS) signal, the clock (SCK) signal, and the serial data in/out (SDI/SDO) signal to complete the data transmission. With the SPI control, the resistance between POB and the point of the wiper (POW) can be expressed as

$$R_{WB} = \frac{R_{AB} \times N}{N_{step}}$$

where N_{step} is the total step for a digital potentiometer (e.g., a 7-bit digital potentiometer has 127 steps, an 8-bit digital potentiometer has 257 steps); N is the wiper address (0-127 for a 7-bit digital potentiometer, 0-257 for an 8-bit digital potentiometer) sent by the SPI communication; R_{AB} is the resistance between POA and POB.

To realize the online adjustable gate voltage control, an adjustable LDO to generate the required gate voltage is also important. The output of the adjustable LDO can be derived as follows

$$V_{LDO\_out} = V_{adj} \times (1 + \frac{R_{WB}}{R_2})$$

where V_{adj} (1.2V-1.3V for most adjustable LDOs) is the voltage across the ADJ and GND of the LDO, providing the reference voltage for the output; R_2 is the resistor between the OUT and ADJ pin of the LDO.

Based on the output equation of the adjustable LDO, with the fixed R_2, the output of the LDO can be controlled by the digital potentiometer through SPI communication.

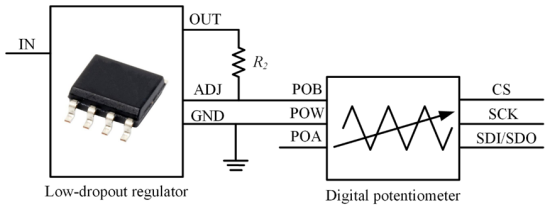

Fig. 8. Design of the online adjustable gate voltage implementation circuit.

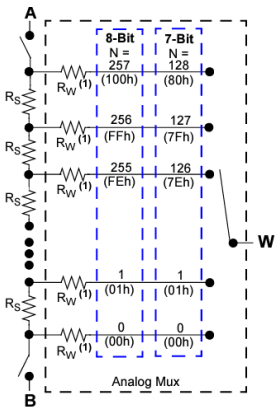

Fig. 9. Resistor block of the digital potentiometer.

IV. Verification Of The Intelligent Gate Driver

A 200V/60A SSCB prototype has been built up to demonstrate the effectiveness of the proposed intelligent gate drive circuit for the SSCB with current limitation capability. The key parameters are summarized in Table I and Fig. 10 shows the cryogenic platform and the SSCB under test.

TABLE I. SSCB KEY PARAMETERS

Parameters	Value
V_{DC}	200V
GaN	GS66516T
TVS	AK3-430
System inductance	5.7uH
Resistance of RC snubber	0.5Ω
Capacitance of RC snubber	150nF
R_g	15Ω
Turn-on gate voltage	6V
Turn-off gate voltage	-3V

Fig. 10. Cryogenic test set up for the proposed SSCB.

A. Verification of breaker mode

Fig. 11 illustrates the waveform of the proposed DC-SSCB in breaker mode when L_{sys} = 5.7μH. v_{desat} is the sensing v_{ds} to trigger the protection, and v_{flt} is the fault signal to control DC-SSCB.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. The increasing speed of i_{sys} is based on the value of L_{sys}. When GaN is turned on, the high dv_{ds}/dt induces the current flowing through the RC snubber from 0 μs to 0.5 μs. Since DC-SSCB is always conducted during normal operation and the fault happens when DC-SSCB is conducted, this will not occur in the real scenario.

When the fault happens, v_{desat} and i_{sys} keep increasing. Since the fault is not detected, v_{gs} = 6V, and GaN keeps on-state. Then, at 2.6 μs, v_{desat} increases to the threshold voltage, triggering the protection. v_{gs} decreases to -3V to turn off DC-SSCB. From 2.6 μs to 3.2 μs, current commutate from GaN to RC snubber and TVS. Peak drain-source voltage V_{DS_peak} is clamped by TVS to 590V, and the peak system current I_{sys_peak} is 131A. Finally, after 3.2 μs, TVS keeps dissipating the extra system energy produced during the interruption process.

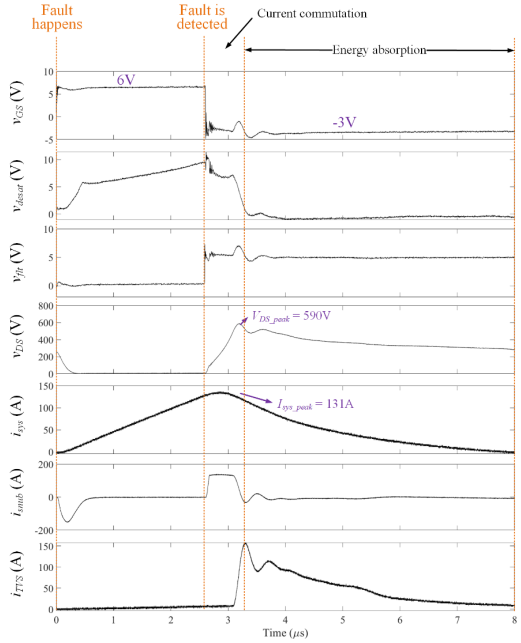

Fig. 11. Waveform of the proposed DC-SSCB in breaker mode.

B. Verification of limiter mode

To verify the current limitation function, Fig. 12 shows the waveform of the proposed DC-SSCB in limiter mode when L_{sys} = 5.7 μH.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. Then, when the fault is detected, v_{gs} is controlled by the intelligent gate drive decreasing to the current limitation gate voltage (2V in this case). Because GaN has arrived in the active region and the current flowing through the GaN is determined by the current limitation gate voltage, which can limit the system fault current. For the case in Fig. 12, the current limitation gate voltage is 2V, and i_{ds} is limited to about 10A. Meanwhile, TVS and RC snubber cooperate in dissipating the extra energy generated when DC-SSCB starts to limit the system current. Following the fault signal, the system's current limitation time is 45μs, which is determined by the RC constant of the reset function circuit. Finally, v_{gs} will

decreases to -3V to turn off DC-SSCB when the input PWM signal is low.

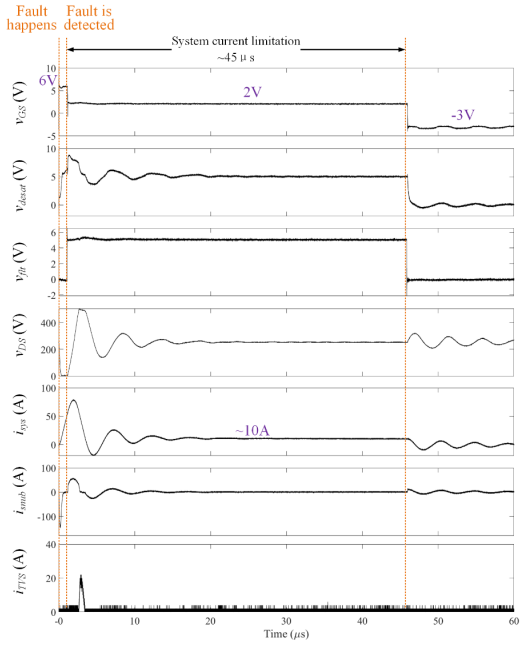

Fig. 12. Waveform of the proposed DC-SSCB in limiter mode.

C. *Verification of the 90K operation*

The signal level test results of the breaker and limiter mode under 90K chamber temperature are illustrated in Fig. 13 and Fig. 14. From the signal level, it can be found that the breaker mode and limiter mode work well under 90K.

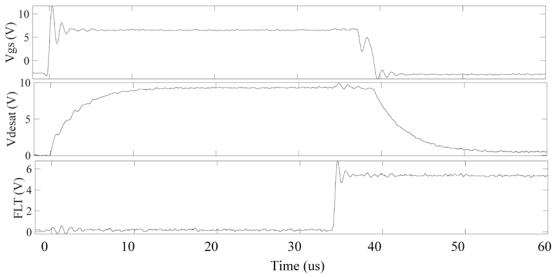

Fig. 13. Waveform of the proposed DC-SSCB in breaker mode when temperature is 90k.

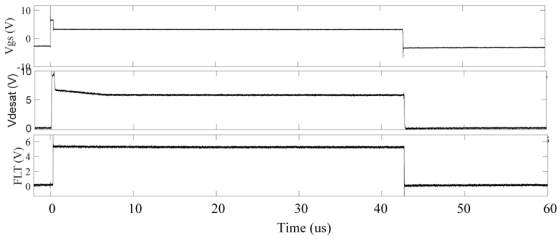

Fig. 14. Waveform of the proposed DC-SSCB in limiter mode when temperature is 90k.

V. CONLUSION

This paper demonstrates the intelligent gate drive circuit design for the SSCB with current limitation capability. The current limitation is realized by decreasing the gate voltage and the power semiconductor can limit the system fault current based on the V-I curve characteristics. The current limitation level can be tuned by the gate voltage. Moreover, the proposed intelligent gate drive circuit operates appropriately with 90K, which can improve the performance of the power semiconductor for SSCB.

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