Transformer Current Spike Elimination for Dual Active Bridge Converter Considering Multiple-Phase-Shift Modulation

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Abstract—**With the development of the modulation strategies for dual-active-bridge (DAB) converters, single-phase-shift (SPS), dual-phase-shift (DPS) and triple-phase-shift (TPS) have been proposed aiming at the realization of zero-voltage-switching (ZVS) or elimination of the reactive power at different power and voltage. While the previous work mainly focuses on the steady-state operation or the small-signal model for one specific modulation strategy, the real practice requires modulation strategies to switch among SPS, DPS and TPS frequently during the load transients, which can cause a current spike and dc-bias current in the transformer. Therefore, a smooth transition among different modulations is necessary. This paper proposes a duty-cycle compensation method to eliminate such current spike and DC bias. The implementation of the proposed method in the control loop is also discussed. Finally, the experimental results are provided to validate the performance of the duty-cycle compensation method.**

Index Terms — **Zero-Voltage-Switching, transformer current spike, current DC bias, phase shift control, dual active bridge.**

I. INTRODUCTION

Owing to the characteristics of bidirectional power flow and galvanic isolation, dual-active-bridge (DAB) converters can be implemented for various applications, for example, photovoltaic panel, battery, resistive load or the interface to other converters. To improve the steady-state performance, the modulation strategies of DAB have been explored, for example, single-phase-shift (SPS) [1, 2], dual-phase-shift (DPS) [3, 4] and triple-phase-shift (TPS) [5, 6] control. SPS modulation is applied on DAB converters at heavy load or when the input voltage is equal to the reflected output voltage. By inserting an additional phase shift into the primary-side or secondary-side H-bridge, DPS modulation exhibits lower loss or lower current stress than the SPS modulation. With various phase shifts, the transformer current can be designed to realize zero-voltage-switching [7, 8] and reduce the reactive power [3]. At light load or even no-load conditions, TPS modulation is another good candidate to replace SPS or DPS modulations. The inner phase shifts are applied at both H-bridges. To fully utilize the advantages of different control strategies, [9-12] answer how to integrate different modulation strategies through the wide operational range by using multiple-phase-shift modulation. The smooth transition among different modulation strategies is then necessary [13, 14]. The MPS modulation proposed in [12]

is a good candidate to realize ZVS for all switches by considering the transformer magnetizing current.

Besides the steady-state performance, dynamic performance is also important to meet the requirement when the load transient happens. To improve the dynamic performance, a small-signal model is built up to accurately describe the magnitude and the phase information in the frequency domain [15, 16]. Also [17] gives a detailed explanation of the influence by using digital control in real applications. [18] further explores the difference of small-signal models in different modulation strategies. However, because of the continuity of the current flowing through the transformer and the distinctive transformer current in different modulations, there are current spikes and DC bias when load or phase shifts change fast. The current spike incurs the saturation of the transformer and the external power inductor. For the safe operation, the current capability should be enlarged, which will increase the volume of the transformer or the external inductor. [19] brought up the phenomenon of the current spike in the transformer when load changes, which is the key factors in the unreliability of DAB and its proneness to failure during startup and power switching. Therefore, the elimination of such a current spike during load transients is important. [19] discussed the preliminary concept of DC bias during load transient. [20] provided the potential solution for specific modulations.
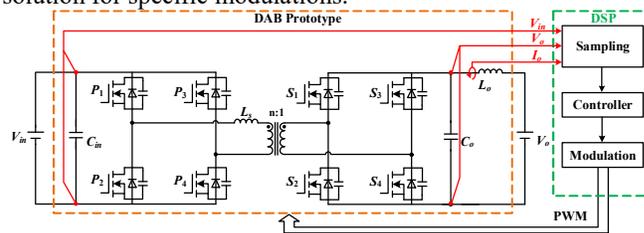
Fig. 1. A DAB converter with a digital control system.

In this paper, the comprehensive solution to eliminate the current spike and DC bias in the transformer during load transients is proposed by applying for the duty-cycle compensation. The implementation of the proposed method is also considered based on the digital control, which is shown in Fig. 1. For the structure of this paper, Section II describes a multiple-phase shift (MPS) modulation integrating SPS, DPS and TPS, and the current spike during load transition in the MPS control. Section III discusses the proposed duty-cycle compensation method to eliminate the current spike and DC

bias in the transformer when the load current changes. Section IV implements the proposed compensation method in control loop. Experiment results are shown in Section V to verify the proposed method.

II. MULTIPLE PHASE SHIFT MODULATION
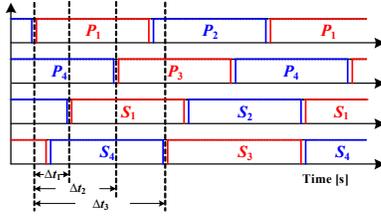
Fig. 2. Definition of different phase shifts.

(a)

(b)

(c)

(d)
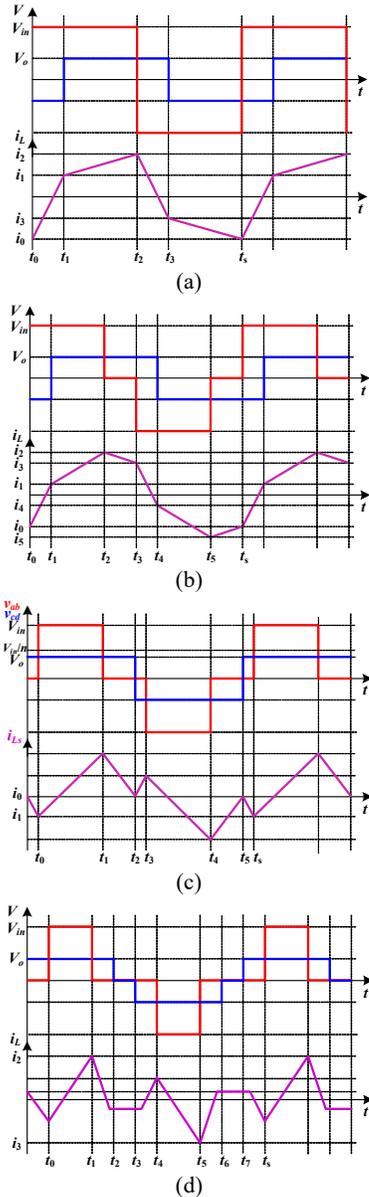
Fig. 3. Switching modes when $V_{in} > nV_o$: (a) SPS; (b) DPS1; (c) DPS2; (d) TPS.

Multiple-phase-shift modulation, such as SPS, DPS and TPS, has been well-developed to extend ZVS range in wide-voltage and full-load range. When the input voltage is not equal to the reflected output voltage, different modulation strategies can be applied at heavy load, medium load, or light load, respectively. When the inner phase shifts are applied to the primary-side or secondary-side H-bridges, a three-level voltage waveform appears at the related side of the transformer, introducing more time intervals in a single switching period.

All three phase shifts are defined as Fig. 2. $P_1 \sim P_4$ represent gate signals of primary-side switches and $S_1 \sim S_4$ are for secondary-side switches. All switches have a 50% duty cycle.

$$\begin{cases} \phi = \dfrac{\Delta t_1}{T_s / 2} \\ \phi_p = \dfrac{\Delta t_2}{T_s / 2} \\ \phi_s = \dfrac{\Delta t_3}{T_s / 2} \end{cases} \tag{1}$$

When the input voltage is higher than the reflected output voltage, the switching waveforms of different modulation strategies are shown in Fig. 3. The developed MPS modulation is aimed at extending the ZVS range for all primary-side switches within the full load range. At heavy load, SPS control is used to ensure ZVS for all switches, as shown in Fig. 3 (a). The phase shift in SPS control is shown below.

$$\begin{cases} \phi_p = 1 \\ \phi_s = 1 + \phi \end{cases} \tag{2}$$

With the power decreasing, the switching current at t_1 for secondary-side ZVS is decreasing. When the current is equal to I_{r1}, the minimum required current to finish ZVS transition for all secondary-side switches, the inner phase shift is applied at the primary side in Fig. 3 (b). The relationship between different phase shifts is shown below. With the proposed modulation strategy, the switching current at t_1 can be fixed at I_{r1}. However, the switching current at t_3 will continue increasing, which needs to be kept large enough to finish the ZVS transition for primary-side switches.

$$\begin{cases} \phi_p = \dfrac{nV_o - 4L_s f_s I_{r1}}{V_{in}} + 2\phi \\ \phi_s = 1 + \phi \end{cases} \tag{3}$$

Assuming the minimum required ZVS current is I_r, when the switching current decreases to I_r, a different DPS control strategy can be applied to the primary-side H-bridge in Fig. 3 (c). The relationship between the primary-side inner phase shift and the phase shift between the primary side and secondary side is shown in Eqn (4). By inserting the inner phase shift at the primary-side H-bridge, $P_1 \sim P_4$ can realize ZVS all the time. The drawback, however, is that $S_1 \sim S_4$ will lose ZVS within a certain range, although they can still realize ZVS at the light load.

$$\begin{cases} \phi_p = \dfrac{nV_o - 2nV_o |\phi| + 4L_s f_s I_r}{V_{in}} \\ \phi_s = 1 + \phi \end{cases} \tag{4}$$

At the light load, TPS control can take over to reduce the switching loss and conduction loss, as shown in Fig. 3 (d). The relationship between all the phase shifts is shown below.

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$$\begin{cases} \phi_p = \dfrac{nV_o + nV_o\phi + 2L_s f_s (I_r - I_{r1})}{V_{in}} \\[2mm] \phi_s = 1 - \dfrac{2L_s f_s (I_r + I_{r1})}{nV_o} \end{cases} \quad (5)$$

Although the application of MPS modulation can improve the performance of the DAB converter, to integrate different modulation strategies, the boundary conditions among different modulation strategies should be well defined. As summarized below, the boundary condition when switching from the SPS control to DPS1 control is

$$\frac{V_{in}(2\phi-1) + nV_o}{4L_s f_s} \le I_{r1}. \quad (6)$$

The boundary condition when switching from DPS1 to DPS2 is

$$\frac{V_{in} + nV_o}{2L_s f_s}\phi \le I_{r1} + I_r. \quad (7)$$

The boundary condition when switching from DPS2 to TPS is

$$-\frac{nV_o}{2L_s f_s}\phi \le I_{r1} + I_r. \quad (8)$$

With one phase leg at the primary side as the reference of phase shifts, the transformer current at t_0 has a significant difference in different modulation strategies. To realize a fast-dynamic response, a DAB converter should have the ability to regulate the load current swiftly. Hence, the value of phase

shifts will change dramatically in the following switching cycles, resulting in positive or negative current DC bias in the transformer. Fig. 4 shows an example of the transformer current spike in transient from light load to heavy load, where the modulation strategy switches from DPS to SPS.
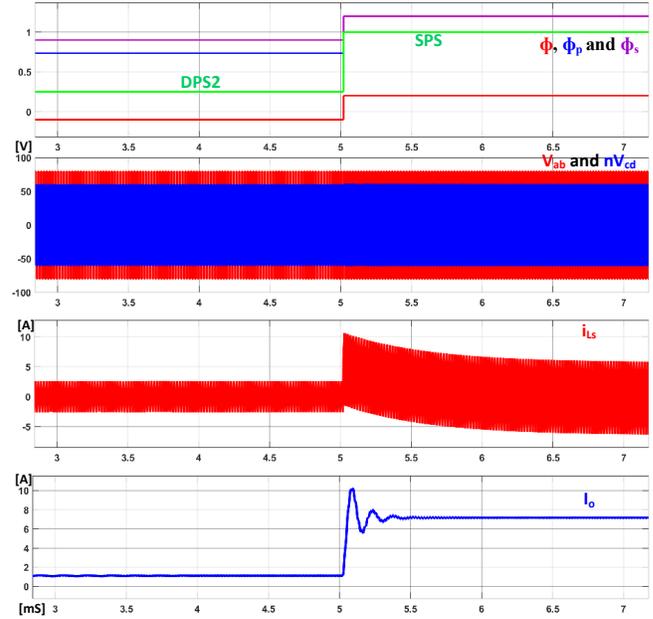
Fig. 4. Simulation waveform when a step change happens in the DAB converter based on MPS modulations.
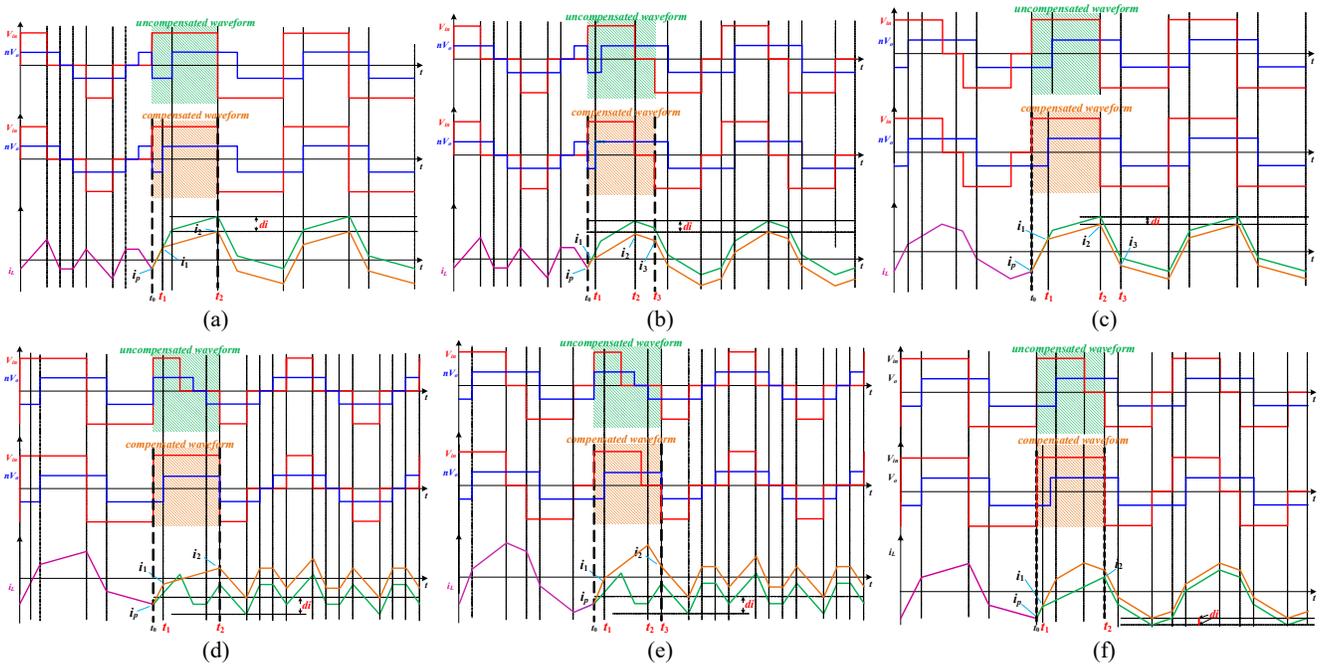
Fig. 5. Current Spike elimination: (a) modulation switching from TPS to SPS (light load to heavy load); (b) modulation switching from SPS to TPS (heavy load to light load); (a) modulation switching from TPS to DPS (light load to medium load); (b) modulation switching from DPS to TPS (medium load to light load).

III. DUTY CYCLE COMPENSATION TO ELIMINATE CURRENT SPIKE

The current spike mainly occurs when the phase shifts change drastically during load transients, especially when the modulation strategy needs to switch to another one. In addition, with the volt-second balance principle and the symmetry of the DAB operation, there will be a DC bias in the transformer current in the following switching cycles. Therefore, the modulation strategy in the next switching period after the load changes needs to be redesigned, right at the joint point between two different modulation strategies. Because the starting point and the endpoint of this switching cycle should be different for the sake of the smooth transition, the duty cycle of PWM signals should be adjusted instead of being kept at 50% as regular DAB modulations. To simplify such a design process, the modification of the modulation strategies in this paper mainly focuses on the first half switching cycle.

A. Load Current Increasing

As discussed in Section II, there are four modulation strategies to cover the full-load-range operation. Typically, P_1 is set as the time reference for all phase shifts. The basic reason causing the current spike during load transition is the difference between the switching current at the beginning of the switching cycle. For TPS control and DPS2 control, the switching current at t_0 is the same. Therefore, TPS and DPS2 control can be categorized as the same group in terms of the current spike elimination.

When the modulation strategy switches from TPS to SPS, to eliminate the positive current spike, the first interval when the transformer current is increasing needs to be limited in Fig. 5 (a). The current at the endpoint of TPS is I_r, which is the ZVS current for primary-side switches. In the first half switching period, switching actions at t_1 can be adjusted to limit the spike current. Meanwhile, the current at t_2 should reach the steady-state value to make sure the smooth transition between the TPS control and SPS control. To adjust the time interval from t_0 to t_1, duty cycles of $S_1 \sim S_4$ need to be calculated based on the equation below.

$$\begin{cases} t_1 = t_0 + \dfrac{com}{2f_s} \\ com = \dfrac{nV_o + V_{in}(\phi - \phi_p) + 2L_s f_s(I_r - I_{r1}) + nV_o\phi}{2nV_o} \end{cases} \quad (9)$$

By using a similar method, the current spike can also be eliminated when switching between other modulations. Fig. 5 (b) shows the current spike elimination from TPS to DPS1. In the next switching period, the inner phase shift of the primary-side H-bridge is kept the same. The duty cycles of secondary-side switches need to be modified. The time interval from t_0 to t_1 needs to be compensated is

$$com = \frac{nV_o - V_{in} + 4L_s f_s I_r + 2nV_o\phi}{4nV_o}. \quad (10)$$

Furthermore, when the modulation strategy switches from DPS to SPS, the designed compensation waveform is shown in Fig. 5 (c). There is no inner phase shift at the primary-side H-

bridge in the next half switching cycle. The compensation time interval from t_0 to t_1 is

$$com = \frac{nV_o + V_{in}(\phi_1 - 1) + 2L_s f_s(I_r - I_{r1}) + nV_o\phi_1}{2nV_o}. \quad (11)$$

B. Load Current Decreasing

In the transient process, there could be negative DC bias in the transformer current. For example, the current at the endpoint of SPS modulation is smaller than the current at the starting point of TPS modulation in steady-state. To make sure the switching current at the end of the half switching cycle is the same as the current in the next period, the transformer current needs to increase to the desired value by adjusting the relationship between $t_1 \sim t_0$ and $t_2 \sim t_1$ as shown in Fig. 5 (d). Hence the first interval from t_0 to t_1 is

$$com = \frac{nV_o - V_{in} + 2V_{in}\phi_1 - 4L_s f_s I_{r1} + 2nV_o(\phi + \phi_1)}{4nV_o}. \quad (12)$$

When the modulation strategy switches from DPS control to TPS control, there is also a negative DC bias current appearing in Fig. 5 (f). To eliminate such negative current DC bias, the inner phase shift at the primary-side H-bridge keeps the same as the last switching cycle. By changing the first period in the next half switching cycle, the transformer current can have enough time to rise to compensate for the negative DC bias. The calculated time interval from t_0 to t_1 is

$$com = \frac{nV_o - V_{in} + 4L_s f_s I_r + 2nV_o\phi_1}{4nV_o}. \quad (13)$$

Finally, to mitigate the potential negative DC bias when switching from SPS to DPS, the compensation method can also be applied to secondary-side switches in Fig. 5 (f). The necessary time interval from t_0 to t_1 is

$$com = \frac{nV_o + V_{in}(1 + 2\phi - 2\phi_p) - 4L_s f_s I_{r1} + 2nV_o(\phi_1 + \phi)}{4nV_o}. \quad (14)$$

By applying modified duty-cycle control to different switches, the transformer current spike, as well as the DC current bias during the load change, is eliminated.

IV. CONTROL ALGORITHM IMPLEMENTATION
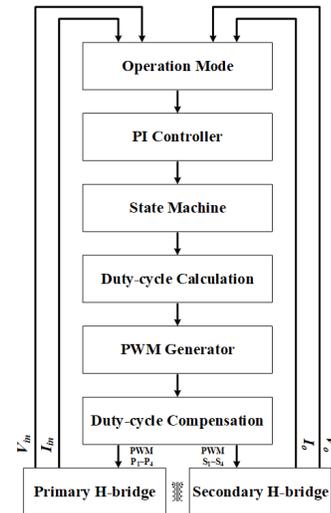
Fig. 6. Structure of the control loop in DAB.

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The structure of the control loop in a DAB converter is shown in Fig. 6. The operation mode can decide if the output voltage, output current or output power is regulated. The state machine can decide which modulation strategy is going to be implemented in the next switching cycle based on the input voltage, output voltage and the output of the PI controller, which is the phase shift between the primary side and the secondary side. The boundary conditions discussed in Section II can specify when it is necessary to switch modulation strategies. Then, based on the modulation strategy and the phase shifts in the current and next switching periods, the compensated duty cycle is calculated. A PWM generator will provide square waveforms for all switches with a 50% duty cycle. Modified duty cycles will then be applied to certain switches. Finally, a microcontroller generates PWM signals to different switches.
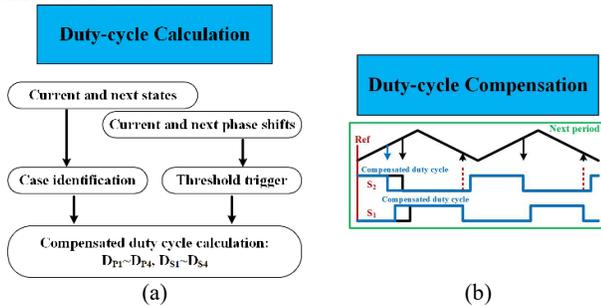
Fig. 7. Duty-cycle compensation method: (a) calculation of duty cycle; (b) implementation of compensation duty cycle.

The detailed duty-cycle calculation and compensation process are shown in Fig. 7. In Fig. 7 (a), as mentioned above, when the modulation strategy switches to another one, the duty-cycle compensation method is going to be triggered. At the same time, the change of the phase shift between the primary and secondary sides also needs to be large enough to cause the current spike or current DC bias in the transformer. An example

of the modification for S_1 and S_2 is shown in Fig. 7 (b). The duty cycle of S_1 is enlarged resulting in the time interval between t_0 and t_1 being reduced.

V. EXPERIMENT VERIFICATION

The prototype is built up to verify the proposed duty-cycle compensation method during load transients. The input voltage is 80V, the output voltage is 30V, the turn ratio of the transformer is 2, and the power inductance is 36μH. I_{r1} and I_r are set at 1A and 1.5A, respectively. The steady-state operations for SPS, DPS and TPS modulations are shown in Fig. 8. Switching waveforms in Fig. 8 (a)~(d) are close to the designed modulation in Section II. By linearly increasing the phase shift between the primary side and secondary side, the output current increases. The smooth transition in Fig. 8 (e) verifies the boundary conditions among different modulation strategies.

Without the duty-cycle compensation method, Fig. 9 (a) shows the current spike in the transformer appears when the load current suddenly increases. The maximum current during the load transient is 12A, which is 5A higher than the current at the steady-state current in Fig. 8. Fig. 9 (b) shows the negative current DC bias in the transformer when the load current suddenly decreases. The transformer current DC bias in the next switching cycle after the load transient is around 3A. But in the steady-state operation, there is nearly no dc-bias current in the transformer in Fig. 8. Fig. 10 shows experiment results with the implementation of the proposed duty-cycle compensation method. Fig. 10 (a)~(c) shows the current spike elimination when the load current increases. The maximum transformer current in the next switching cycle after load change is the same as the current at steady state. Fig. 10 (d)~(f) shows the DC bias elimination when the load current decreases. There is nearly no current spike or DC bias in the transient process like Fig. 9. The zoomed-in waveforms are also provided. The duty-cycle compensation in the first half switching cycle can all works as the design in Section III.
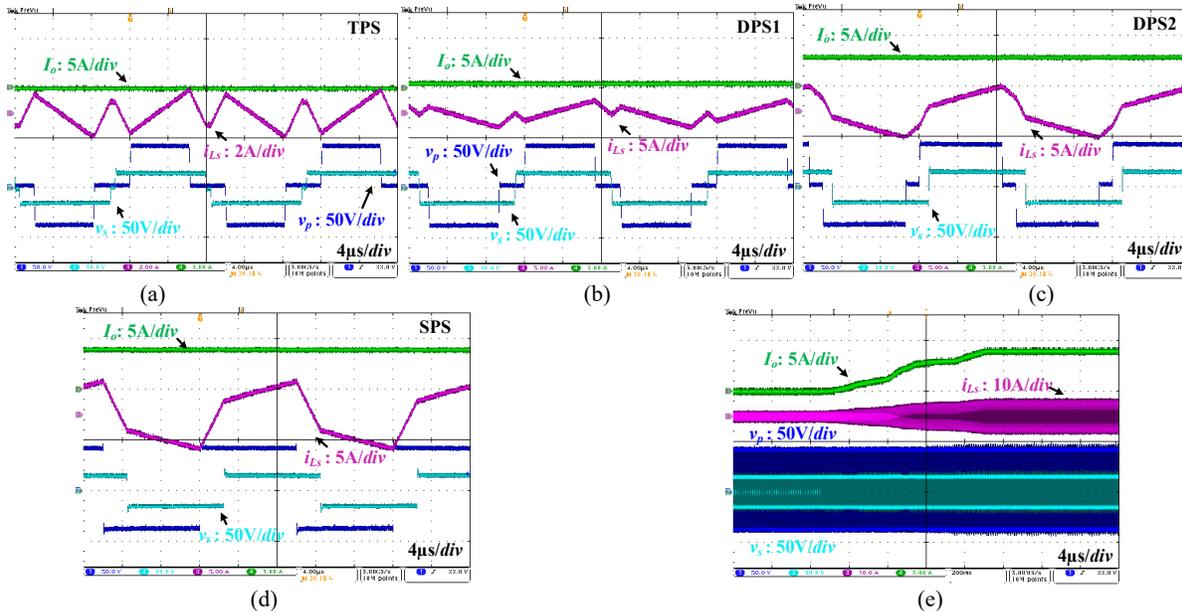
Fig. 8. Switching Waveforms for MPS modulation: (a) TPS; (b) DPS2; (c) DPS1; (d) SPS; (e) continuous transition among different modulation strategies.

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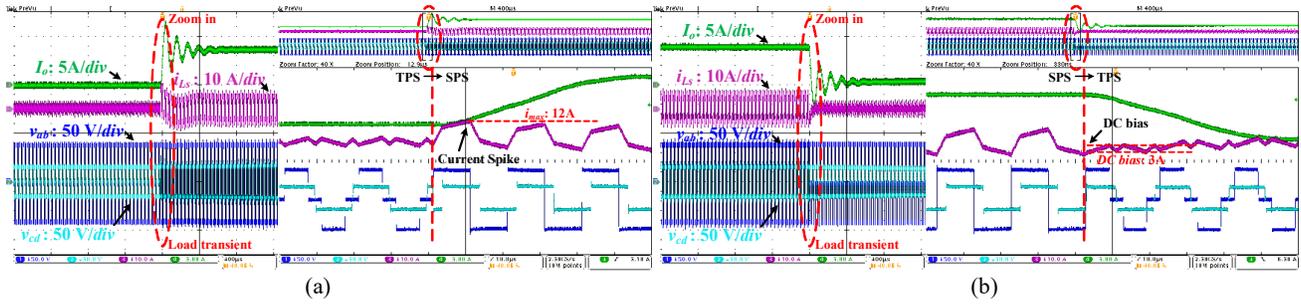
Fig. 9. Transformer current spike when step change of phase shift happens, without the duty cycle compensation: (a) from TPS to SPS; (b) from SPS to TPS.
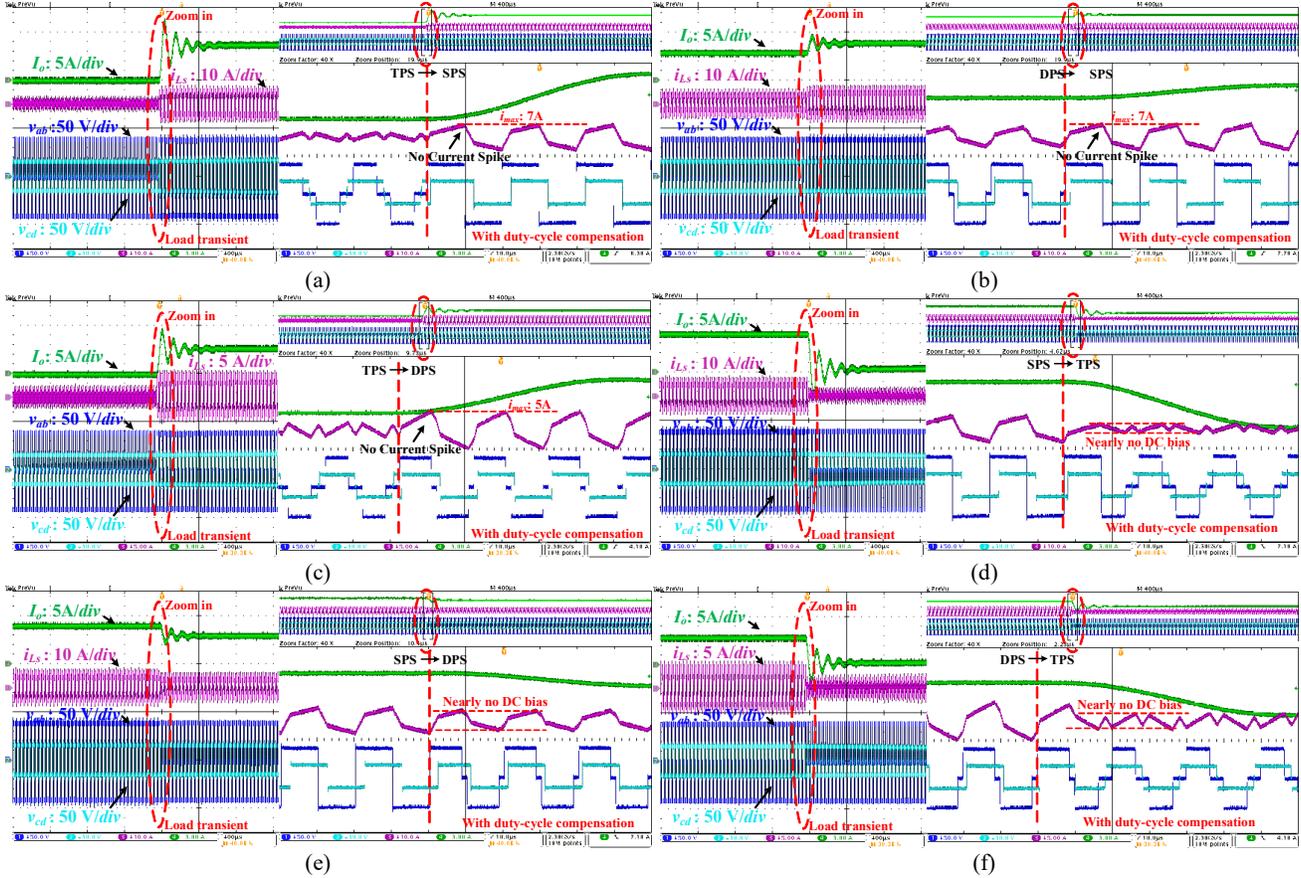
Fig. 10. Transition process among different modulations when load changes, with the duty cycle compensation: (a) from TPS to SPS; (b) from DPS1 to SPS: (c) from TPS to DPS1: (d) from SPS to TPS: (e) from SPS to DPS1: (f) from DPS1 to TPS.

VI. CONCLUSION

By applying the proposed duty-cycle compensation method during load transients in the DAB converter, the current spike and DC bias can be eliminated in the transformer. The compensated method mainly focuses on the first half switching cycle to simplify the design process. The design of the duty-cycle compensation mainly happens when switching from TPS to SPS, from TPS to DPS or from DPS to SPS. The test results are also provided to verify the proposed compensation method. Although in this paper we mainly focus on when the input voltage is higher than the reflected output voltage, it is worth noting that the same design principle applies when the reflected output voltage is higher than the input voltage. Therefore, the design procedure proposed in this paper can be a reference for the smooth transition among various modulation strategies without introducing any transformer current spike.

REFERENCE

[1] B. Hua, C. C. Mi, and S. Gargies, "The Short-Time-Scale Transient Processes in High-Voltage and High-Power Isolated Bidirectional DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 2648-2656, 2008.

[2] A. Rodriguez, A. Vazquez, D. G. Lamar, M. M. Hernando, and J. Sebastian, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Transactions on Power Electronics,* vol. 30, no. 2, pp. 790-804, 2014.

[3] B. Zhao, Q. Yu, and W. Sun, "Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid,"

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IEEE Transactions on Power Electronics, vol. 27, no. 11, pp. 4667-4680, 2012.

[4] B. Hua and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC–DC Converters Using Novel Dual-Phase-Shift Control," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 2905-2914, 2008.

[5] A. K. Das and B. G. Fernandes, "Fully ZVS, Minimum RMS Current Operation of Isolated Dual Active Bridge DC-DC Converter Employing Dual Phase-Shift Control," in *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019, pp. P. 1-P. 10: IEEE.

[6] J. Qiu, K. Shen, A. Tong, L. Hang, and J. Liao, "Unified ZVS strategy for DAB with triple-phase-shift modulation in boost mode," *The Journal of Engineering,* vol. 2019, no. 18, pp. 4906-4910, 2019.

[7] Y. Yan, H. Gui, and H. Bai, "Complete ZVS Analysis in Dual Active Bridge," *IEEE Transactions on Power Electronics,* vol. 36, no. 2, pp. 1247-1252, 2020.

[8] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics,* vol. 30, no. 2, pp. 985-995, 2014.

[9] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 29, no. 8, pp. 3954-3970, 2014.

[10] J. Lu *et al.*, "A Modular-Designed Three-Phase High-Efficiency High-Power-Density EV Battery Charger Using Dual/Triple-Phase-Shift Control," *IEEE Transactions on Power Electronics,* vol. 33, no. 9, pp. 8091-8100, 2018.

[11] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range," *IEEE Transactions on Power Electronics,* vol. 26, no. 4, pp. 1228-1236, 2011.

[12] G. Xu, L. Li, X. Chen, Y. Liu, Y. Sun, and M. Su, "Optimized EPS control to achieve full load range ZVS with seamless transition for dual active bridge converters," *IEEE Transactions on Industrial Electronics,* 2020.

[13] Z. Guo, "Modulation Scheme of Dual Active Bridge Converter for Seamless Transitions in Multiworking Modes Compromising ZVS and Conduction Loss," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 9, pp. 7399-7409, 2019.

[14] Y. Yan, H. Bai, A. Foote, and W. Wang, "Securing Full-Power-Range Zero-Voltage Switching in Both Steady-State and Transient Operations for a Dual-Active-Bridge-Based Bidirectional Electric Vehicle Charger," *IEEE Transactions on Power Electronics,* vol. 35, no. 7, pp. 7506-7519, 2019.

[15] D. Costinett, D. Maksimovic, and R. Zane, "Design and Control for High Efficiency in High Step-Down Dual Active Bridge Converters Operating at High Switching Frequency," *IEEE Transactions on Power Electronics,* vol. 28, no. 8, pp. 3931-3940, 2013.

[16] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC–DC converter," *IEEE Transactions on Power Electronics,* vol. 27, no. 4, pp. 2078-2084, 2011.

[17] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital control of high-frequency switched-mode power converters*. John Wiley & Sons, 2015.

[18] Y. Yan and H. Bai, "Dynamic Response Analysis Based on Multiple-Phase-Shift in Dual-Active-Bridge," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 1546-1551: IEEE.

[19] B. Zhao, Q. Song, W. Liu, and Y. Zhao, "Transient DC Bias and Current Impact Effects of High-Frequency-Isolated Bidirectional DC–DC Converter in Practice," *IEEE Transactions on Power Electronics,* vol. 31, no. 4, pp. 3203-3216, 2016.

[20] J. Hu, S. Cui, D. von den Hoff, and R. W. De Doncker, "Generic dynamic phase-shift control for bidirectional dual-active bridge converters," *IEEE Transactions on Power Electronics,* vol. 36, no. 6, pp. 6197-6202, 2020.