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RESEARCH ARTICLE

10 kV SiC MOSFET Based Medium Voltage Power Conditioning System for Asynchronous Microgrids

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ABSTRACT Distributed energy resources (DERs) and microgrids have seen tremendous growth and research activities in recent years. Flexible DERs and asynchronous microgrids (ASMG) can have many system-level benefits over fixed DERs and conventional microgrids. The key enabler for flexible DERs and ASMG is a power converter based power conditioning system (PCS) as the interface between DERs/microgrids and the medium voltage (MV) distribution grid. High voltage (HV, >3.3 kV) silicon carbide (SiC) based MV converter is now a promising solution for the PCS. This article presents development and testing of a 10 kV SiC MOSFET based MV PCS for 13.8 kV ASMG. MV PCS converter design addressing high dv/dt issue generated by fast switching of the 10 kV SiC MOSFET is presented. The developed PCS is successfully tested at 25 kV dc 13.8 kV ac voltages and 100 kVA power. Grid support functions are also demonstrated with the developed PCS prototype and hardware tests beds, validating HV SiC converter benefits for ASMG.

INDEX TERMS 10 kV SiC MOSFET, power conditioning system (PCS), medium voltage power converter, asynchronous microgrid (ASMG).

I. INTRODUCTION

A microgrid is a relatively small-scale local grid, with its own distributed generation sources, loads, and sometimes energy storage systems. As seen from the main utility grid, a microgrid can be regarded as a ''single controllable entity''. A microgrid can connect to the main distribution grid to work in ''grid-connected mode,'' serving the power and energy needs of both local loads and the main grid simultaneously, and even providing ancillary grid support functions. A microgrid can also be totally separated from the main grid to work in ''islanded mode,'' when the main grid becomes unavailable, or the grid power quality is not satisfactory [1]–[3]. Microgrids can increase reliability and

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resiliency, which is important for many critical infrastructures including manufacturing facilities [4]–[6]. Some distributed generation sources are provided by renewable energy resources (RES), especially solar PV, enabling microgrids to reduce their environmental impact for the electricity they provide.

Typical microgrids are ac synchronous microgrids, which are directly interfaced to and operate synchronously with main distribution grids in grid-connected mode. As a result of their direct coupling to the main grid, the design and operation of these microgrids are relatively complex. The challenges include voltage and frequency control, especially with integrated RES [7], [8], poor dynamic performances of mode transitions [9], [10], complex stability consideration and protection strategies [11], [12]. To mitigate these issues, a different microgrid concept was proposed, which is named asynchronous microgrid (ASMG) [13]. An ASMG connects to an ac distribution grid through a microgrid power conditioning system (PCS). As shown in Figure 1, the ASMG PCS can be made up with two back-to-back ac/dc converters, similar to back-to-back high voltage dc (HVDC) converters in connecting two asynchronous ac transmission grids. Different from back-to-back converters in HVDC and wind power applications, the PCS in ASMG needs to support microgrid unbalanced loads, multiple operation modes and mode transitions.

Compared with typical ac synchronous microgrid, the ASMG has decoupled dynamics with the distribution grid. Consequently, it provides several system-level benefits: 1) easier integration of RES into microgrids without the need to consider interaction between RES and the distribution grid; 2) better under voltage and under frequency ride-through capability; 3) easier transition between grid-connected and islanded modes, and elimination of the need for resynchronization control; and 4) isolation of unbalance and faults, for easier microgrid protection coordination and control. Furthermore, PCS converters can provide independent var support to microgrids and main grids, and even allow integration of energy storage and other distributed resources through its dc link.

Previous publications on ASMG mainly focus on the demonstration of system-level benefits provided by system architecture. The ASMG network and potential application cases are discussed in [13]. In [14], an ASMG is proposed for New York City, and ASMG benefits are demonstrated through simulation, including disturbance decoupling, fault isolation, etc. A novel load balancing strategy is proposed to show the unbalanced load support benefit provided by the ASMG PCS in [15]. Although the PCS is the key to ASMG, very limited research has focused on actual hardware implementation of the PCS and rare full scale PCS has been reported. It is challenging to have a suitable PCS, because it can add cost, size, and power loss of the system, especially given that today's PCS is based on lossy and relatively slow switching Si technology. As a result, there are almost no real applications for asynchronous ac microgrids.

In recent years, with the development of high voltage (HV) SiC MOSFETs, medium voltage (MV) converters based on these devices have become a promising solution for ASMG PCS. HV SiC MOSFETs can realize high switching frequency with low switching loss, which can reduce the size of passive components and achieve high control bandwidth. HV SiC devices can simplify converter topology to reduce the control complexity [16], [17]. Furthermore, the high control bandwidth enabled by HV SiC devices can lead to more system-level benefits such as improved system stability and power quality [18], [19]. 10 kV SiC MOSFET based ASMG PCS has been studied recently. A back-to-back connected PCS converter employing 10 kV SiC MOSFET-based three-level neutral power clamped converters (3L-NPCs) is demonstrated for a 13.8 kV grid in [20]. However, device series connection is required in this case. Compared with the 3L-NPC converters, modular multi-level converters (MMCs) can achieve better modularity and scalability, which are desired features for grid applications.

This article presents a 10 kV SiC MOSFET and MMC topology based PCS for a 13.8 kV microgrid. 10 kV SiC based MV PCS subsystem design addressing high dv/dt issue is presented. Full voltage and power back-to-back PCS testing and system-level benefits demonstration with the developed MV PCS are presented.

The organization of this article is as follows. Section II overviews benefits of HV SiC based PCS for an ASMG. Section III presents the 10 kV SiC MOSFET based MV PCS design. Section IV provides the PCS testing and system-level benefit demonstration. Section V concludes this article.

II. BENEFITS OF HV SiC MOSFET BASED PCS FOR ASMG

There are in general three ways that HV SiC MOSFET can benefit microgrid applications including direct device substitution, topology simplification, and new or enhanced functionality or even new application.

Due to lower power loss of SiC devices over Si devices, a direct substitution using SiC device can lead to gains in efficiency and corresponding reduced need for cooling.

HV SiC devices have higher breakdown voltage than Si and LV SiC devices. In addition, SiC device can switch much faster than Si device. As a result, converter design can be simplified, especially, those topologies requiring many series/paralleled Si devices or many levels to achieve needed voltage level or needed equivalent switching frequency. Most converters for medium voltage applications exceed the voltage capabilities of the available Si devices (e.g. the highest Si IGBT voltage is 6.5 kV). In addition, the HV Si devices have limited switching capabilities (e.g. the 6.5 kV Si IGBT normally switches at around 1 kHz), resulting large pulsating ripple or energy. Thus, multi-level converters, paralleled converters, and/or large passive components for filtering and energy storage will be needed. With higher voltage and faster switching SiC devices, the need for complex topology and large filter can be alleviated. The topology simplification

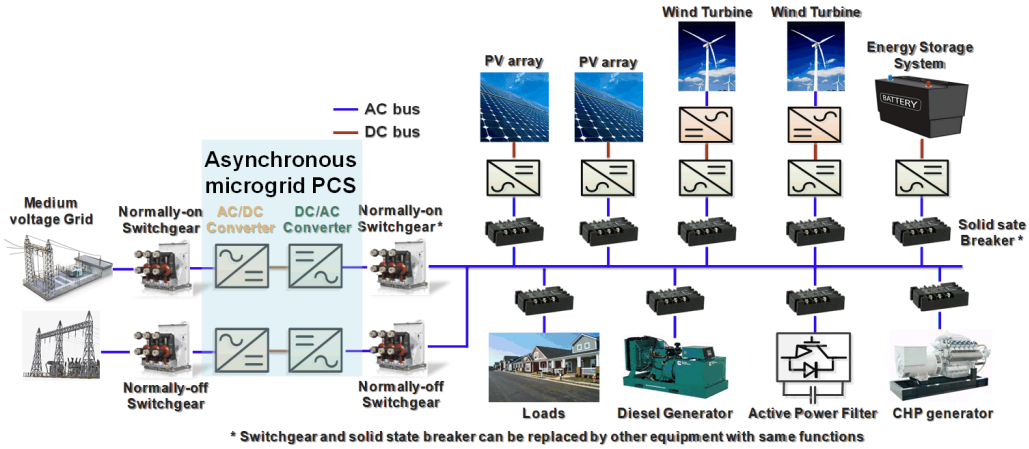

FIGURE 1. Configuration of a MV ASMG.

could lead to lower cost, higher power density and higher reliability.

With high switching speed and switching frequency, HV SiC devices can also enable power converters with high control bandwidth and faster dynamic response. These features can lead to enhanced or new functionality for microgrid. For example, the active power filtering (APF) function can be integrated into the PCS, given the switching frequency is much higher than the harmonic frequencies. The integration can reduce the need for dedicated APF, leading to lower overall converter rating and cost. For interruption equipment like solid-state circuit breaker (SSCB) and solid-state fault current limiter (SSFCL), HV SiC device can potentially speed up the response time and improve system reliability. The high control bandwidth of PCS enabled by HV SiC can also be used in stabilizing the system.

A case study in [21] shows that, at converter level, for a 1 MW MV PCS, the SiC based PCS solution can achieve >80% weight and size reduction and >10X control bandwidth compared with Si based PCS solution. At system level, simulation studies demonstrate that the higher control bandwidth offered by the HV SiC MOSFET enables more grid support functions of the PCS including power quality improvement, system stability enhancement, and dynamic performance improvement in fault ride-through, mode transition, and black start. The potential system-level benefits of ASMG with PCS as well as SiC based PCS are summarized in Table 1.

III. 10 kV SiC MOSFET BASED MV PCS DESIGN

This section presents the 10 kV SiC MOSFET based MV PCS overall design considering grid requirements and subsystem components design addressing high *dv*/dt issue.

A. OVERALL PCS DESIGN CONSERDING GRID REQUIREMENTS

1) PCS TOPOLOGY SELECTION

The PCS is interfacing 13.8 kV ac rms voltage distribution grid and asynchronous microgrid. A 25 kV dc bus voltage is selected which requires a modulation index of 0.9. With the high blocking voltage of the 10 kV SiC MOSFET, a five-level converter topology can be adopted to achieve the desired 25 kV dc bus voltage and 13.8 kV ac voltage. Three mainstream five-level topologies, including five-level neutral point clamped (5L-NPC) converter, five-level flying capacitor (5L-FC) converter, and five level modular multilevel converter (MMC) with four submodules in one arm, are considered as candidates.

The 5L-NPC converter and 5L-FC converter can achieve smaller size and weight compared to MMC because MMC topology requires bulky capacitors to filter the low frequency harmonics. However, the NPC and FC based converter are not modular and scalable. The 5L-NPC and 5L-FC based converters also have complicated switching commutation loops and capacitor voltage balancing control. This poses overvoltage risk for 10 kV SiC MOSFET based PCS which has much faster switching transients than Si IGBTs. On the other hand, MMC topology has inherent modular structure. Thus, MMC has excellent scalability for higher voltage and power and the inherent redundancy to tolerate component failure in the submodule [22], [23]. The MMC submodule has simple switching communication loop like the two-level converter. The modular structure also makes it easier to design and test the converter based on the emerging 10 kV SiC MOSFETs. For grid applications, modularity, scalability, and reliability are more desired features than size and weight. Therefore, MMC topology is selected for PCS.

For grid application, the PCS should be able to provide unbalanced load support on the microgrid side. As a result, the modulation strategies with 3rd order harmonic injection cannot be used, although they have better voltage utilization and require lower dc bus voltage. The selected modulation scheme is hence the pure sinusoidal pulse width modulation (SPWM) without any 3rd order harmonic injection. The split dc-link capacitor structure is adopted to support unbalanced load in the microgrid [24]. The split dc-link capacitor method is a cost-effective and straightforward scheme to realize the neutral line for the unbalanced load on the microgrid side, compared to other solutions, such as the topology with

TABLE 1. Potential system-level benefits of the SiC based ASMG PCS.

Use case	Benefits of ASMG PCS	Benefits of SiC
Grid-connected mode		
Frequency & voltage control	Simple for a) reactive power support, for both grid and microgrid sides independently; b) power transfer control	Not significant (smaller filter can have more var), overall faster dynamic response
Stability	Isolation -can isolate stability issue of microgrid and generally simplify the design for stability, enabling easy integration of RES in microgrid. A microgrid stable in islanded case can be more easily integrated with the distribution grid. Oscillation damping & voltage stability – easier inertia emulation & var support	Stability – faster SiC can help control and impedance forming Oscillation damping – faster SiC can help with inertia emulation & var support
Power quality	PCS converters can provide active power filtering (APF) functions for both distribution grid and microgrid. Can save dedicated filters.	APF function only effective with fast SiC
Low voltage ride through	No voltage drops in microgrid, load voltage maintained	Better dynamic response
Multi-feeder microgrid	Simple to achieve microgrid with multiple feeders: a) no need for information on voltage amplitude and phase of feeders; b) simple to isolate from the fault feeder and maintain the connection with other feeders.	Not obvious
Short circuit current	Short circuit current will be reduced with ASMG, as the interface converters will isolate/limit fault current contributions	Not obvious
Efficiency	Will incur additional loss during normal operation – a drawback of ASMG PCS	SiC can have lower power loss than Si
Islanded mode		
Transition	Seamless transition between grid connected and islanded modes, no voltage drop in microgrid	Better dynamic response
Frequency & voltage control	Microgrid side PCS provides var support	Not obvious
Stability	PCS could be a stabilizer	SiC can help control and impedance forming
Power quality	Microgrid side PCS converter can provide APF function, reducing or eliminating need for dedicated filters	APF function only effective with SiC
Black start	Black start is easy with microgrid PCS, but not obvious benefit over traditional islanded microgrid	Not obvious
Other benefits: The interface converters can integrate energy storage, combined heat & power (CHP)/local generation, and fault current limiting/protection functions.		

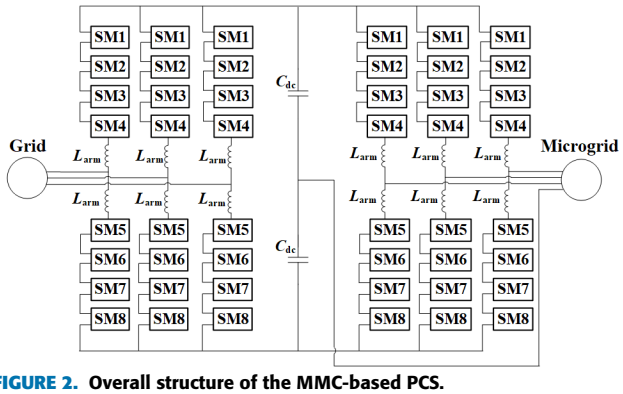

FIGURE 2. Overall structure of the MMC-based PCS.

a neutral leg and adding a neutral forming transformer [25]. Figure 2 shows the overall structure of the MMC-based PCS.

2) DC-LINK CAPACITOR, ARM INDUCTOR, AND SUBMODULE CAPACITOR DESIGN

The dc-link capacitance of MMC is determined by the unbalanced load. Under the unbalanced load condition, the zero sequence current flows into the dc-link midpoint causing voltage ripple. Considering two phases full load and the other phase no load condition which is the worst load unbalance case, a 6.25 uF capacitance is required and selected to limit the voltage ripple within 10%.

The arm inductor of MMC is used to suppress the circulating current as well as served as the filter inductor between the inverter and power grid. It is cost-effective to eliminate dedicated ac side filter. The arm inductance is selected based on two considerations: circulating current suppression with circulating current control considered and THD requirement of the current in ac side [26]. The arm inductance is determined as 90 mH which can ensure $< 5\%$ THD of the current on ac side and $< 10\%$ arm current ripple.

With 25 kV dc-link voltage, the nominal submodule capacitor voltage is 6.25 kV. The designed submodule capacitance is 6 μF to meet the 20% peak-to-peak voltage ripple target [27]. Four 1900V/35μF film capacitors from AVX Corporation are connected in series to serve as the submodule capacitor, leading to a submodule capacitance of 8.75 μF. Such implementation ensures that the submodule capacitor voltage is lower than 7 kV, which is also the blocking voltage of 10 kV SiC MOSFETs in the submodule.

3) PCS CONTROLLER DESIGN

The PCS architecture follows the IEEE guide 1676-2010 [28], which is for MV power converters. The PCS controller

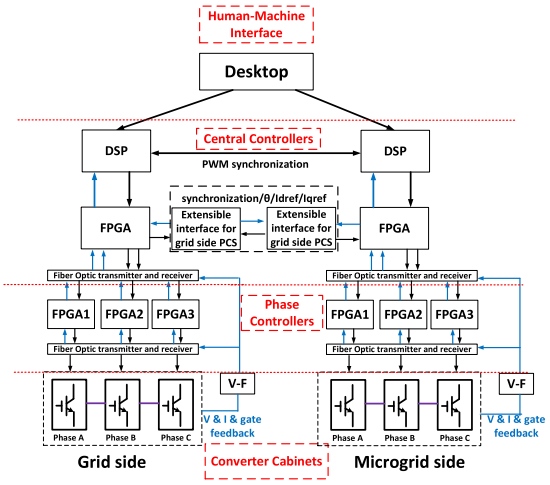

FIGURE 3. ASMG PCS control architecture.

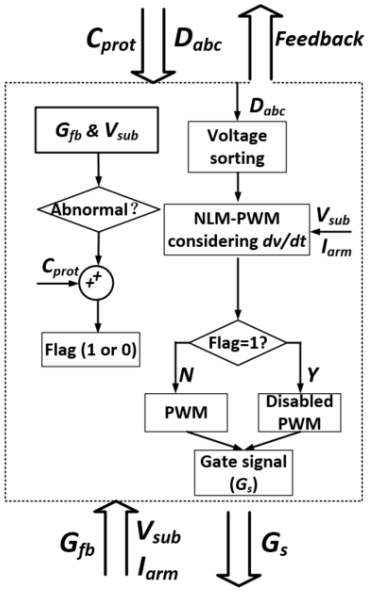

FIGURE 4. PCS converter single phase controller function block diagram.

architecture is shown in Figure 3, which contains the human-machine interface, central controllers, and phase controllers. To achieve modular setup and operation, the grid side and microgrid PCS converters have their own central controllers. Each ac/dc PCS converter is composed of three phase-leg cabinets and each phase-leg cabinet has its own phase controller so that the phase-leg can also be debugged independently. The modular design approach simplifies the PCS debugging and improves the implementation efficiency.

The grid side and microgrid side PCS converters have different system level functions. The grid side converter mainly operates in the grid-connected mode, and the central controller needs to regulate the dc-link voltage and provide reactive power to the grid. The grid side PCS also has the local islanding detection function to detect the abnormal grid condition and enable the islanding transition locally.

With the transformer-less PCS converter topology, the dc-link midpoint is grounded to provide microgrid side grounding. As a result, the grid side PCS converter will provide a path for zero-sequence current from the grid side, which is undesirable. A zero-sequence current control is implemented in the grid side PCS converter to regulate the low-frequency zero-sequence current within the control bandwidth. The high frequency zero-sequence current due to switching is limited by the arm inductors.

The microgrid side PCS converter operates both in grid-connected and islanded mode. In the grid connected mode, the microgrid side PCS regulates the microgrid ac voltage magnitude and frequency. In the islanded mode, it controls the dc-link voltage and provides microgrid with reactive power. Moreover, the PCS converter can work as an active power filter (APF) to improve the microgrid power quality. In both operation modes, the microgrid side PCS converter also supports the unbalanced load of the microgrid.

The phase controller is responsible for converting the duty cycles calculated by the central controller to PWM signals and realizing converter protections. Each phase controller controls one phase leg, and the phase controller functions for grid side and microgrid side PCS converter are the same. As shown in Figure 4, the phase controller functions include modulation, MMC submodule voltage balancing control and converter protections.

B. SUBSYTEM DESIGN CONSIDERING HIGH DV/DT

The switching action generated dv/dt of the 10 kV SiC MOSFET can be as high as 100 V/ns, which is nearly 30 times higher than conventional HV Si IGBTs. High dv/dt poses great challenges for the noise immunity and insulation design. MMC submodule, which is the basic unit for MMC, includes 10 kV SiC MOSFETS based half bridge, gate driver, isolated power supply, and voltage sensors as shown in Figure 5. The MMC submodule components design to address high dv/dt and high voltage insulation are presented. Modulation strategy for dv/dt reduction of MMC is also briefly discussed.

In the submodule PCB design, the clearance distance requirements in IPC-2221B standard [34] and the creepage requirements in UL 60950-1 standard [35] are followed to ensure adequate insulation.

1) 10 kV SiC MOSFET CHARACTERISTICS

The Wolfspeed 3rd generation 10 kV /20 A discrete SiC MOSFET (XPM3-10000-0350B) is used [29]. With a non-isolated package, the 10 kV SiC MOSFET has the die soldered on a copper plate which serves as the drain terminal and heat dissipation plate simultaneously, as shown in Figure 5.

The measured forward conduction characteristic of the 10 kV SiC MOSFET at 25°C is shown in Figure 6. Once the gate-source voltage V_{gs} exceeds 13 V, the on-resistance is almost constant when device current is lower than 20 A, because the on-resistance is dominated by the resistance in the drift region instead of the channel resistance. The on-state

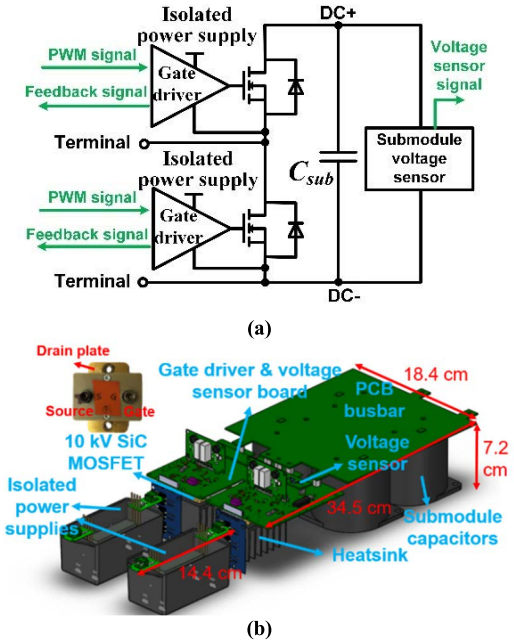

FIGURE 5. 10 kV SiC MOSFET based MMC submodule: (a) schematic; (b) 3D design of the submodule.

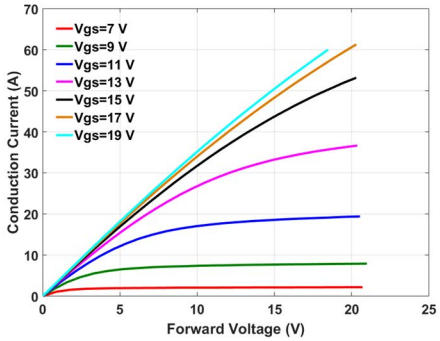

FIGURE 6. Forward I-V characteristic of the 10 kV SiC MOSFET at 25 °C.

V_{gs} is selected to be 15V which is a tradeoff between on-state conduction loss and short-circuit withstand time.

One feature of the 10 kV SiC MOSFET is its much larger input capacitance, compared to 1.2 kV and 1.7 kV SiC MOSFETs with similar current rating from Wolfspeed. For example, the 1200V/20 A SiC MOSFET from Wolfspeed has an input capacitance C_{iss} of 350 pF, about 6% of the input capacitance of this 10 kV SiC MOSFET as shown in Figure 7. Meanwhile, Miller capacitance C_{rss} of the 1.2 kV and 1.7 kV SiC MOSFET is close to that of 10 kV SiC MOSFETs. Therefore, the cross-talk issue caused by Miller current is greatly alleviated in the 10 kV SiC MOSFET by its large ratio between input capacitance and Miller capacitance C_{iss}/C_{rss}.

Figure 8(a) and (b) show the measured turn-on and turn-off switching transient waveforms. Figure 8(c) and (d) shows the measured turn-on and turn-off average dv/dt with different gate resistances. With 15 Ω turn-on gate resistance and 3 Ω

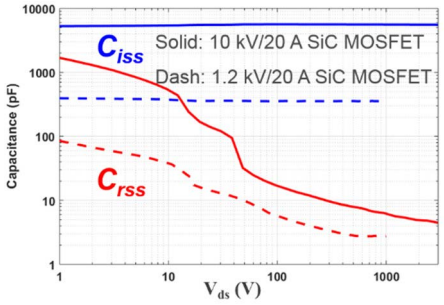

FIGURE 7. Parasitic capacitances C_{iss} and C_{rss} of 10 kV/20 A SiC MOSFET.

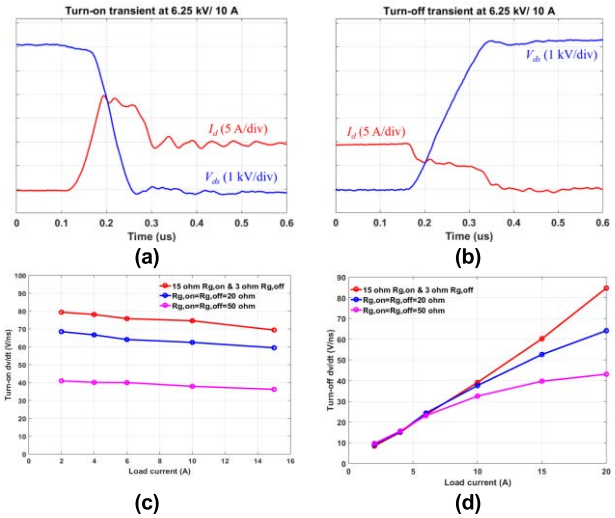

FIGURE 8. Switching characteristics of 10 kV SiC MOSFET at 6.25 kV and 125°C. (a) turn-on transient, (b) turn-off transient, (c) turn-on dv/dt and (d) turn-off dv/dt.

turn-off gate resistance, the dv/dt is limited to be within 100 V/ns. For this 10 kV SiC MOSFET, the turn-off transient is dominated by capacitive charging process and hence not a strong function of gate resistance, especially at low current.

2) GATE DRIVING AND PROTECTION

Gate driver for the 10 kV SiC MOSFET is designed to support robust continuous operation and fast switching speed. The main challenges are high voltage insulation and high dv/dt (up to 100 V/ns).

The on-state and off-state driving voltage are selected as 15 V and −5 V, respectively. 15 V is chosen in order to balance the need of reduced short circuit current and low on-state loss, and −5 V for off-state can ensure reliable turn-off under high dv/dt. The turn-on and turn-off gate resistance are 15 Ω and 3 Ω, respectively, which provide both low switching loss and acceptable dv/dt, based on switching characterization results. Anti-cross-talk circuitry is not needed for this 10 kV SiC MOSFET due to the large ratio between input capacitance and Miller capacitance.

The designed gate driver diagram is shown in Figure 9. Functions including status feedback function, dead time

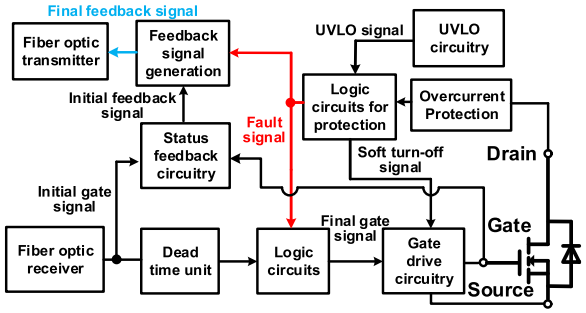

FIGURE 9. Function diagram of the designed 10 kV SiC MOSFET gate driver.

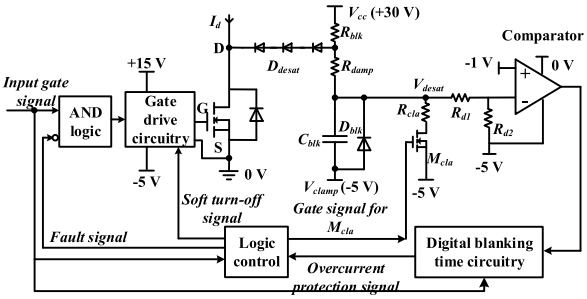

FIGURE 10. Desat protection circuit of the 10 kV SiC MOSFET.

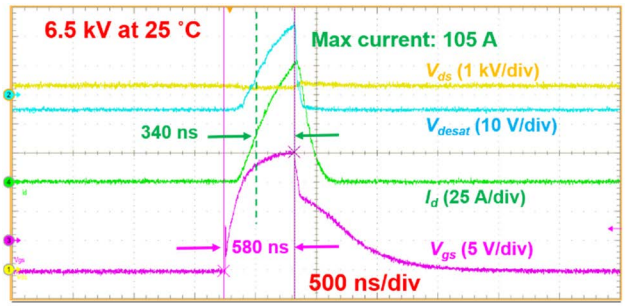

FIGURE 11. HSF short circuit test of the lower MOSFET in MMC submodule at 6.5 kV dc bus voltage.

insertion, undervoltage lockout, and short-circuit protection are implemented to support robust operation of the MMC submodule. Status feedback signal in every switching cycle is generated based on the measured gate-source voltage, which is necessary for the controller to monitor the status of the gate driver and the MOSFET during the continuous operation. If a short circuit or overcurrent fault is detected, a fault signal is sent back to the controller via the feedback signal. Isolation between gate driver and microcontroller is achieved through fiber optic.

Desat protection technique is widely adopted for MOSFET short circuit protection. Fast response time while maintaining strong noise immunity under dv/dt is required for this 10 kV SiC MOSFET. Fig. 10 shows the desat protection circuit design for this 10 kV SiC MOSFET. Three 3.3 kV SiC Schottky diodes are connected in series as the desat diode to achieve the required blocking voltage as well as low parasitic capacitance. The protection threshold voltage is selected based on the I-V characteristics of the MOSFET and the desired protection threshold current. An improved desat protection scheme is designed which realize 600 ns blanking time by digital ICs so that the blanking time is independent of the blanking capacitor. Then a much smaller blanking capacitance can be used which significantly accelerates protection response. Hard switching fault (HSF) short-circuit test shown in Figure 11 demonstrates the fault can be cleared with a response time of 340 ns with the designed improved desat protection.

The desat protection can be falsely triggered by both high positive dv/dt during turn-off and negative dv/dt during turn-on. The main concern with high negative dv/dt is the resulting negative voltage spike which can falsely trigger the desat comparator with the phase reversal issue. The noise immunity under negative dv/dt is improved by selecting comparators without phase reversal issue and adding clamping diodes. High positive dv/dt can falsely trigger desat protection by generating a positive voltage spike in V_{desat} (shown in Figure 10). In addition to reducing the desat diode parasitic capacitance as discussed in literature, minimizing the capacitive coupling between the protection circuitry and the drain terminal with high dv/dt is more critical for this 10 kV SiC MOSFET. Because of the long duration time of the high dv/dt generated by the 10 kV SiC MOSFET (much longer than the 1.2 kV and 1.7 kV SiC MOSFETs), very small parasitic capacitance coupled (<0.1 pF) from the device drain terminal to the voltage divider and comparator input could have large influence on the noise induced into the desat protection circuitry. Attention should be paid to the layout design of the protection circuitry to reduce this capacitive coupling. A copper shielding layer beneath the desat protection circuitry can be considered to reduce this capacitive coupling. Reducing the voltage divider impedance (R_{d1} and R_{d2} shown in Figure 10) will also help to reduce the coupled noise.

3) ISOLATED POWER SUPPLY

The isolated power supply, with an insulation voltage of 20 kV or higher, is expected to supply the gate driver for 10 kV SiC MOSFET, to provide a safe and reliable insulation barrier between the MV power stage and the control circuit. Due to the high dv/dt up to 100 V/ns generated by the 10 kV SiC MOSFET, the isolated power supply should also have low interwinding capacitance, typically below 5 pF, between the input and output, to limit the common-mode current which may cause control system malfunction.

The flyback converter topology is selected for this isolated power supply as it has simple structure and low component count. The input and output voltage are 12 V and 24 V, respectively. The output power is 2.5 W. The output voltage is regulated by closed-loop control. The printed circuit board (PCB) winding based transformer is adopted. Figure 12 shows the developed isolated power supply. Measured

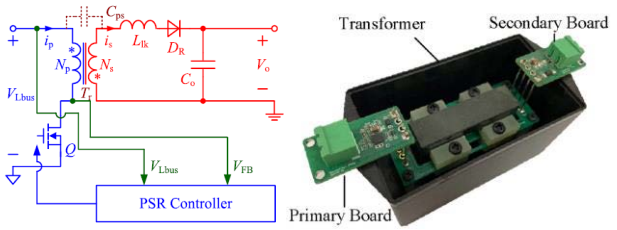

FIGURE 12. The isolated power supply schematic and prototype.

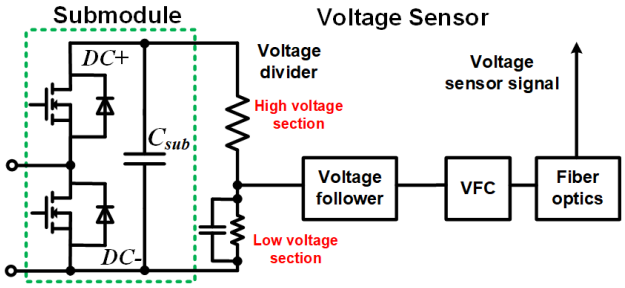

FIGURE 13. Block diagram of the designed submodule voltage sensor.

efficiency is between 66% and 80% from very light load to full load.

To achieve above 20 kV insulation capability, silicone gel is utilized for the flyback transformer potting. The air between transformer core and winding is fully removed with vacuum potting technique. Insulation capability of the transformer is tested and verified with hi-pot and partial discharge (PD) test.

Finite element simulations are conducted to investigate the impact factors on transformer interwinding capacitance. To reduce the interwinding capacitance, the PCB trace's width-to-thickness ratio should be reduced, the winding-to-core distance needs be swept to find the optimal point achieving minimum winding-to-core capacitance, the winding turns should be reduced, and low dielectric constant insulation material should be adopted. With these guidelines, the transformer is carefully designed and implemented and achieved 1.85 pF interwinding capacitance.

4) VOLTAGE SENSOR

Voltage sensor is used to measure voltage of the MMC submodule for realizing submodule voltage balance control of the MMC. It can also be used to detect the submodule overvoltage fault. The voltage sensor is connecting the MV power stage and the control circuit and thus should provide sufficient insulation barrier between the two parts for safe and reliable operation. The voltage sensor should also have good noise immunity capability and not be interfered by the high dv/dt generated by the 10 kV SiC MOSFET.

The designed voltage sensor for the MMC submodule is shown in Fig. 13, which can measure submodule voltage up to 8 kV. The voltage sensor first measures the differential voltage between the submodule positive and negative dc terminals through a voltage divider. The voltage divider steps down the submodule voltage with a ratio of 935:1, which is designed based on requirements in UL-347A [33]. The measured analog voltage signal is converter to a digital PWM signal through a voltage-to-frequency converter (VFC). This signal is then sent to the controller through fiber optic, which provide a reliable insulation barrier between MV power stage and the controller. The frequency of the generated output signal of the voltage sensor is proportional to the submodule capacitor voltage with a resolution of 2.02 V/kHz.

The noise is mainly caused by the displacement current in the parasitic capacitances between the switch node of the half bridge and the PCB trace of the voltage divider. In a compact SM design, the voltage sensor is very close to the power stage, resulting in a 0.1∼1 pF parasitic capacitance which cannot be neglected, especially for the 10 kV SiC MOSFET with high dv/dt. To achieve strong noise immunity, the voltage sensor layout is optimized to minimize the capacitive coupling between switch node and the voltage divider, voltage divider impedance is reduced, and a RC filter is implemented. The developed voltage sensor has good noise immunity and successfully supported the submodule voltage balancing and full power testing of the MMC.

5) MODULATION FOR DV/DT REDUCTION

The nearest-level pulse width modulation (NLM-PWM) is very attractive for MMC with a small number of submodules and thus is preferred for MV applications with HV SiC devices. There is one submodule that operates in PWM mode while others are in inserted mode or bypass mode. The conventional voltage balancing control (VBC) with NLM-PWM has been provided in [30]. In the conventional VBC with NL-PWM, several submodules may switch their modes simultaneously when the voltage sorting changes, resulting in a higher dv/dt, which could be multiple times of the dv/dt of a single 10 kV SiC device. For N submodules, the highest dv/dt will be N/2 times of the dv/dt of a single 10 kV SiC device.

The dv/dt can be limited if only two submodules switch their modes in a control cycle when the voltage sorting changes. With this principle, an improved VBC method with dv/dt reduction is proposed in [31]. With this modulation method implemented for the developed MMC converter, the maximum dv/dt in the MMC can be limited to be the dv/dt of a single 10 kV SiC device, while the submodule voltage balance can be maintained.

IV. 10 kV SiC MOSFET BASED MV PCS TESTING AND GRID SUPPORT FUNCTION DEMONSTRATION

This section presents the 10 kV SiC MOSFET based 100 kVA MV PCS hardware, testing, and grid support function demonstration.

A. PCS HARDWARE AND TEST SETUP

Figure 14(a) shows one phase-leg hardware of the PCS converter including eight submodules, two arm inductors, and a phase controller. The back-to-back PCS contains six such

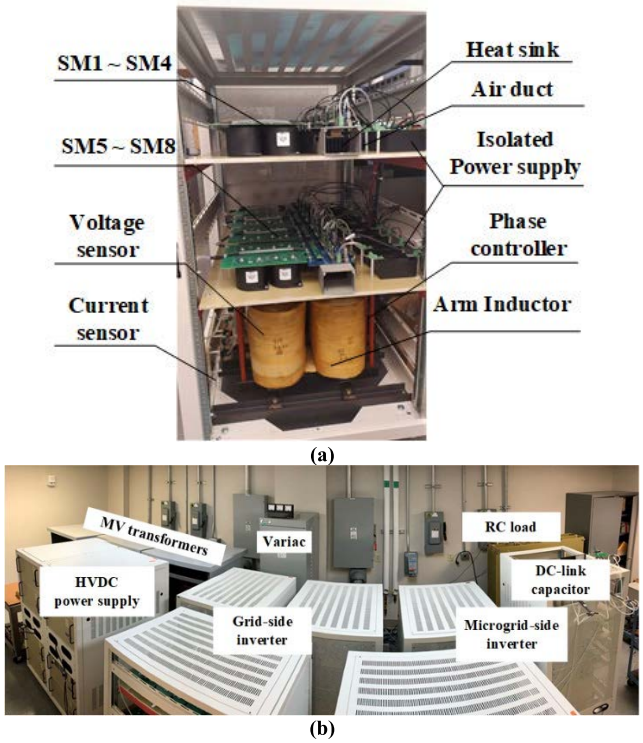

FIGURE 14. (a) One phase-leg hardware, (b) test setup of the back-to-back PCS.

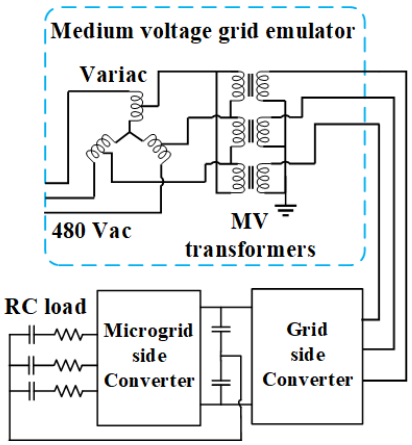

FIGURE 15. Back-to-back structured test circuit of the PCS converters.

phase-legs, and Figure 14(b) shows the back-to-back PCS test setup placed in a high voltage test lab.

Figure 15 shows the testing circuit scheme. Two ac/dc PCS converters form a back-to-back structure. One three-phase variac and three single-phase medium voltage transformers compose a medium voltage grid emulator to provide medium voltage ac power. A three-phase RC load (R = 250 Ω and C = 1.25uF) is used to simulate the load on the microgrid side.

The control is implemented in the $dq0$ coordinate system as shown in Figure 16. The grid side PCS controls the dc-link voltage and the microgrid side PCS regulates microgrid side ac voltage. V_{abc} and u_{abc} denote the microgrid side and the

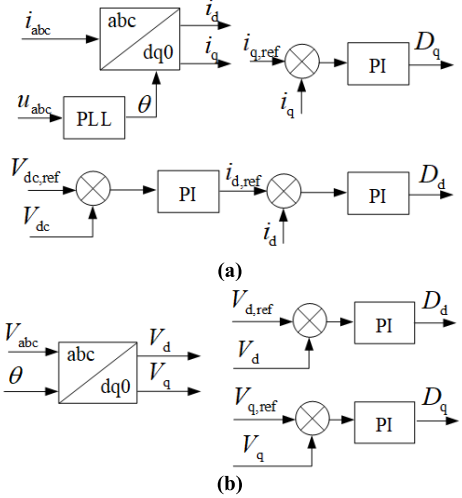

FIGURE 16. Control diagram of the back-to-back PCS converter system, (a) grid side converter and (b) microgrid side converter.

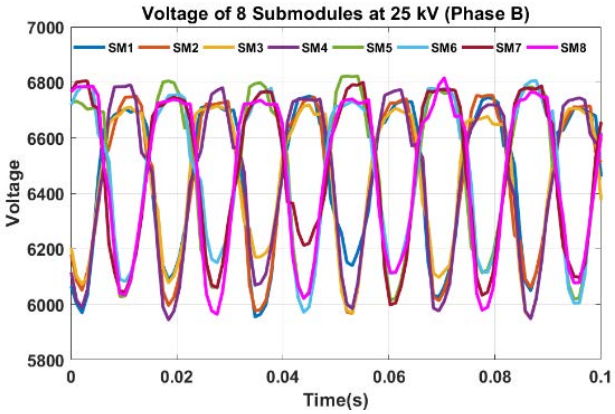

FIGURE 17. Submodule voltage balance control test results.

grid side three-phase voltages, respectively. V_d, V_q, I_d, and I_q are the voltages and currents in the $dq0$ coordinate system. D_d and D_q are duty cycles. θ is the phase angle for abc to $dq0$ coordinate transformation.

B. BACK-TO-BACK PCS TESTING

The developed back-to-back PCS is successfully tested at 25 kV dc-link voltage and microgrid side 13.8 kV ac rms line-to-line voltage and 100 kVA power rating.

Figure 17 shows the submodules voltage balancing control experimental results. The nominal submodule voltage is 6.25 kV. The maximum voltage difference between submodules is less than 250 V; and for each submodule, the voltage variation is within a range of 15% (below the 20% target).

Figure 18 shows the experimental waveforms of the back-to-back PCS at rated voltage and power.

Due to the high voltage low current operation condition of the PCS converter, the current waveforms look not very sinusoidal, especially the rectifier side ac current. The PCS and arm inductor are designed to limit the harmonics to be

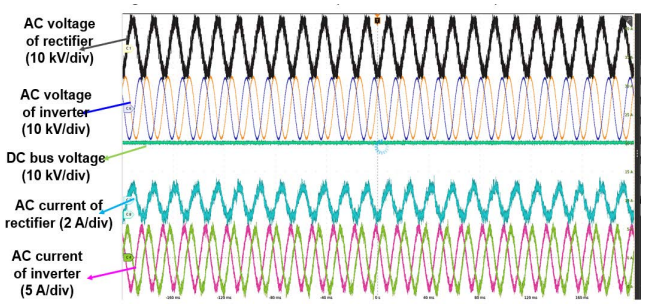

FIGURE 18. Test results of the back-to-back PCS at rated voltage and power.

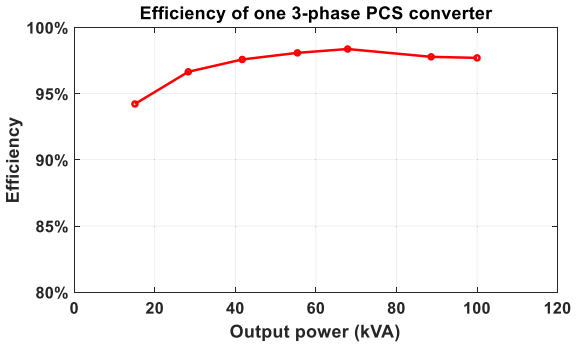

FIGURE 19. Efficiency curve of the PCS converter.

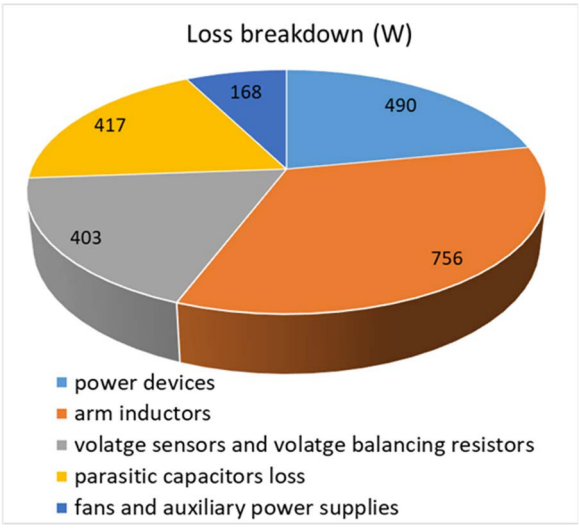

FIGURE 20. Loss breakdown of the PCS converter at rated voltage and full load.

less than 5% (THD<5%) at rated current. Following IEEE std 1159-2019, the harmonics components are considered only up to 50th order (3000Hz) as the higher order components are easy to be damped in the lines. The main harmonics in the current include both the low frequency components (i.e. the 3rd, 5th, 7th and 9th order components) and the switching frequency components (i.e. the 10 kHz and 20 kHz components). In the test, the inverter side ac current can meet the <5% THD requirement when calculated up to 50th order. If the switching frequency component related harmonics are included, the inverter side ac current THD is 10.7%. The rectifier side ac current looks less sinusoidal than the inverter side ac current because the rectifier side current is smaller than the inverter side current while the harmonics are similar. In the lab test, due to the power limit from the lab panel, RC load is connected to the inverter side to support the rated voltage and current operation of the inverter and the load mainly consumes reactive power. The rectifier only provides the active power of the RC load and also PCS loss. Thus, the rectifier current is smaller. As a result, the rectifier current harmonics percentage is higher and the waveforms look less sinusoidal.

The efficiency of the PCS converter is tested. Figure 19 shows the tested efficiency curve of one PCS converter at 25 kV dc bus voltage and various loads. The tested efficiency is 97.7% at full load condition.

At full load condition, the power loss breakdown is estimated and shown in Figure 20. In addition to the power devices loss, arm inductors loss, and fans and auxiliary power supplies loss, the voltage sensors and voltage balancing resistors loss and parasitic capacitance loss are also included. These two parts of loss are usually small and not considered in low voltage converters. However, for medium voltage converters, they actually occupy a large portion of the total power loss and cannot be neglected, especially for this PCS which has high voltage and low current.

The voltage sensors and voltage balancing resistors loss refer to the loss consumed by the resistors used in the voltage dividers of voltage sensors (PCS ac and dc sides voltage sensors, submodule voltage sensors) and resistors used for voltage balancing of series-connected capacitors (submodule capacitors and dc-link capacitors) and series-connected desat diodes (diodes in desat protection circuits). Although these resistors are in the megaohm range, the consumed loss is still high considering the high voltage.

The parasitic capacitance loss includes the arm inductor parasitic capacitances (turn to turn and turn to core parasitic capacitances) and other voltage pulsating (dv/dt) terminals to ground parasitic capacitances introduced loss. As PWM voltages are applied to these parasitic capacitances, they are charged/discharged during the switching transients, and the stored energies are consumed in the power devices, inductor windings, wires, and PCB traces in the charging/discharging loops.

The voltage sensors and voltage balancing resistors loss and parasitic capacitances loss are determined by the voltage level rather than the power level of the PCS converter. Thus, these two parts of loss almost keep unchanged, resulting in lower efficiency at light load conditions.

To further improve the efficiency of medium voltage PCS converters, it is critical to reduce the parasitic capacitances in the PCS setup, especially for dv/dt terminals. Increasing the resistances of voltage sensors and voltage balancing resistors

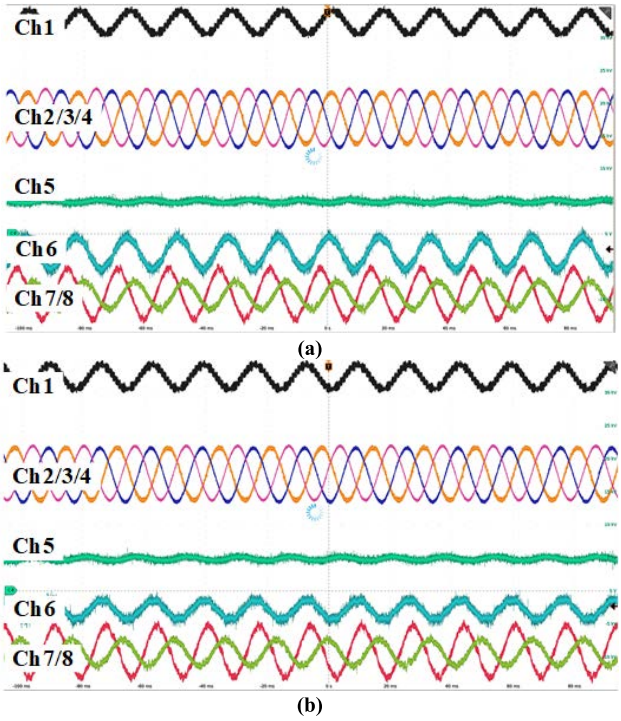

FIGURE 21. Microgrid side unbalanced load support operation test results: Ch1, grid voltage (10 kV/div); Ch2/3/4, microgrid voltage (5 kV/div); Ch5, dc link positive voltage (5 kV/div); Ch6, grid current (2 A/div); Ch7/8, microgrid current (5 A/div). (a) without zero-sequence and negative-sequence control; (b) with zero-sequence and negative-sequence control.

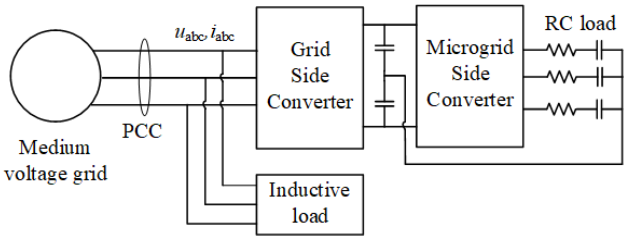

FIGURE 22. Reactive power compensation test circuit.

FIGURE 23. Reactive power compensation test results.

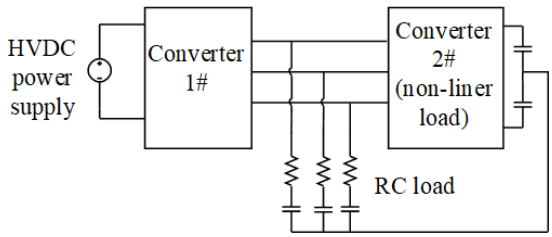

FIGURE 24. Active power filter test circuit.

can also be considered, but the voltage sensor noise immunity capability and voltage balancing performance of the voltage balancing resistors could be compromised. Note that the arm inductors loss is more than 30% of the PCS converter total loss at full load. The arm inductors are based on low cost but high loss silicon steel from commercial vendor, which can be further optimized for loss reduction.

C. PCS GRID SUPPORT FUNCTION TESTING

1) UNBALANCED LOAD SUPPORT FUNCTION TEST

Unbalanced load support is one of the essential features of the ASMG PCS. As mentioned, a three-phase RC load (R = 250 Ω and C = 1.25uF) is used in the experiments to simulate the load on the microgrid side. To test the unbalanced load operation, the microgrid side phase C load capacitance is modified to be 2.5 uF while Phase A and Phase B keeps 1.25 μF.

The zero-sequence and negative-sequence voltage control are added to guarantee the output voltage balance during the unbalanced load condition.

Figure 21 shows the test results of the unbalanced load operation at 10 kV dc-link voltage. Ch5 shows that the dc-link positive voltage contains significant voltage ripples caused by the unbalanced loads. Compared with the experimental results of the microgrid side voltage of channel 2/3/4, the zero-sequence and negative-sequence control can suppress the output voltage unbalance from 5% to 2%.

2) REACTIVE POWER COMPENSATION FUNCTION TEST

Reactive power support is one of the advantages of PCS. Figure 22 shows the test circuit diagram of reactive power compensation. After compensation, the power factor at the grid interface is close to unity, as shown in Figure 23.

3) ACTIVE POWER FILTER FUNCTION TEST

Excessive current harmonics is one major power quality problem in the grid. The high control bandwidth of the SiC based PCS enables active power filtering (APF) and can be used to suppress grid harmonics.

Figure 24 shows the test circuit diagram of the active power filter. Converter 2 emulates a nonlinear load with its output current including both fundamental and harmonic currents. Converter 1 represents the microgrid side PCS converter. In addition to support the system fundamental voltage, the APF function of Converter 1 is realized by controlling the harmonic voltage. In this case, the harmonic currents to the load will be suppressed.

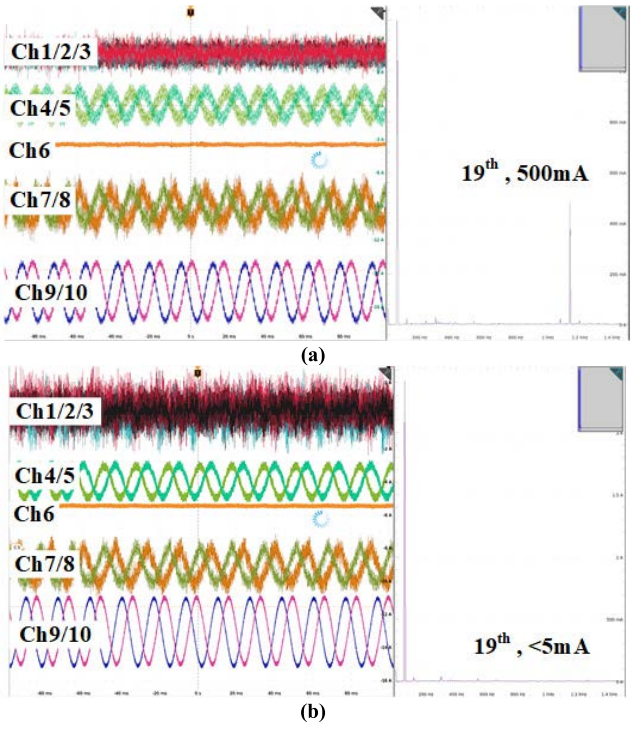

FIGURE 25. Active power filter experimental results: Ch1/2/3, rectifier mode converter output current (5 A/div); Ch4/5, RC load current (5 A/div); Ch6, rectifier mode converter dc link voltage (10 kV/div); Ch7/8, inverter mode converter output current (5 A/div); Ch9/10, grid voltage (10 kV/div). (a) without harmonic filter; (b) with harmonic filter.

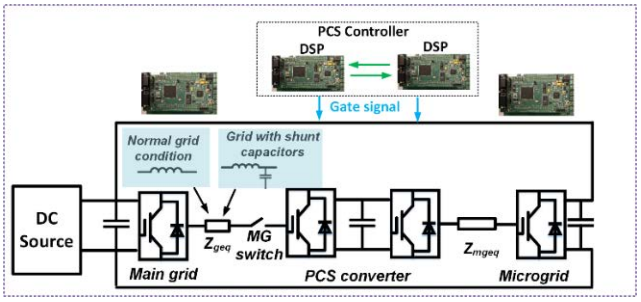

FIGURE 26. ASMG HTB testing setup.

In the test, the harmonic source injects 19th order (1140 Hz) harmonic current to the grid. Figure 25(a) and 25(b) show the experimental results for Converter 1 without harmonic compensation and with harmonic compensation, respectively. The harmonics are effectively suppressed. FFT analysis results show that the grid harmonic voltage reduced from 15% to 1% after harmonic filtering.

4) FAULT RIDE THROUGH FUNCTION TEST AND GRID STABILITY FUNCTION TEST

It is difficult to demonstrate some system-level benefits of ASMG PCS with MV PCS prototype in the lab due to the complexity of the setup. In this case, the lower voltage converter-based hardware testbed (HTB) is applied to demonstrate the system-level benefits of the PCS in an ASMG [32].

TABLE 2. Electrical parameters of the HTB.

Parameters	Values
Dc-link voltage (V_{dc})	200 V
Ac phase voltage (V_{ac})	81 V
Current base (I_b)	15 A
Fundamental frequency (f)	60 Hz
Converter filter impedance	L=0.575 mH, R=0.25 Ω
Dc-link capacitor (C_{dc})	5400 uF
Control frequency (f_c)	10 kHz
Digital control delay (T_d)	150 us (10 kHz)
Grid side shunt capacitor (C_g)	150 uF
Grid line impedance	L_g=0.575 mH, R_g=0.25 Ω

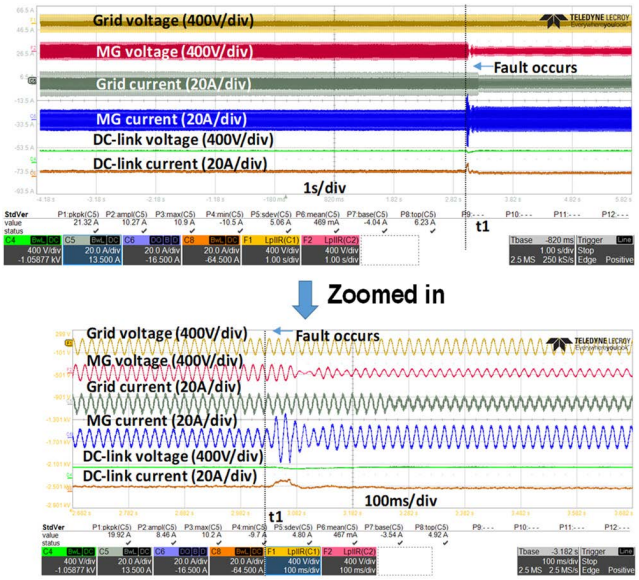

FIGURE 27. Testing results of PCS fault ride through in the grid-connected mode.

As shown in Figure 26, four low-voltage two-level voltage-source inverters are utilized to emulate an ASMG with PCS, where the PCS is emulated by two back-to-back connected inverters and the grid and microgrid are emulated by other two inverters, respectively.

Two testing cases are demonstrated on the HTB: fault ride through and grid stability improvement. The testing parameters are summarized in Table 2. In the fault ride through testing, an inductive distribution line is assumed. In the stability testing, a line with a shunt capacitor connection is emulated to evaluate the stability in a weak grid condition.

Two cases are applied to demonstrate the ASMG fault ride through. The first case is the fault ride through in the grid-connected mode as shown in Figure 27. When the fault occurs on the microgrid side, the microgrid side converter will detect the fault and ride through to limit the output current at t_1. Due to the decoupling of the PCS, the fault does not impact the grid voltage, indicating that the microgrid side fault is isolated by the PCS. The second case is in the islanded mode as shown in Figure 28. When the fault occurs on microgrid side, the microgrid emulator limits its current and the microgrid side converter can provide reactive power to support the microgrid.

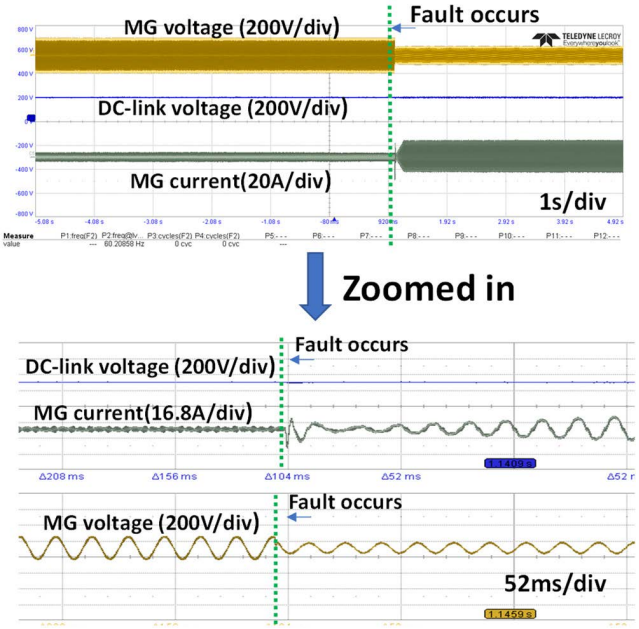

FIGURE 28. Testing results of PCS fault ride through in islanded mode.

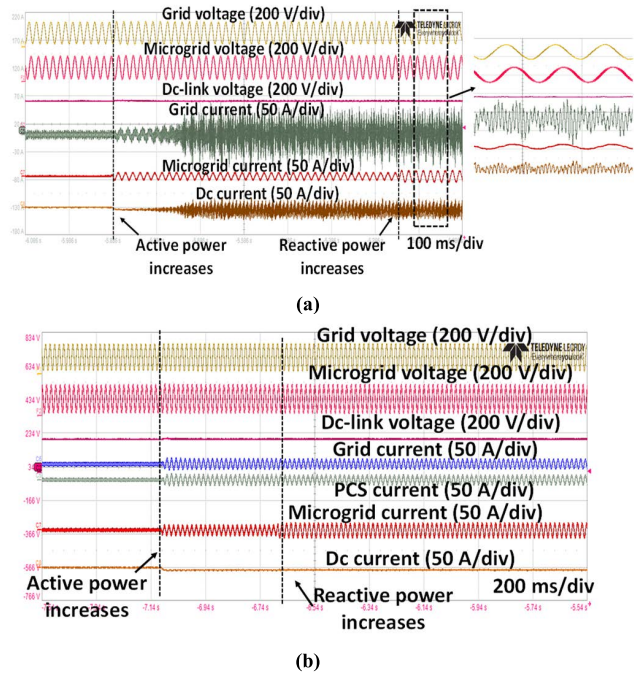

FIGURE 29. PCS grid stability enhancement testing: (b) 4 kHz control frequency; (b) 10 kHz control frequency.

The SiC-based PCS can further benefit grid stability with its high control frequency. The test results are shown in Figure 29. When the control frequency of the grid side PCS converter is 4 kHz, the grid current becomes unstable; when the control frequency is 10 kHz, no instability occurs.

V. CONCLUSION

This article presents a 10 kV SiC MOSFET five-level MMC based PCS for the 13.8 kV ASMG. The fast switching of the 10 kV SiC MOSFET results in high dv/dt and poses great challenges for noise immunity and insulation design of the MV PCS. The subsystem gate driving and protection, isolated power supply, voltage sensors, and modulation design addressing the high dv/dt issue are presented. The developed PCS is successfully tested at 25 kV dc 13.8 kV ac voltages and 100 kVA power, verifying the presented design. The higher control bandwidth offered by the 10 kV SiC MOSFET enables more grid support functions of the developed MV PCS. Grid support functions including unbalanced load support, var compensation, active harmonic filtering, fault ride through, and enhanced stability are also successfully demonstrated, validating the SiC based PCS system-level benefits for ASMG.

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REFERENCES

[1] C. Chen, J. Wang, and D. Ton, "Modernizing distribution system restoration to achieve grid resiliency against extreme weather events: An integrated solution," *Proc. IEEE*, vol. 105, no. 7, pp. 1267–1288, Jul. 2017.
[2] Z. Li, M. Shahidehpour, F. Aminifar, A. Alabdulwahab, and Y. Al-Turki, "Networked microgrids for enhancing the power system resilience," *Proc. IEEE*, vol. 105, no. 7, pp. 1289–1310, Jul. 2017.
[3] S. F. Zarei, H. Mokhtari, and F. Blaabjerg, "Fault detection and protection strategy for islanded inverter-based microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 472–484, Feb. 2021.
[4] S. Ganesan, U. Subramaniam, A. A. Ghodke, R. M. Elavarasan, K. Raju, and M. S. Bhaskar, "Investigation on sizing of voltage source for a battery energy storage system in microgrid with renewable energy sources," *IEEE Access*, vol. 8, pp. 188861–188874, 2020.
[5] D. Wu, F. Tang, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, "A control architecture to coordinate renewable energy sources and energy storage systems in islanded microgrids," *IEEE Trans. Smart Grid*, vol. 6, no. 3, pp. 1156–1166, May 2015.
[6] L. Che, X. Zhang, M. Shahidehpour, A. Alabdulwahab, and A. Abusorrah, "Optimal interconnection planning of community microgrids with renewable energy sources," *IEEE Trans. Smart Grid*, vol. 8, no. 3, pp. 1054–1063, May 2017.
[7] J. Zhao, X. Lyu, Y. Fu, X. Hu, and F. Li, "Coordinated microgrid frequency regulation based on DFIG variable coefficient using virtual inertia and primary frequency control," *IEEE Trans. Energy Convers.*, vol. 31, no. 3, pp. 833–845, Sep. 2016.
[8] J. Schiffer, T. Seel, J. Raisch, and T. Sezi, "Voltage stability and reactive power sharing in inverter-based microgrids with consensus-based distributed voltage control," *IEEE Trans. Control Syst. Technol.*, vol. 24, no. 1, pp. 96–109, Jan. 2016.
[9] Y. Li, L. Fu, K. Meng, Z. Y. Dong, K. Muttaqi, and W. Du, "Autonomous control strategy for microgrid operating modes smooth transition," *IEEE Access*, vol. 8, pp. 142159–142172, 2020.
[10] M. Ganjian-Aboukheili, M. Shahabi, Q. Shafiee, and J. M. Guerrero, "Seamless transition of microgrids operation from grid-connected to islanded mode," *IEEE Trans. Smart Grid*, vol. 11, no. 3, pp. 2106–2114, May 2020.
[11] A. Hooshyar and R. Iravani, "Microgrid protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1332–1353, Jul. 2017.
[12] A. Vukojevic and S. Lukic, "Microgrid protection and control schemes for seamless transition to island and grid synchronization," *IEEE Trans. Smart Grid*, vol. 11, no. 4, pp. 2845–2855, Jul. 2020.
[13] M. Barnes and P. Binduhewa, "Asynchronous interconnection of a microgrid," in *Proc. CIRED Seminar, SmartGrids Distrib.*, 2008, pp. 64–68.

[14] R. Salcedo, A. Bokhari, M. Diaz-Aguilo, N. Lin, T. Hong, F. de Leon, D. Czarkowski, S. Flank, A. McDonnell, and R. E. Uosef, "Benefits of a nonsynchronous microgrid on dense-load LV secondary networks," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1076–1084, Jun. 2016.

[15] T. Hong and F. de Leon, "Controlling non-synchronous microgrids for load balancing of radial distribution systems," *IEEE Trans. Smart Grid*, vol. 8, no. 6, pp. 2608–2616, Nov. 2017.

[16] S. Ji, X. Huang, L. Zhang, J. Palmer, W. Giewont, F. Wang, and L. M. Tolbert, "Medium voltage (13.8 kV) transformer-less grid-connected DC/AC converter design and demonstration using 10 kV SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 1953–1959.

[17] S. Parashar, A. Kumar, V. Jakka, S. Bhattacharya, and V. Veliadis, "Demonstration of new generation 10kV SiC MOSFET modules in medium voltage power converters," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 208–213.

[18] J. Guo, T. Fan, Q. Li, and X. Wen, "Coupling and digital control delays affected stability analysis of permanent magnet synchronous motor current loop control," in *Proc. IEEE Vehicle Power Propuls. Conf. (VPPC)*, Oct. 2019, pp. 1–5.

[19] S.-I. Hamasaki, K. Nakahara, and M. Tuji, "Harmonics compensation in high frequency range of active power filter with SiC-MOSFET inverter in digital control system," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata-ECCE Asia)*, May 2018, pp. 3237–3242.

[20] S. Parashar, A. Kumar, and S. Bhattacharya, "High power medium voltage converters enabled by high voltage SiC power devices," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata-ECCE Asia)*, May 2018, pp. 3993–4000.

[21] F. Wang and S. Ji, "Benefits of high-voltage SiC-based power electronics in medium-voltage power-distribution grids," *Chin. J. Electr. Eng.*, vol. 7, no. 1, pp. 1–26, Mar. 2021.

[22] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. Int. Power Electron. Conf. (ECCE ASIA)*, Jun. 2010, pp. 502–507.

[23] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. 8th Int. Conf. Power Electron. (ECCE Asia)*, May 2011, pp. 1425–1431.

[24] W. Zhao, X. Ruan, D. Yang, X. Chen, and L. Jia, "Neutral point voltage ripple suppression for a three-phase four-wire inverter with an independently controlled neutral module," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2608–2619, Apr. 2017.

[25] I. Vechiu, O. Curea, and H. Camblong, "Transient operation of a four-leg inverter for autonomous applications with unbalanced load," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 399–407, Feb. 2010.

[26] Y. Li, E. A. Jones, and F. Wang, "Circulating current suppressing control's impact on arm inductance selection for modular multilevel converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 182–188, Mar. 2017.

[27] Z. Xu, H. Xiao, and Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renew. Power Gener.*, vol. 10, no. 6, pp. 788–797, Jan. 2016.

[28] *IEEE Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems*, Standard 1676-2010, 2011.

[29] J. B. Casady, V. Pala, D. J. Lichtenwalner, E. V. Brunt, B. Hull, G. Wang, J. Richmond, S. T. Allen, D. Grider, and J. Palmour, "New generation 10 kV SiC power MOSFET and diodes for industrial applications," in *Proc. PCIM Eur.* Nuremberg, Germany, 2015, pp. 1–8.

[30] Y. Wang, C. Hu, R. Ding, L. Xu, C. Fu, and E. Yang, "A nearest level PWM method for the MMC in DC distribution grids," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9209–9218, Nov. 2018.

[31] S. Ji, L. Zhang, X. Huang, J. Palmer, F. Wang, and L. M. Tolbert, "A novel voltage balancing control with dv/dt reduction for 10-kV SiC MOSFET-based medium voltage modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12533–12543, Nov. 2020.

[32] Y. Ma, J. Wang, F. Wang, and L. M. Tolbert, "Converter-based reconfigurable real-time electrical system emulation platform," *Chin. J. Electr. Eng.*, vol. 4, no. 1, pp. 20–27, 2018.

[33] *Standard for Medium Voltage Power Conversion Equipment*, document UL 347A, 2015.

[34] *Generic Standard on Printed Board Design*, document IPC-2221B, 2012.

[35] *Standard for Safety of Information Technology Equipment—Part 1: General Requirements*, document UL 60950-1, 2007.

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