A 6.6-kW High-Frequency Wireless Power Transfer System for Electric Vehicle Charging Using Multilayer Nonuniform Self-Resonant Coil at MHz

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***Abstract*—A high-power, high-frequency wireless power transfer system for electric vehicles (EVs) is proposed in this article with lightweight and compact coil design. Leveraging a multilayer nonuniform self-resonant coil, no external capacitor is needed for compensation and the high-frequency conduction loss is mitigated by sharing current between multiple copper layers. The analytical model for the proposed coil is provided, and prototype coils with 200-mm radius are fabricated and tested, achieving a quality factor over 450 at 3 MHz. The optimized design for both coils and a GaN-based power stage are detailed and validated experimentally. Experimental tests show 95.2% dc–dc efficiency with 6.6-kW power transferred across a 100-mm coil-to-coil distance with 52.5 kW/m^2 power density. The system demonstrates the first 6.6-kW wireless power transfer system for EV charging using compact self-resonant coils at MHz.**

***Index Terms*—Electric vehicle (EV) charging, multilayer spiral coil, self-resonant coil, wireless power transfer.**

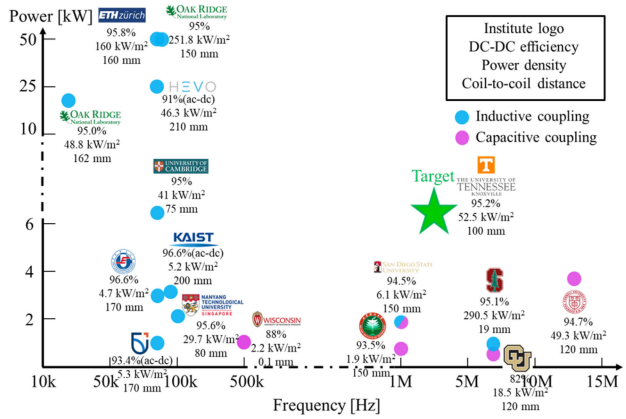

Fig. 1. State-of-the-art WPT systems for EV charging.

I. Introduction

With the increasing public awareness of the environmental impact of greenhouse gas emissions, electric vehicles (EVs) have drawn worldwide attention as the potential successor to gasoline vehicles. In contrast to conventional wired EV chargers, wireless power transfer (WPT) allows EV battery charging without a physical, cable connection in a safe, robust, and unobtrusive way. The wireless charging coils are buried underground, allowing the charging station footprint to be reduced. In addition, charging plugs, which can be easily damaged or cause electric safety concern without supervision, are no longer required [1].

Based on the different coupling mechanism between transmitter side and receiver side of the WPT system, there are two types of WPT techniques as candidates for high-power wireless EV applications: Inductive power transfer (IPT) and capacitive power transfer (CPT) [2]–[5]. Fig. 1 summarizes the state-of-the-art WPT systems for EV charger applications, with the power ranging from several hundred watts to kilowatts and the switching frequency ranging from tens of kilohertz to several megahertz. The color of dot represents the WPT technique applied. Critical performance specifications are also labeled, including system dc–dc efficiency, coil power density, and power transfer distance. IPT systems have been demonstrated with power rating up to tens of kilowatts, but most use frequencies below 100 kHz [6]–[15], many of which use 85 kHz following SAE J2954. High-frequency WPT system design at frequencies above 1 MHz has also been investigated. For instance, Gu *et al.* [16] use a parallel self-resonant (SR) coil structure at 6.78 MHz and reach an even higher power density at 291 kW/m^2 for IPT, but the power transfer is limited to 1 kW through only 19-mm air gap. This work investigates the feasibility of high-frequency, high-power WPT system design beyond the scope of the current literature. High-frequency operation does not inherently benefit the system, but enables the use of new SR passive components designs, which have the potential to reduce weight and volume of the system.

Since there is no high-frequency core loss and winding loss, CPT systems tend to work in higher frequency range in order to increase coupling between the metal plates [17], [18] but have limited power density and power rating. Work in [19] provides a

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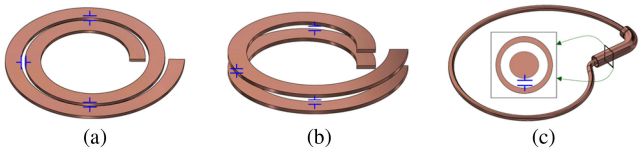

Fig. 2. SR coil classification based on the capacitance generation source. (a) Adjacent turns. (b) Parallel plates. (c) Coaxial capacitance on turns.

concept to integrate IPT and CPT systems, but power density is still not comparable to IPT systems. Compared with IPT, CPT does not require expensive high-frequency Litz wires or a magnetic core, which aids the high-frequency design to reduce the weight of passive components. However, CPT suffers from two major issues: low coupling capacitance and high fringing field. Capacitive coupling requires a relatively large coupling area to achieve large coupling capacitance, imposing a design challenge on high power density. For high-power EV applications with a large air gap, the transmission efficiency is low due to the low coupling [20]–[23]. By operating at 13.56 MHz, design in [24] further increases the power density of the capacitive link, but two large, specially designed toroidal interleaved-foil coupled inductors with 200-mm diameter are used to reduce the magnetic loss in the compensation network; the volume of these inductors is not included in the power density shown in Fig. 1. The high fringing field at the edge of coupled metal plate pairs is another concern for CPT because of electric field exposure limits on the human body [25], [26].

IPT is a relatively mature technology for WPT systems for EV chargers with air gap up to dozens of centimeters. However, the efficiency and power rating of IPT systems are often limited by low coupling between the transmitter coil and receiver coil due to the large air gap. This issue can be addressed by using more Litz wire windings or heavier magnetic cores and having larger coils up to 400–500 mm in radius to gain larger inductance value and higher coupling coefficient. However, the efficiency and power density are often sacrificed, and overall manufacturing cost is inevitably increased. Moreover, the compensation networks like capacitors take a significant percentage of system total loss [6]. Together with associated cooling components, the system volume is further increased. If the size of the compensation network is included, the calculated power density for low-frequency IPT systems in Fig. 1 will be reduced significantly.

Among many WPT coil structures, the SR coil has many advantages for MHz-range applications, including its compact structure and high-quality factor design. Based on the parasitic capacitance used for resonance, SR coils are classified into several types, including parasitic capacitance from adjacent turns [27], [28], from parallel-plate-shaped coils [29]–[32], and from other coaxial capacitors on the turn itself with complex structures [33]. The concept diagram based on different forms of capacitance generation is plotted in Fig. 2.

The coil in [27] uses an open bifilar coil consisting of two conductors wound in parallel. The coil of [28] has series-connected copper layers at both the top and bottom of a printed circuit board (PCB). The capacitance generated by adjacent turns is limited because the winding surface is not fully utilized for capacitance generation, which will inevitably increase the coil size. To reduce eddy current loss, coils made of thin foil copper are applied in [29]–[32] instead of round wire, and capacitance is formed between the overlapped copper plate areas with more efficient utilization of winding surface. The single-turn structure of [29] results in a low inductance value, which may result in large secondary-side current for a certain power rating. Three types of series-resonant SR coils using copper plate capacitance, with different number of layers, are presented in [30]–[32]. In [30] multiple layers are paralleled with good current sharing to reach over 800 quality factor, which is superior to the case in [31]. However, the designed inductance in [31] is much larger due to its multiturn spiral structure. Design in [32] is only considered for a complementary metal oxide semiconductor (CMOS) process for less than 1-W output. The capacitance in [33] is created by adding a hollow cylinder around the winding to form coaxial-like capacitor. The structure is complicated, and no power delivery is demonstrated. Of all the SR coils in [27]–[33], only the structure from [29] reaches 1-kW output in [16]. Still, the potential for higher power is limited by the single-turn inductance of less than 1 μH. Also, to avoid short and to drive the parallel resonant coils in [29], one series *L-C* filter and one choke inductor are required at the inverter side and rectifier side, respectively. Due to the limited achievable inductance and quality factor at MHz, there is no reported SR coil demonstration for high-power EV charging in the reviewed literature.

In this article, a high-power, high-frequency wireless EV charger is demonstrated utilizing the proposed multilayer nonuniform SR coil [34]. By pushing for higher frequency, smaller air-core coils with lower inductance values can be applied for the same power transfer. Litz wire is excessively expensive for strand diameters below 50 μm and may result in higher loss than solid-core copper with larger strand diameter for MHz frequencies. The multilayer SR coil structure used in this work allows high quality factor coils to be fabricated from layers of inexpensive copper foil and dielectric film. Additionally, the SR coil utilizes its interlayer capacitance for resonance, eliminating the external compensation capacitor and shrinking the overall volume of passive component to increase power density. A 6.6-kW prototype is built to validate the proposed coil structure, reaching 95.2% dc–dc efficiency at full power through 100-mm air gap. The power density is 52.5 kW/m^2 without any ferrite or external compensation components.

The rest of this article is organized as follows. Section II gives the multilayer nonuniform SR coil structural analysis. Section III presents the inductance and capacitance modeling process for the proposed coil, demonstrating its design process through geometry optimization. Section IV gives the system-level optimization, incorporating results of the optimized coil design. Section V presents the fabrication process and experimental measurements of a prototype system. Finally, Section VI concludes this article.

II. Proposed Multilayer Nonuniform Self-Resonant Coil Structure

Coil design plays a critical role for any high-efficiency, high-power density, low-cost, and robust WPT system. Based on the

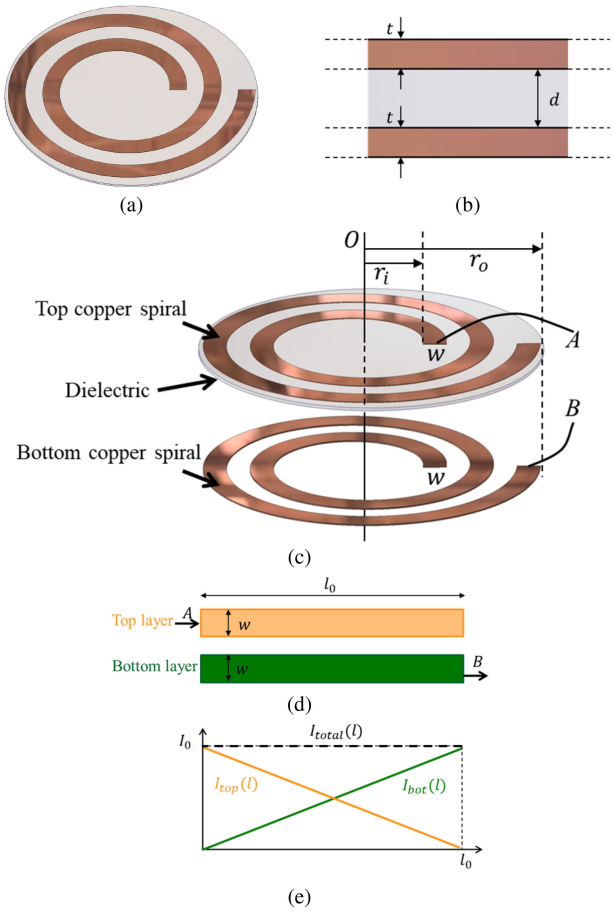

Fig. 3. Two-layer SR coil structure. (a) Three-dimensional view. (b) Side view. (c) Exploded 3-D view. (d) Top view of unfurled copper traces for top and bottom layers. (e) Current distribution along each copper trace.

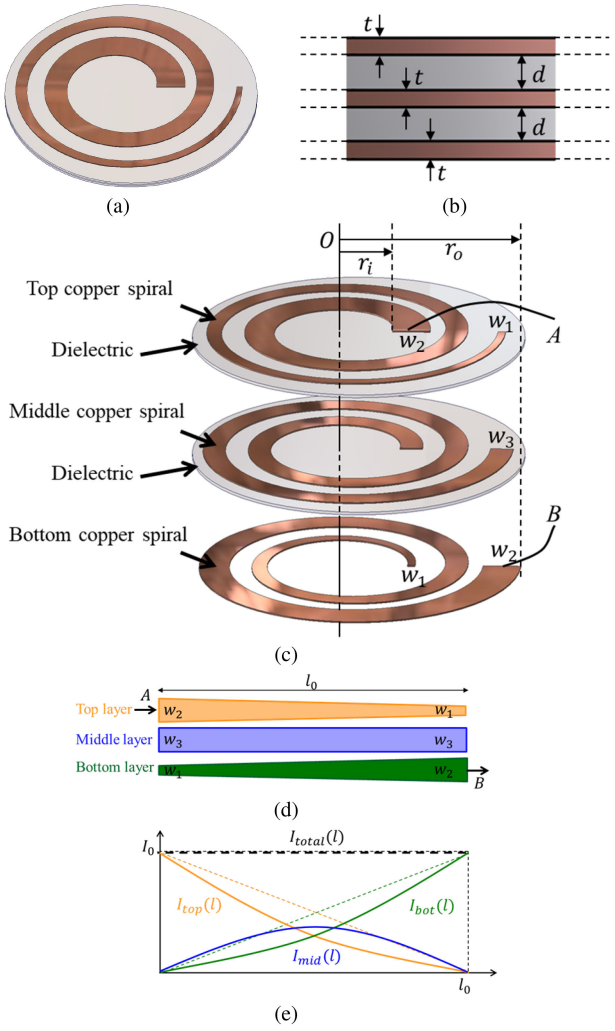

Fig. 4. Three-layer nonuniform SR coil structure. (a) Three-dimensional view. (b) Side view. (c) Exploded 3-D view. (d) Top view of unfurled copper traces for top, middle, and bottom layers. (e) Current distribution along each copper trace.

multiturn spiral SR coil structure in [31], a multilayer nonuniform SR coil with series resonance is proposed in this article, improving the quality factor by distributing the source current among multiple layers instead of the original two-layer design while maintaining a multiturn structure for large inductance. The proposed structure can be implemented with varying size and number of turns, making it applicable in WPT systems for consumer electronics and electric vehicles. Compared with the conventional SR coil designs, it has the advantages of high inductance and high quality factor, and exhibits a series *L*-*C* resonant characteristic. The coil structure and copper trace dimensions of the benchmark two-layer SR coil are shown in Fig. 3. The top layer and the bottom layer consist of two planar copper spirals with identical width, w, and trace length, l_0. The two spirals are separated by a dielectric material of thickness d. A parallel plate capacitor is formed between the overlapped areas of the copper traces on the top and bottom layers. The structure forms a series *L*-*C* resonant network between terminals *A* and *B*. When biased by an external ac source, current flows through the length of the spiral, gradually transferring between layers in the form of displacement current distributed over the length of the trace.

Due to the uniform copper trace width, the capacitance per unit length is constant over the length of the spiral. Thus, the current in the top spiral trace decreases linearly along its length as it transfers to the bottom spiral trace. Consequently, current on the bottom layer will be increasing at the same rate. At any point along the length of the spiral, the sum of the currents in two layers is equal to the source current I_0, as shown in Fig. 3(e).

As in a conventional spiral coil, the copper resistance can be reduced, thereby increasing the quality factor of the coil, by increasing the copper width w. However, for this two-layer coil structure, the trace width also determines the interlayer resonant capacitance, causing a reduction in resonant frequency as the trace width is increased. The maximum copper width is also limited by the coil diameter and number of turns needed to achieve a designed inductance value. Therefore, the achievable quality factor for a two-layer coil is inherently restricted by its SR structure.

To increase the copper area while maintaining a designed resonant frequency, a multilayer nonuniform SR coil is proposed. The structure of a three-layer case is shown in Fig. 4. Three layers of copper spiral traces are stacked vertically, with

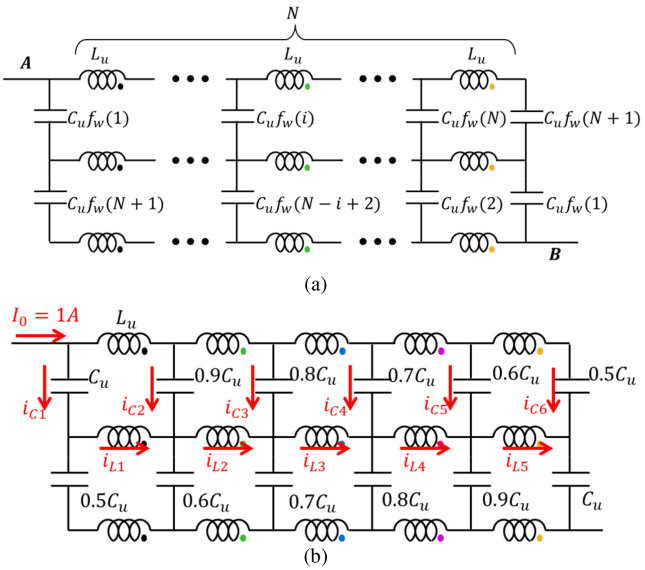

Fig. 5. (a) Generalized lumped element model for three-layer SR coil. (b) $N = 5$ segment lumped element model for three-layer nonuniform SR coil.

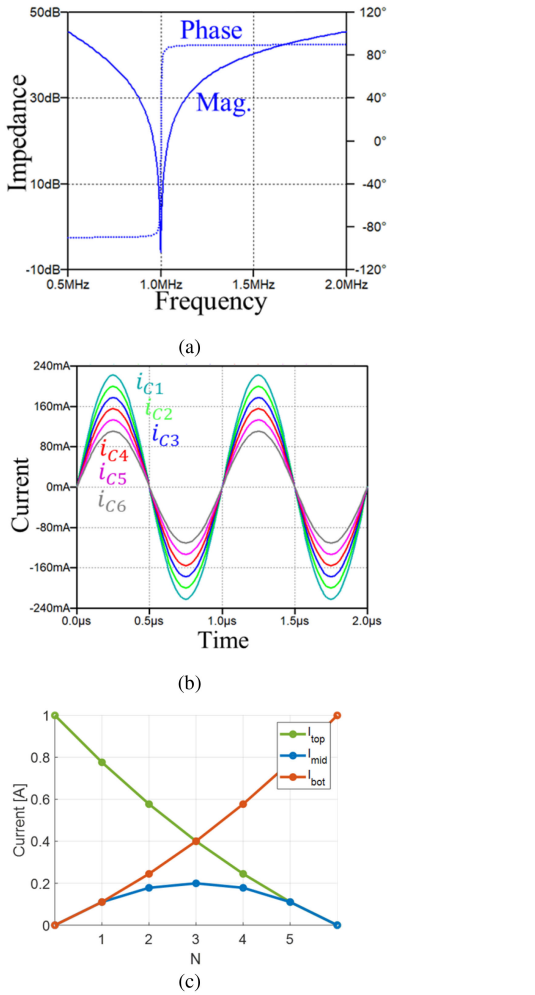

Fig. 6. LTspice simulation. (a) Impedance plot. (b) Current waveforms at distributed capacitors. (c) Current distribution in distributed inductors of three layers.

two equal-thickness layers of dielectric material sandwiched between. Different from the two-layer case, the current is transferred from terminal *A* on the top layer to the middle layer and eventually to the terminal *B* on the bottom layer in the form of displacement current. Equivalently, the current is gradually transferred through two dielectric layers in series. Detailed current flow and distribution are illustrated in the lumped element model simulation in Fig. 6. Together with the inductance from the spiral coils, the three-layer coil still works as a series *L*-*C* resonant network just like the two-layer coil.

The total current I_0 is now distributed over three layers of copper, allowing lower current density in the conductor and smaller equivalent coil resistance. To control the current density of each layer, the geometry of the traces is manipulated to have nonuniform width. As shown in Fig. 4(d), the width of the top layer is linearly decreased from w_2 to w_1, while on the bottom layer, width is linearly increased from w_1 to w_2. The width of middle layer is a constant, w_3. Due to the nonuniform copper width, the capacitance per unit length formed between adjacent copper layers varies along the trace length l_0. This variable capacitance is used to control the impedance, and thereby the current distribution between the three layers.

The current distribution achieved by the coil geometry of Fig. 4(d) is given in Fig. 4(e). The top layer current decreases exponentially along the spiral length, while the bottom layer current increases symmetrically. At any point in the spiral, the sum of the current in all three layers is constant. Varying the width profile of any trace will modify the current distribution. In the design of Fig. 4, the largest current among the three layers always flows in the copper trace with the widest width, resulting in reduced current density and conduction loss.

A generalized lumped element model is used to simulate and verify the relationship between the capacitance and current distribution in the three-layer SR coil. As shown in Fig. 5(a), each copper spiral layer is divided into *N* segments and modeled by *N* lumped inductors

$$L = NL_u. \tag{1}$$

A series of distributed capacitors are used to model the varying interlayer capacitance along the copper trace due to the varying copper width

$$C = \frac{C_u}{2} \sum_{i=1}^{N+1} f_w(i) \tag{2}$$

where C_u is the unit capacitance and f_w is the function to describe the variations in capacitance along the length of the spiral due to changing trace width. Higher values of *N* will yield more accurate models of the structure.

A simple example with $N = 5$ is shown in Fig. 5(b) and simulated behaviors are shown in Fig. 6(b) to demonstrate the coil operation. The example has $L = 20\ \mu$H and $C = 1.27$ nF for a 1-MHz resonant frequency.

$$f_w(i) = 1 - \frac{i-1}{2N}. \tag{3}$$

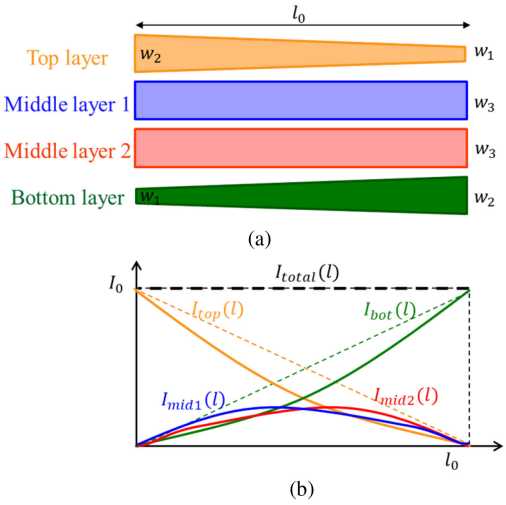

Fig. 7. Four-layer nonuniform SR coil structure. (a) Top view of unfurled copper traces for top, middle 1, middle 2, and bottom layers. (b) Current distribution along each copper trace.

The total impedance seen at the terminals is given in Fig. 6(a), verifying a series *L*-*C* characteristic behavior and resonance at 1 MHz as predicted. Fig. 6(b) shows the current in the lumped capacitors between the top and middle layer, and the current magnitude in each of the capacitors is exactly proportional to the capacitance value. Asymmetric capacitance between any two vertically connected capacitors results in a current sharing in three layers of distributed inductors, as shown in Fig. 6(c). The simulated current-sharing pattern matches the analysis in Fig. 4(e), and a quantitative current distribution for a coil design example will be provided after the coil-modeling process in Section III with the proposed coil *L*-*C* models. At any point in the model, the sum of currents in the three vertically aligned inductances is equal to I_0.

A special case occurs when all three layers have uniform copper width

$$f_w(i) = 1. \tag{4}$$

In this case, the currents in any two vertically connected capacitors in Fig. 5(a) are equal, leaving zero current in the middle copper layer. This case does not fully take advantage of the three-layer structure but is instead similar to the conventional two-layer case, with slightly modified fringing electric field distribution in the dielectrics. This case will be compared in detail in Section III with the nonuniform copper width case.

The coil geometry can be extended to have more than three layers. With more middle layers, it is possible for the total current to be shared in a more distributed way. As shown in Fig. 7 for a four-layer case, the current in the middle layer of Fig. 4 is now shared between two middle layers. Further increase in the number of layers with varying width will continue to improve current sharing, though with diminishing returns. The benefit of additional layers is physically bounded by the size of the coil. With more interlayer capacitors connected in series, the width of copper layer needs to be increased accordingly to maintain

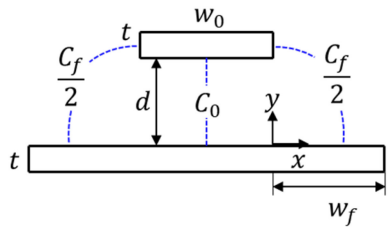

Fig. 8. Parallel plate capacitor with unequal width.

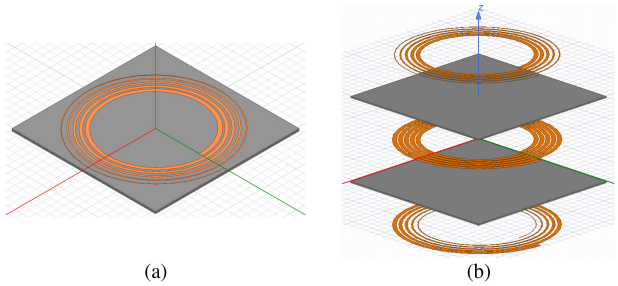

Fig. 9. (a) HFSS model for coil. (b) Exploded view of HFSS model.

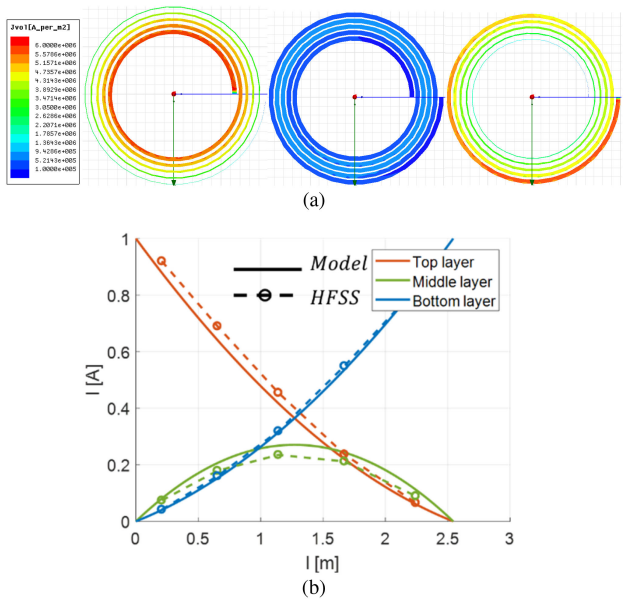

Fig. 10. (a) HFSS simulation for current density on three layers, top (left), middle (middle), and bottom (right). (b) Current distribution comparison based on model and HFSS simulation.

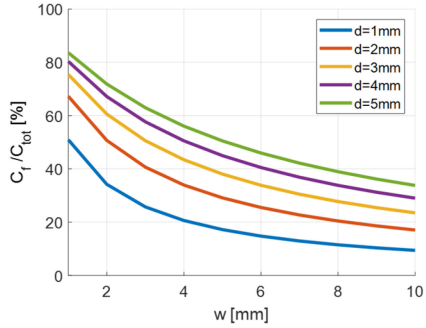

Fig. 11. Fringing capacitance to total capacitance ratio with different dielectric thickness for a parallel plate capacitor.

a same total equivalent capacitance of the coil. In addition, the increased proximity loss among layers will eventually outweigh the benefit of current sharing as the number of layer increases.

Considering all the factors above and manufacture limits, the coil cases with three-layer structure are studied in the following sections.

III. Multilayer Nonuniform Self-Resonant Coil Modeling and Design Optimization

A. Inductance Modeling

The inductance of a single-layer, multiturn spiral coil is given by [35]

$$L = \mu N^2 r_{\text{avg}} \left(\ln \frac{2.46}{r_{\text{diff}}} + 0.2 {r_{\text{diff}}}^2 \right) \tag{5}$$

where μ is the magnetic permeability and

$$r_{\text{avg}} = \frac{r_o + r_{\text{in}}}{2} \tag{6}$$

$$r_{\text{diff}} = \frac{r_o - r_{\text{in}}}{r_o + r_{\text{in}}} . \tag{7}$$

As was reported for the two-layer case, the inductance of the multilayer spiral coil is well-approximated by (2) as long as the coil thickness is much smaller than its copper width [31]. Because of the multilayer spiral structure, there is a vertical component to the current, but the vertical current flow is distributed over the entire surface area of the coil, whereas the circumferential current distributes only over the cross-sectional winding area. Therefore, the magnetic field resulting from the vertical component is relatively minor, and the component inductance is well-approximated by the field resulting from the circumferential flow, as modeled by (2).

B. Capacitance Modeling

In the three-layer structure, the capacitance is generated by the parallel plate structure between adjacent copper layers. With unequal copper width, both the overlap area and the fringing effect will contribute to the total capacitance value. The capacitance per unit length from overlapped area is

$$C_0 = \varepsilon_0 \, \varepsilon_r \frac{w_0}{d} \tag{8}$$

where ε_r is the relative dielectric permittivity, w_0 is the overlapped copper width between the two layers, and d is the dielectric thickness, as depicted in Fig. 8.

The fringing field capacitance per unit length is calculated using potential-theoretic method [36]. Based on Fourier series expansion, the electric field is

$$\phi(x, y) = \sum_{n=1}^{\infty} A_n \sin(k_n y) \, e^{-k_n x}. \tag{9}$$

A_n and k_n are constants determined by the boundary conditions for electric potential around the parallel plate. A symmetric boundary condition is assumed for simplification

$$f(\xi) = \begin{cases} F_1(\xi): \ -T \le \xi \le -d - t \\ -v_0: \ -d - t \le \xi \le -d \\ \frac{v_0}{d} \xi: \ -d \le \xi \le d \\ v_0: \ d \le \xi \le d + t \\ F_2(\xi): \ d + t \le \xi \le T \end{cases} \tag{10}$$

where $F_1(\xi)$ and $F_2(\xi)$ can be defined as either exponentially or linearly decreasing functions.

A linearly boundary condition is applied here

$$F_1(x) = -v_0 \frac{(T + x)}{(T - d - t)} \tag{11}$$

$$F_2(x) = v_0 \frac{(T - x)}{(T - d - t)}. \tag{12}$$

Under these boundary conditions, the Fourier series coefficients are

$$A_n = \frac{1}{T} \int_{-T}^{T} f(\xi) \sin(k_n \xi) \, d\xi \tag{13}$$

$$k_n = \frac{n\pi}{T} \tag{14}$$

and fringing field capacitance is

$$C_f = 2 \sum_{n=1}^{\infty} \varepsilon_0 \varepsilon_r \frac{A_n}{v_o} \left(1 - e^{-k_n (w_f + d)} \right) \tag{15}$$

where w_f is half of the width difference of two copper plates, t is the copper thickness, and v_o is the electric potential difference between two plates. Adding (5) and (12) together gives the total capacitance per unit length

$$C_{\text{tot}} = C_0 + C_f. \tag{16}$$

C. Three-Dimensional HFSS Simulation for Coil Current Distribution

A 3-D electromagnetic field simulation in HFSS is used to further validate the proposed structure and the *L-C* modeling result. Table I gives the coil parameters for the simulation.

TABLE I
Coil Geometry Details for HFSS Simulation

Inductance L [μH]	6
Capacitance C [pF]	92
Resonant frequency f_0 [MHz]	6.78
Outer radius r_o [mm]	100
Inner radius r_i [mm]	61.93
Copper thickness t [oz]	1
Total dielectric thickness $2d$ [mm]	3.048
Turns N	5
w_1 [mm]	0.1
w_2 [mm]	4.9
w_3 [mm]	4.9

Fig. 9 provides the simulation model in HFSS and Fig. 10(a) shows the current density of the three layers. Starting from the innermost turn on the top layer, the current is gradually transferred to the middle and bottom layers. The current density on the middle layer reaches its peak value at the spiral trace

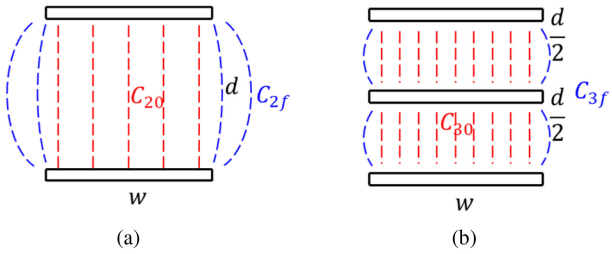

Fig. 12. Electric field of (a) two-layer capacitor and (b) three-layer capacitor.

midpoint, then drops to zero slowly, as expected from both analysis and lumped-element simulation. Fig. 10(b) gives a detailed comparison between the modeled and simulated current distribution. There is less than 10% error on average between modeled and simulated currents for all layers, which validates the coil *L-C* modeling results from Sections III-A and III-B. The error is mainly caused by the electric field modeling error in the capacitance model using potential-theoretic method. The limited mesh resolution in HFSS also contributes error in current distribution. The coil modeling results in this section will be further verified by the prototype coil characterization in Section V.

D. Effect of Fringing Capacitance in Three-Layer Coil Design

The three-layer SR coil gains additional benefit over a two-layer design due to the impact of the fringing capacitance. When the distance between copper layers is comparable to the copper width, the reduced fringing capacitance between copper layers that results from a higher number of layers facilitates a wider copper width compared with the two-layer case.

Fig. 11 shows the ratio of fringing capacitance C_f to the total capacitance $C_{\rm tot}$ for varying dielectric thickness d in a parallel plate capacitor of equal width. When the width of the plates w is small and the distance d between them is large, the fringing field dominates the overall capacitance.

To better understand the impact from fringing capacitance, Fig. 12 compares the electric fields of a segment of two-layer and three-layer coils. The total dielectric thickness d and width w are identical for both cases for a fair comparison. Neglecting fringing fields, the capacitance of both structures is the same.

$$C_{20} = C_{30}. \tag{17}$$

However, when fringing is considered, the three-layer structure exhibits a smaller capacitance due to the lower fringing field contributed by the smaller plate-to-plate distance.

$$C_{2f} > C_{3f} \tag{18}$$

$$C_2 = C_{20} + C_{2f} > C_3 = C_{30} + C_{3f}. \tag{19}$$

In other words, if both structures are designed for the same target capacitance, wider plates will be needed in the three-layer structure.

This effect is detailed in Fig. 13 by examining the numerical capacitances C_2 and C_3 from the two structures of Fig. 12 when total thickness d is 3 mm. The closer distance between parallel plates in the three-layer case gives better confinement of the

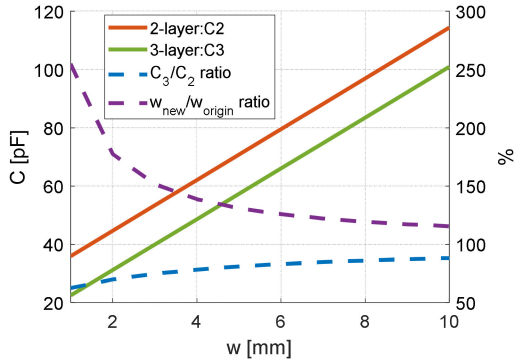

Fig. 13. Capacitance and copper width comparison of two-layer and three-layer coils.

fringing field, making the total capacitance C_3 smaller than C_2. Fig. 13 also shows the ratio of trace widths required in the three-layer and two-layer cases to achieve the same target capacitance. For example, when the copper width $w = 3$ mm, the copper width of the three-layer case needs to be increased by 52% such that $C_3 = C_2$. This increase results in further conduction loss reduction in addition to the current-sharing effect in the three-layer nonuniform SR coil. The analysis above is based on the modeling result in Sections III-A and III-B, and the benefit of the confined fringing field in a multilayer coil is further quantified by qualify factor comparison for optimized coil geometries at the end of the following section.

E. FEMM-Based Design Optimization for the Proposed Three-Layer Coil

Based on the *L-C* modeling, the design of both inductance and capacitance values are coupled by the geometry of the coil and the properties of the dielectric material. The coil inner radius r_i, outer radius r_o and number of turns N determine the inductance value and also constrain the available trace width which determines the total capacitance.

With a fixed coil size, there is a single coil geometry which will exhibit the highest quality factor for any achievable pair of inductance and capacitance values of the SR coil. Between these designs, selection of the optimal (L,C) pair requires consideration of the power stages and overall converter operation, which is addressed in Section IV. Initially, the coil design space is narrowed by considering only the optimal quality factor designs for any (L,C) pair.

To find coil designs with optimal quality factor, the coil resonant frequency f_0, inductance L, capacitance C, inner radius r_i, number of turns N, copper trace width w_1, w_2, and w_3, and dielectric material thickness d are swept to generate all feasible coil designs. The coil design flow chart in shown in Fig. 14. In the sweeping process, number of turns N is always preselected as the minimum number based on the inductance L requirement, since any larger N results in larger copper trace length and will unnecessarily increase the coil loss significantly. For each possible geometry combination, the coil total ESR R is calculated and compared to locate the optimal design with minimum R, or equivalently, the largest Q.

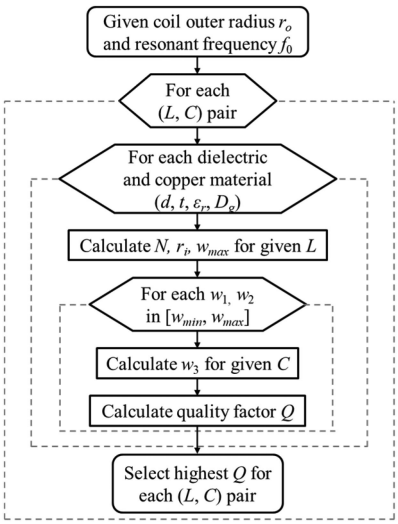

Fig. 14. Design flowchart for coil geometry.

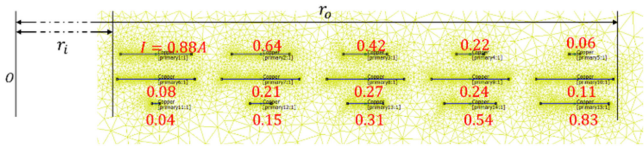

Fig. 15. Two-dimensional FEMM simulation setup example.

The dielectric ESR R_c is determined by the loss tangent D_g of the dielectric material

$$R_C = \frac{D_g}{2\pi f_0 C}. \tag{20}$$

Finite element method magnetics (FEMM) [37] is used to perform two-dimensional finite element analysis (FEA) for a fast simulation of copper loss to find R_{skin} and R_{prox}. Using the magnetostatic solver, the currents in each turn of every layer of the coil are assigned as individual sources. The coil is modeled as axisymmetric, and one setup example is shown in Fig. 15. Between the coil inner radius r_i and outer radius r_o, an $N = 5$ turns, three-layer coil is excited with discrete current values. From the innermost turn on the top copper layer, the current is decreasing continuously and transferred into the outermost turn on the bottom copper layer through the middle layer, as an approximate representation the real current distribution in the 3-D structure.

Note that the electric field between parallel copper plates cannot be simulated simultaneously with the magnetic field in FEMM. Accordingly, any current redistribution within the copper region caused by the electric field is neglected here. In Section V, the prototype coil experimental measurements prove that FEMM simulation provides a fast and accurate tool to demonstrate the benefit of the three-layer structure over the two-layer case. The resulting simulated quality factor Q, including the calculated dielectric loss of three-layer coil, is shown Fig. 16. For each inductance value along the x-axis, the coil geometry is optimized by the sweeping process in Fig. 14 for the highest quality factor Q at that inductance design point.

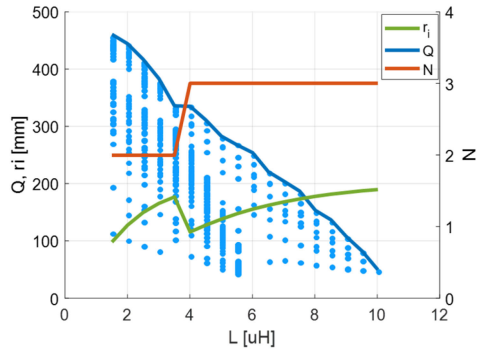

Fig. 16. Sweeping result of three-layer coil with $r_o = 200$ mm and $f_0 = 6.78$ MHz.

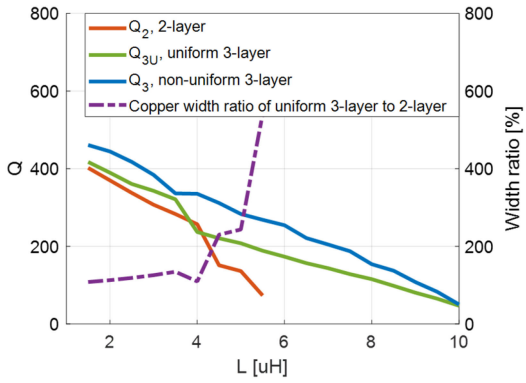

Fig. 17. Quality factor comparison for two-layer and three-layer coils with uniform copper width, and three-layer coil with nonuniform copper width coils. $r_o = 200$ mm and $f_0 = 6.78$ MHz.

The dielectric material properties align with the ROGERS Teflon laminates RO3003 [38], with relative dielectric constant $\varepsilon_r = 3$, maximum thickness $d = 1.52$ mm, loss tangent $D_g = 0.001$, and copper thickness $t = 1$ oz. The minimum inner radius r_i is fixed at one-third of the outer radius r_o. In this design example, the coil with outer radius $r_o = 200$ mm and resonant frequency $f_0 = 6.78$ MHz is selected to demonstrate the coil geometry optimization process. With the increasing inductance value along the x-axis, the inner radius needs to be increased when N is fixed. When $L = 4$ μH, the inner radius is close enough to the outer radius such that no design is available to fulfill the capacitance requirement. As a result, N is increased from 2 to 3, allowing r_i to drop and more space is available for copper traces between the inner and outer radius. When N jumps again to 4 at $L > 10$ μH, the total copper trace length is so large such that it needs very small copper width ($w \leq 0.1$ mm) to satisfy the capacitance value requirement, which leads to impractical fabrication requirements.

A design comparison between the two-layer and three-layer coil is given in Fig. 17. The maximum dielectric thickness for the two-layer case is 3.04 mm for a fair comparison with three-layer cases. A third case, of a three-layer coil with uniform copper width $w_1 = w_2 = w_3$, is also included. The uniform width case represents solely the advantage of diminished fringing electric field compared to the two-layer case as discussed previously. The trace width ratio between the two-layer and three-layer,

TABLE II
MULTILAYER COIL DESIGN CASE COMPARISON

	2-layer	3-layer uniform width	3-layer non-uniform width
Capacitance [pF]	100.2	100.2	100.2
w_1 [mm]	0.36	1.94	0.1
w_2 [mm]	0.36	1.94	4.38
w_3 [mm]	NA	1.94	2.47
Q	73.2	188.5	268.2
Q improvement		158%	42%

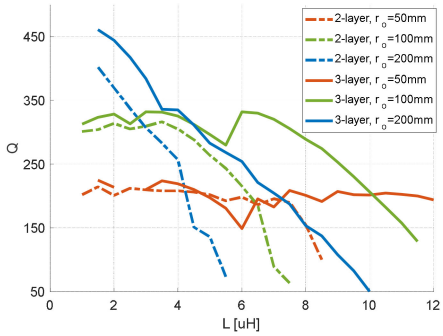

Fig. 18. Quality factor comparison for two-layer and three-layer coils with different coil radius, $f_0 = 6.78$ MHz.

uniform width, designs is shown by the dashed line. Clearly the fringing field effect partially accounts for the quality factor improvement in the three-layer nonuniform case in most of the sweeping range, especially with larger inductance value. Note that one exception occurs when $L = 4$ μH. Due to the fact that $N = 3$ for the uniform three-layer case and $N = 2$ for the 2-layer case at this point, the three-layer has much longer total copper trace length than the two-layer case, resulting in a comparable copper width and slightly lower quality factor.

A more detailed comparison of designs from Fig. 17 is provided in Table II to show the effect of copper width on generated capacitance from different coil structures. The targeted inductance is 5.5 μH and capacitance is 100.2 pF. For the two-layer case, the copper width is limited to a very small value due to the relatively high fringing electric field, leading to a quality factor less than 100. The three-layer with uniform copper width case reduces the fringing effect, and much wider copper width is allowed resulting 1.58 times higher quality factor. Combining the advantages from both better controlled fringing capacitance and current sharing among three layers, the nonuniform copper width case gives an additional 42% increase in quality factor over the uniform width case.

Fig. 18 gives the coil design results for the two-layer coil and the three-layer nonuniform coil with different outer radius. The quality factor is largely increased for the three-layer coil. At larger radius and inductance, the advantage is more significant. Note that for any coil structure, the largest, 200-mm radius is only advantageous in the range of smaller inductance, or equivalently larger capacitance. For example, for $L > 10$ μH, the three-layer coil has the highest Q for the smallest, 50-mm radius. When the desired capacitance is small at high inductance, the copper width of the 200-mm radius case is much smaller than

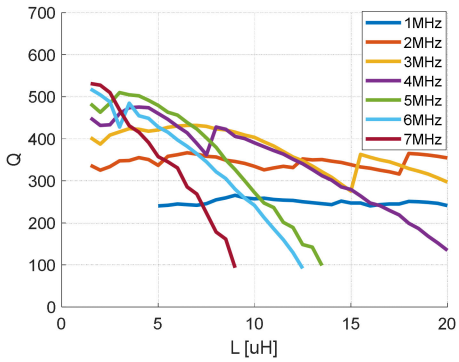

Fig. 19. Coil quality factor comparison with different frequencies $r_o = 200$ mm.

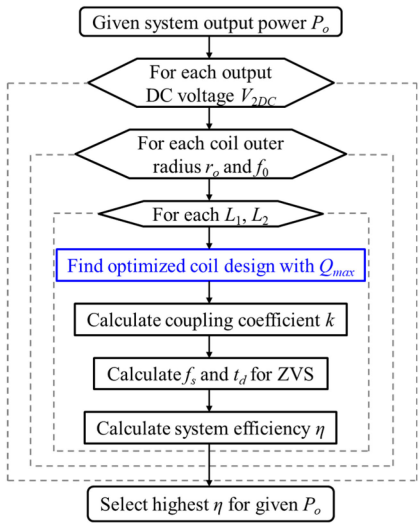

Fig. 20. Design flowchart for WPT system.

the 50-mm radius case due to the limited maximum dielectric thickness, leading to an insufficient utilization of coil pad surface area.

The complete three-layer coil design result is given in Fig. 19, with coil outer radius $r_o = 200$ mm and resonant frequency ranging from 1 to 7 MHz. This plot contains the optimal coil design for a range of coil inductances. The highest quality factor coils occur with very small inductance and high frequency. These designs do not necessarily guarantee the highest system efficiency; instead, the coil design in Fig. 19 is combined with a system-level design optimization, including power stages to determine the best overall system design in the next section, including the coil geometry and resonant frequency.

IV. WIRELESS CHARGING SYSTEM DESIGN PROCESS

A. System Design Flowchart

The integrated system design flowchart is shown in Fig. 20. For a given system power rating P_o and output voltage V_{2DC}, the system efficiency is calculated as both the transmitter and receiver coil designs are swept across all locally optimal designs from the previous section. Note that the coupling coefficient k between two coils is also a strong factor affecting the system

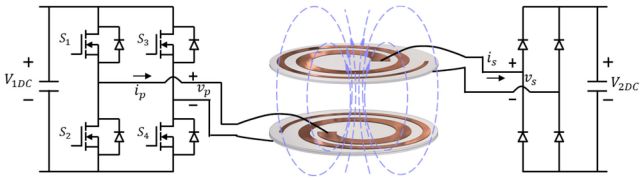

Fig. 21. Proposed WPT system diagram with two SR coils.

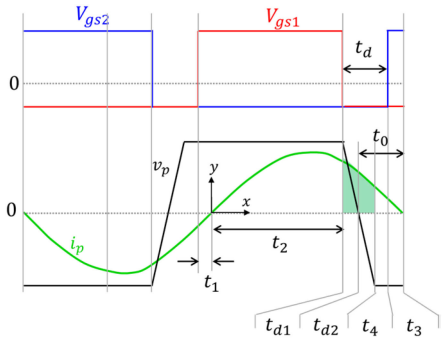

Fig. 22. Waveforms for inverter gate signals V_{gs1}, V_{gs2}, and inverter switching node voltage v_p and current i_p within one switching cycle.

operating point, which is determined by the coil geometries and distance between them. In Fig. 20, k is calculated each iteration for a fixed coil-to-coil distance. Switching frequency f_s is also tuned and maximum efficiency is calculated for each L_1 and L_2 pair.

In this section, the power stage loss models are based on GaN Systems GS66516T 650 V GaN transistors and CREE C4D08120E 1200 V SiC Schottky diodes implementing the high-frequency inverter and rectifier, respectively. In the system modeling process, coil waveforms are approximated by their fundamental frequency component. Junction capacitance of both GaN transistors and diode bridge are accurately modeled during the high-frequency transient, as discussed in [39], [40]. The system diagram is given in Fig. 21. The coils are designed with radius up to $r_o = 200$ mm and an air gap of 100 mm. Input and output voltages are allowed to vary, but constrained below voltage ratings of the selected GaNFET and diode.

For a 6.6-kW GaN inverter with MHz switching frequency, the zero-voltage switching (ZVS) condition should always be maintained within the wide load range to avoid any hard switching. As shown in Fig. 22, proper tuning of the switching frequency f_s around the coil resonant frequency f_0 gives an inductive load seen by the inverter and forms a positive phase shift t_0 between the zero-crossing of the inverter output voltage and current. The green shaded area is the total charge $2Q_{\rm oss}$ required during the dead-time to achieve full ZVS of one phase leg. For the completion of ZVS, time intervals t_{d1} and t_{d2} need to fulfill

$$Q_{\rm oss} = \int_{\frac{T_s}{2}-t_0-t_{d1}}^{\frac{T_s}{2}-t_0} \sqrt{2} I_p \sin(\omega_s t) dt \tag{21}$$

$$Q_{\rm oss} = \int_{\frac{T_s}{2}-t_0}^{\frac{T_s}{2}-t_0+t_{d2}} \sqrt{2} I_p \sin(\omega_s t) dt \tag{22}$$

where I_p is the root mean square (RMS) value of i_p, and the switching dead-time t_d is selected such that

$$t_{d1} + t_{d2} \le t_d \le t_{d1} + t_0. \tag{23}$$

The lower boundary of dead-time $t_{d1} + t_{d2}$ is determined by the total charge $2Q_{\rm oss}$, and the upper boundary $t_{d1} + t_0$ prevents any recharging of $C_{\rm oss}$ that may occur if the dead-time does not complete before the polarity of i_p reverses direction. In the system optimization process, t_d is selected as the average value of the two boundaries to avoid any accidental partial hard-switching due to the modeling error.

In the following section, converter losses are modeled in detail to facilitate system-level optimization.

B. System Loss Model

The conduction loss when the transistor is ON is

$$P_{\rm con+} = 4\frac{1}{T_s}\int_{-t_1}^{t_2} i_p^2 R_{\rm ds} dt = 4 f_s I_p^2 \left[t_2 - \frac{\sin(2\omega_s t_2)}{2\omega_s} + t_1 - \frac{\sin(2\omega_s t_1)}{2\omega_s} \right] R_{\rm ds}. \tag{24}$$

The reverse conduction time, t_4, should be minimized especially when applying a large negative OFF-state gate voltage. The reverse conduction loss is

$$P_{\rm rev} = 4\frac{1}{T_s}\int_{\frac{T_s}{2}-t_0+t_{d2}}^{\frac{T_s}{2}-t_0+t_{d2}+t_4} (v_{0\rm rev} + R_{\rm rev} i_p) i_p dt \tag{25}$$

$$P_{\rm rev} = 4\left[v_{0\rm rev}\left(-\frac{\sqrt{2}I_p}{2\pi}\right)\left[\cos(\omega_s(t_3+t_4)) - \cos(\omega_s t_3)\right] + f_s I_p^2 \left[t_4 - \frac{\sin(2\omega_s(t_3+t_4))}{2\omega_s} + \frac{\sin(2\omega_s t_3)}{2\omega_s} \right] R_{\rm rev} \right] \tag{26}$$

where $R_{\rm ds}$ is the conducting resistance during ON-time, $R_{\rm rev}$ is the reverse conduction resistance, and $v_{0\rm rev}$ is the forward voltage when reverse conducting. Adding (21) and (23) together gives the total conduction loss.

The residual turn-OFF loss with ZVS fulfilled is estimated by the difference between the hard switching energy $E_{\rm off}$ and the energy stored in $C_{\rm oss}$ from device datasheet [41]

$$P_{\rm off} = 4 f_s (E_{\rm off} - E_{\rm oss}) \tag{27}$$

where $C_{\rm oss}$ hysteresis loss $P_{\rm coss}$ is approximated based on the test data for GaN Systems GS66504B transistors from [42] and linearly scaled by the device C_{oss} ratio. The diode bridge conduction loss and coil conduction loss are

$$P_D = 4\left(v_0 I_{\rm davg} + I_{\rm drms}^2 R_d\right) = 4\left(v_0\frac{\sqrt{2}I_s}{\pi} + \frac{I_s^2}{2}R_d\right) \tag{28}$$

$$P_{\rm coil} = I_p^2 R_1 + I_s^2 R_2 \tag{29}$$

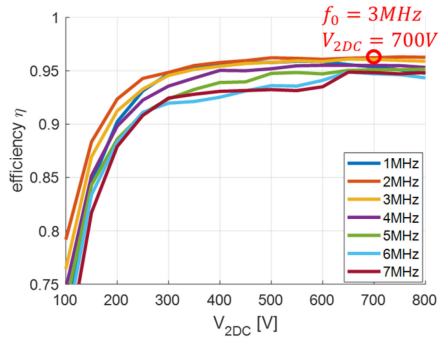

Fig. 23. Efficiency comparison with coil resonant frequency f_0 and load voltage V_{2DC}.

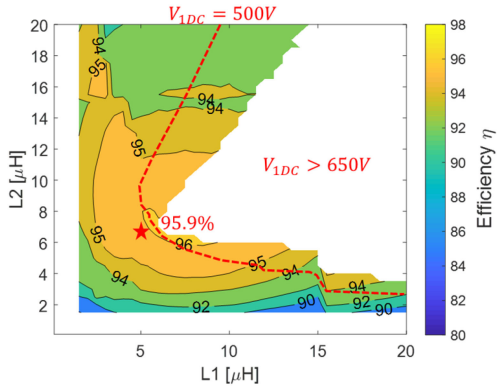

Fig. 24. System efficiency contour, $V_{2DC} = 700$ V, and $f_0 = 3$ MHz.

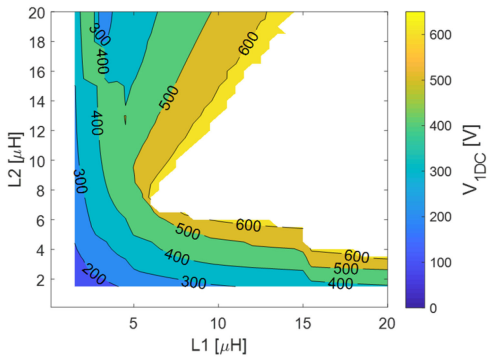

Fig. 25. System input voltage V_{1DC} contour, $V_{2DC} = 700$ V, and $f_0 = 3$ MHz.

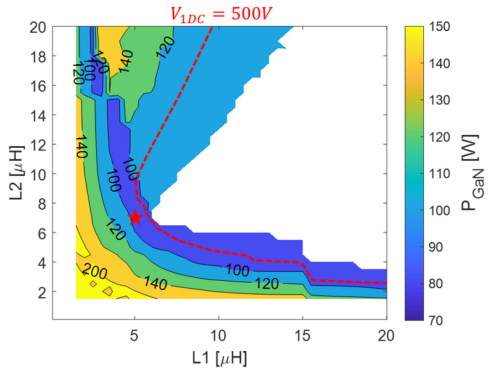

Fig. 26. GaN total loss contour, $V_{2DC} = 700$ V, and $f_0 = 3$ MHz.

where I_s is the RMS value of i_s, v_0 is the diode forward voltage. R_d is the diode resistance during conduction.

The final system efficiency is

$$\eta = \frac{P_o}{P_o + P_{\text{con+}} + P_{\text{rev}} + P_{\text{off}} + P_{\text{coss}} + P_D + P_{\text{coil}}}. \quad (30)$$

C. System Efficiency Contour and Analysis

After the optimizations both at the coil level and system level, the projected system efficiency is shown in Fig. 23 for different coil resonant frequencies. The target power rating is 6.6 kW and coil radius is 200 mm. The peak modeled efficiency point is achieved around $f_0 = 3$ MHz when $V_{2DC} = 700$ V. This design point is further expanded into the efficiency contours in Fig. 24, where the inductance values of primary side and secondary coil, L_1 and L_2 are used as variables. With different combinations of L_1 and L_2, the coil quality factor from Fig. 19 strongly impacts the system efficiency. The high quality factor and low inductance coil designs have degraded the system performance due to excessive peak currents on the primary side.

The right side of Fig. 24 contains a blank area where designs were eliminated due to exceeding the 650 V voltage-rating of GaN devices, which is also shown in the system input voltage contour in Fig. 25. Given a 150-V voltage margin, the highest efficiency design below the 500-V input voltage safety limit achieves 95.9% efficiency as marked. The coil inductances are $L_1 = 5$ μH and $L_2 = 6.5$ μH, with predicted quality factor of 421 and 432 and 3 MHz resonant frequency, respectively. The final system at full power operates at input voltage $V_{1DC} = 451$ V, output voltage $V_{2DC} = 700$ V, and a switching frequency $f_s = 3$ MHz based on the optimization result.

To evaluate the thermal stress on the high-frequency switching GaN devices, the total loss in the GaN devices is plotted in Fig. 26. Note that the total loss for four GaNFETs is close to 100 W, or 25 W per device, at the selected system design point. To mitigate the heating at such high power for the devices, a forced-air cooling solution with air duct and heatsink is designed and implemented, as illustrated in the following experimental verification section.

V. Three-Layer Coil Fabrication and System Experimental Result

With the system operating point determined, two three-layer nonuniform SR coils have been fabricated with RO3003 laminate, which exhibits good stability in dielectric constant over a large range of frequency and temperature variations [38]. The dielectric thickness is 1.524 mm with 5% manufacturing tolerance. The transmitter coil has inner radius $r_i = 79.5$ mm, $N = 4$ turns, and copper trace widths $w_1 = 14.0$ mm, $w_2 = 19.8$ mm, and $w_3 = 18.0$ mm. For the receiver coil, $r_i = 106.7$ mm, $N = 4$, $w_1 = 6.3$ mm, $w_2 = 17.0$ mm, and $w_3 = 13.6$ mm. A $t = 2$ oz, layer of copper cladding on the dielectric is used to form the spiral traces.

The coils are fabricated using laser cutting and chemical etching. Polyimide film tape from 3M is first used to cover the entire

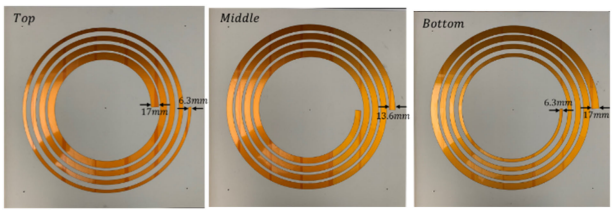

Fig. 27. Completed three copper layers for the receiver coil.

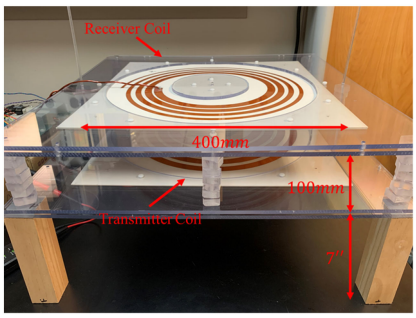

Fig. 28. Fabricated coils with mechanical setup.

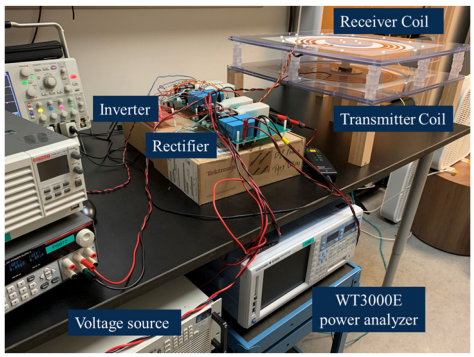

Fig. 29. System test setup with three-layer SR coils.

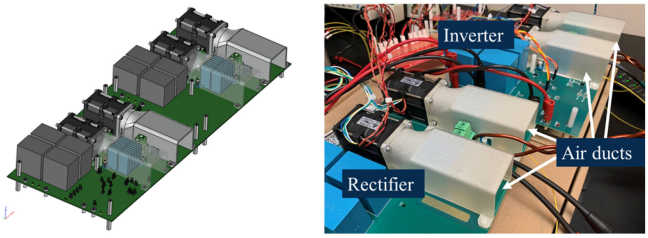

Fig. 30. Thermal management using heatsink with air duct on PCB boards. (a) Three-dimensional illustration. (b) Hardware setup.

TABLE III
SR COILS CHARACTERIZATION AND COMPARISON

	Model	HFSS simulation	Impedance analyzer
	Transmitter coil		
f_0 [MHz]	3	2.8	3
L [μH]	5	5.3	5.2
R [Ω]	0.224	0.220	0.235
Q	421	427	417
	Receiver coil		
f_0 [MHz]	3	2.8	3.21
L [μH]	6.5	6.8	6.7
R [Ω]	0.284	0.278	0.301
Q	432	435	452

TABLE IV
OPERATING POINT COMPARISON FOR MODELING AND TEST RESULT

	Model	Test
Input voltage V_{1DC} [V]	502	501
Transmitter current I_p [A]	17.9	18.6
Load voltage V_{2DC} [V]	727	732
Receiver current I_s [A]	11.9	11.6

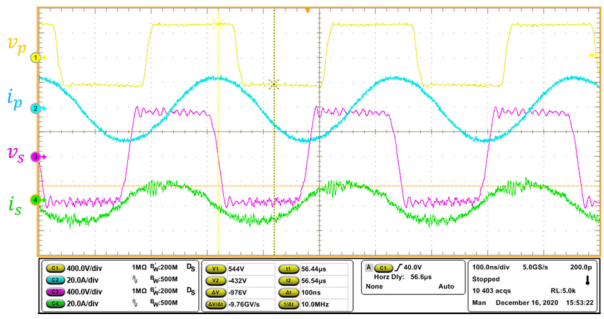

Fig. 31. Inverter output voltage v_p current i_p, and rectifier input voltage v_s current i_s at 6.6-kW output.

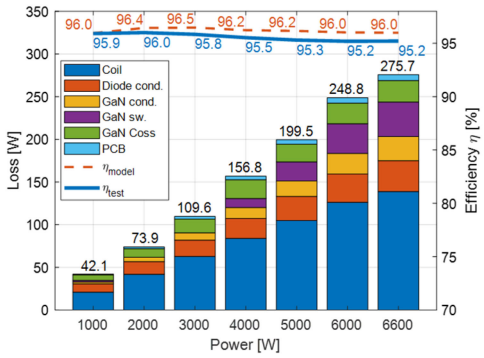

Fig. 32. System power loss breakdown for different power output.

copper cladding of the laminate. The tape is dimensionally stable at the high-temperature, flame-retardant, and chemical-resistant condition to prevent any damage on the outline of copper trace during the cutting or etching. Then, a very low-power computer numerical control (CNC) laser is used to selectively remove tape, leaving only the spiral coil area covered to protect the copper for acid etching. The three spiral patterns on top, middle, and bottom layers of a three-layer coil are center-aligned for an accurate resonant capacitance control. Ferric chloride solution serves as the etching liquid and continuous agitation is applied for faster rate of reaction. After the spirals are fully etched, the coil is cleaned with isopropyl alcohol and deionized hot water, and then baked for 1 h in a 150 °C heat chamber. The three layers of the finished receiver coil are shown in Fig. 27.

The applied dielectric laminate RO3003 is rated for 300 V/mil. To check for degradation due to chemical exposure, a Phenix 6CP30/15-3 AC dielectric test set is used for dielectric strength

TABLE V
WPT COIL DESIGN COMPARISON

Institute	Year	f [kHz]	DC-DC efficiency	Power [kW]	L [μH] pri./sec.	C [nF] pri./sec.	Relative air gap, $d/\sqrt{A}$	Compensation type	Gravimetric power density [kW/kg]†		Volumetric power density [kW/dm³]†	
									Coil	Coil + C	Coil	Coil + C
VT [43]	2018	100	95.9%	3.3	166/163	19.8/19.8	0.4	SS	1.8	1.7	6.6	6.1
ETH [44]	2016	85	96.5%	5	122/70.3	20.8/36.0	0.28	SS	6.4	2.2‡	--	5.0‡
ETH [6]	2016	85	95.8%	50	71.6/71.6	54.1/54.1	0.29	SS	4.7	2.0‡	--	2.7‡
ORNL [13]	2020	88.5	95.1%	50	31.7/31.6	90.7/90.7	0.34	3-phase SS	3.6§	3.3§	11.9	11.0
Stanford [16] & Dartmouth [29]	2021	6780	95.1%	1	0.17/0.16	3.3/3.4	0.32	Self-resonant	5.3		16.7	
UTK	2021	3125	95.2%	6.6	5/6.5	0.56/0.43	0.28	Self-resonant	**7.3***		**17.4***	

† Power densities are calculated separately for coil only (windings and ferrite) and coil with external compensation capacitors.
‡ Final assembly of coil pad with all passive components are included for weight and volume calculation in [44][6].
§ Wire guides are included in coil weight in [13].
* No ferrite is used in prototype

measurement. The fabricated and laminated sample passed the partial discharge test with less than 30 pC discharge at 4.4 kV RMS voltage, which is two times larger than the 1.7-kV RMS voltage on coil at full power, and therefore verifies the robustness of the laminates.

Fig. 28 shows the completed coils with mechanical support for testing. For each coil, the three-layer structure is held together with nylon screws. Quarter-inch thick polycarbonate sheets are applied for better clamping and half-inch polycarbonate bars are used to control the air gap between two coils. A 20-mm clearance is kept from all holes in the laminates and polycarbonate parts to any copper traces to fulfill the creepage requirement from UL60950 and to avoid additional dielectric loss from the polycarbonate.

Table III presents the comparison result between modeled, simulated, and measured coil parameters. The model is based on analysis supplemented with 2-D magnetostatic FEA using FEMM. The HFSS simulation uses 3-D electromagnetic FEA to verify the resonant behavior. The inductance, resistance, and resonant frequency of the two fabricated coils are measured by the curve-fitting function from the impedance analyzer directly. The fabricated coils have quality factor 417 and 452 on the primary and secondary, respectively, with less than 10% error from theoretical design point. Due to the impacts from both contact resistance and lead wires, the fabricated coils have slightly larger ESR compared to the modeling and HFSS simulation results.

The system experimental setup is shown in Fig. 29. The power stage and coils are connected via solid wires instead of stranded wires to minimize additional high-frequency ac loss. To effectively dissipate the heat from the semiconductor devices, a thermal management solution including heatsinks with forced-air cooling is used. The design uses FPX035035035 heatsinks from Advanced Thermal Solutions and HC5000 thermal interface material from Bergquist. To guarantee a laminar flow through the fins on the heatsink, a custom air duct is 3-D-printed using FLHTAM02 resin from Formlabs, with 238 °C heat deflection temperature. Fig. 30 gives the 3-D-printed air duct and final hardware assembly.

Operating waveforms at 6.6 kW output are given in Fig. 31, showcasing full ZVS for the GaN switches. With 80 Ω load resistance, 3.125-MHz switching frequency, and 35 ns dead-time, the system efficiency is 95.2%, measured with a Yokogawa WT3000E power analyzer. Table IV compares the operating point at full power for modeling and test result with less than 5% difference.

The loss breakdown is calculated based on the tested operating condition for different output powers and is shown in Fig. 32. The two coils take 50% of the total loss, including 88-W copper loss and 51-W dielectric loss. Note that at 6.6-kW power output, there is close to 100 W of loss in the GaN transistors, which accounts for 34% of the total loss. The maximum temperature of the GaN transistors at full power is well regulated at 83°C as measured by a sensing thermistor on the PCB board.

VI. CONCLUSION

This article investigates the design of a high-power, high-frequency WPT system for EV applications. By leveraging the structural characteristics of multilayer SR coil, high-inductance, high-quality factor coil design is possible with switching frequencies in the MHz range. Unlike low-frequency designs, this article requires no external compensation components. Together with the compact coil design at high frequency, the proposed structure has the highest gravimetric and volumetric power density compared with other state-of-the-art designs, as shown in Table V. The proposed air-core coil structure is of low cost and lightweight, with 200-mm radius, 3-mm thickness, and only 2-oz copper traces. Both coil and system have been optimized, and there is a good alignment between the theoretical modeling and test result. A 6.6-kW power test achieving 95.2% system efficiency through a 100-mm air gap validates the concept of high-frequency WPT system for EVs with a record-high power delivery using compact SR coils.

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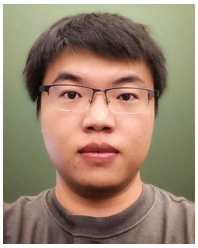

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