Letters

A Bulk-Capacitance Reduction Method Using Self-Driven Thyristor for AC–DC Converters

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***Abstract*—Universal serial bus power delivery fast chargers equipped with wide-bandgap devices are driven to higher power density and efficiency. The indispensable high-voltage bulk capacitors used to smooth the rectifier output could take 40% of the total system volume due to the large capacitance value required. This letter discussed a capacitor reduction method using a self-driven thyristor scheme comprised of only three components in total. No extra control circuit is needed. Circuit analysis and design equations are presented, and the design results are implemented in a 60-W GaN-based active-clamp flyback converter. The measurement results on the prototype show a 36.4% reduction of the bulk-capacitor size with similar efficiency compared to the conventional solution.**

***Index Terms*—AC-DC converter, capacitance reduction, high density, USB-PD.**

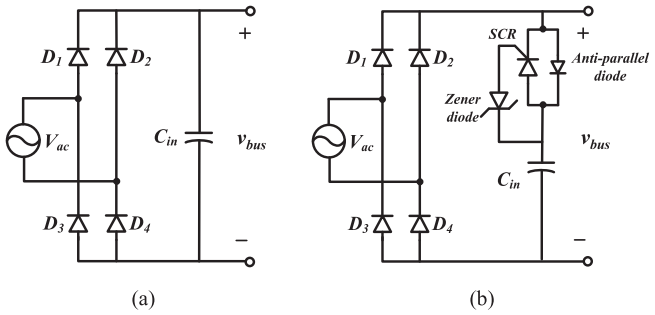

Fig. 1. (a) Conventional full-bridge rectifier circuit for ac–dc applications. (b) Improved rectifier with bulk-capacitance reduction method.

I. Introduction

LOW-POWER plug loads consume up to 46% of forecasted delivered electricity consumption in residential and commercial buildings [1]. Historically, those loads are powered by inefficient and relatively low-quality ac/dc adapters, creating significant end-of-life electronic wastes. Universal serial bus power delivery (USB-PD) unifies the charging standard up to 100 W [2] and is rapidly adopted for a broad category of loads. The market constantly drives the USB-PD solution for smaller size. Gallium nitride technology was adopted for this application by switching at a higher frequency, thus reduces the size of magnetic and output capacitors. However, the bulk electrolytic capacitor remains a challenge since they are line-frequency dependent. For one GaN-based high-frequency charger, the bulk capacitor takes nearly 40% of the total volume [3].

Most research efforts on bulk-capacitor reduction focus on high-power kilowatt applications and most proposed solutions require multiple switches, drivers, sensing and control circuitry, and even microprocessors [4], [5]. The incurred high complexity and cost prohibit their adoptions for the USB-PD ac–dc applications, especially for the cases of power level less than 75 W, where power factor correction is not needed. Research works for those cases are underexplored. A line-conduction extension method is discussed in [6] for a 60-W adapter, but it also requires complicated and costly implementation with additional switches, gate drive, and controls. Another line-conduction extension method using the valley-fill circuit [7], [8] suffers from the limitation of a fixed line-conduction angle that results in unconfigurable bus voltage ripple. In this letter, a self-driven circuit using only three components to automatically realize line-conduction extension and reduce the bulk capacitance is discussed. The operation principles, design analysis, and experimental verifications are presented in the following sections.

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II. Concept of Capacitance Reduction

The conventional full-bridge rectifier stage for ac–dc converters is shown in Fig. 1(a), and the voltage waveforms are shown in Fig. 2(a). When the ac line voltage rectified by the diode bridge is higher than the capacitor voltage, the capacitor is charged and the line voltage supplies the bus voltage; when the ac line voltage is lower than the capacitor voltage, the bulk capacitor is discharged to maintain the bus voltage variation within $V_{\mathrm{bus\_max}}$ and $V_{\mathrm{bus\_min}}$. This overall relationship is

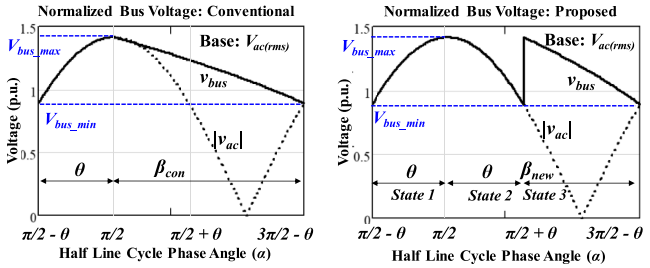


Fig. 2. Exemplary normalized bus voltage at $V_{\rm bus\_min}/V_{\rm bus\_max} = 0.63$ of (a) conventional full-bridge rectifier and (b) the proposed method.

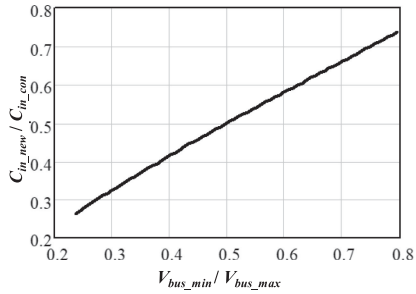


Fig. 3. Relationship between the ratio of capacitance reduction employing the proposed method and the bus voltage limitations calculated by (4).

given by

$$C_{\rm in}(\beta) = \frac{2P_o\beta}{2\pi f_{\rm line}(V^2{}_{\rm bus\_max} - V^2{}_{\rm bus\_min})} \tag{1}$$

where P_o is the output power of the rectifier, $f_{\rm line}$ is the 60-Hz line frequency, and β is the bulk capacitor discharge angle. In the conventional method, the capacitor discharge angle β is derived from the ac line supply angle θ by

$$\beta_{\rm con} = \pi - \theta = \pi - \cos^{-1}\left(\frac{V_{\rm bus\_min}}{V_{\rm bus\_max}}\right). \tag{2}$$

It can be seen from (1) that the capacitance needed is proportional to the angle $\beta_{\rm con}$ for a specific voltage ripple. Therefore, decreasing the capacitor discharging period (i.e., increasing the ac line supply period θ) results in smaller capacitance and improves the power density of the rectifier.

Based on this conclusion, an improved circuit implementation for the rectifier stage, as shown in Fig. 1(b), is discussed in this letter. Compared to the conventional rectifier, the improved solution employs a self-driven thyristor comprising only three low-voltage components [a silicon-controlled rectifier (SCR), a Zener diode, and an antiparallel diode] to extend the ac line supply angle from θ to 2θ, as shown in Fig. 2(b). Assuming the same designed bus voltage limitations $V_{\rm bus\_max}$ and $V_{\rm bus\_min}$, the bulk capacitor discharge angle now becomes

$$\beta_{\rm new} = \pi - 2\theta = \pi - 2\cos^{-1}\left(\frac{V_{\rm bus\_min}}{V_{\rm bus\_max}}\right). \tag{3}$$

Substitute (2) and (3) into (1), the ratio of the capacitance reduction from the proposed solution can be found from

$$\eta = \frac{C_{\rm in}(\beta_{\rm new})}{C_{\rm in}(\beta_{\rm con})} = 2 + \frac{\pi}{\cos^{-1}(V_{\rm bus\_min}/V_{\rm bus\_max}) - \pi}. \tag{4}$$

This capacitance ratio with respect to bus voltage peak-to-peak ratio is plotted in Fig. 3, which suggests more significant capacitance reduction can be achieved with a larger voltage variation between $V_{\rm bus\_max}$ and $V_{\rm bus\_min}$. As $V_{\rm bus\_max}$ equals the sinusoidal peak of input ac voltage (ignoring voltage drop on the diode bridge), and the lower voltage limit $V_{\rm bus\_min}$ should be designed to the absolute minimum in order to maximize the advantage of the capacitance reduction. However, it should be considered that a lower $V_{\rm bus\_min}$ from the rectifier may undermine the efficiency of the subsequent converter stage. Therefore, the value of $V_{\rm bus\_min}$ should be selected based on the tradeoff between capacitor size and overall efficiency for high-density ac–dc converter applications.

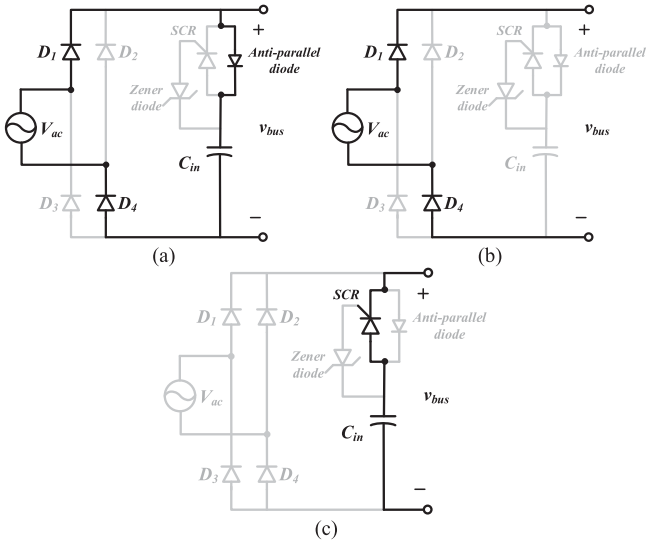


Fig. 4. Schematic illustration of the three operation states. (a) Capacitor charging. (b) Line-conduction extension. (c) Capacitor discharging.

III. Converter Analysis

The implementation of the proposed capacitance reduction method using all self-driven components is discussed in this section. As shown in Fig. 1(b), three extra components, including a SCR, a Zener diode, and an antiparallel diode, are added to the circuit to realize line-conduction extension. The three operation states are illustrated in Fig. 4.

State 1: Capacitor charging. The capacitor is charged during this state through the antiparallel diode until the capacitor voltage reaches maximum bus voltage $V_{\rm bus\_max}$. This state is the same as the charging state in the conventional full-bridge rectifier.

State 2: Line-conduction extension. As the ac line voltage drops below its maximum, both the Zener diode and the antiparallel diode are reverse biased, preserving the capacitor energy from releasing to the load and leaving the line voltage to supply for an extended conduction angle θ. As a result, the ac line voltage supply angle is doubled from θ to 2θ compared to the conventional solution.

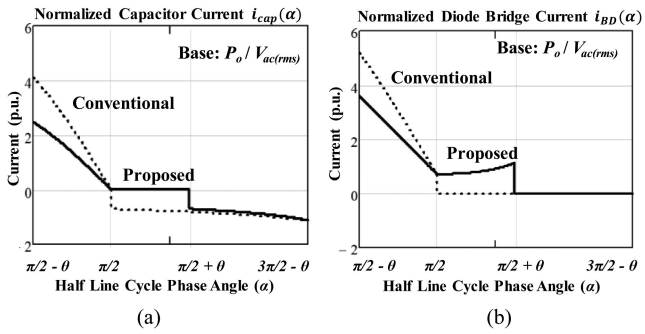
TABLE I
EQUATIONS FOR KEY VOLTAGES AND CURRENTS

Symbols	State 1: $\alpha \in \left(\frac{\pi}{2}-\theta, \frac{\pi}{2}\right)$	State 2: $\alpha \in \left(\frac{\pi}{2}, \frac{\pi}{2}+\theta\right)$	State 3: $\alpha \in \left(\frac{\pi}{2}+\theta, \frac{3\pi}{2}-\theta\right)$	Numbering
$v_{bus}(\alpha)$	$V_{bus\_max}\sin\alpha$	$V_{bus\_max}\sin\alpha$	$\sqrt{V_{bus\_max}^2 - \frac{P_o}{\pi f_{line} C_{in}}\left(\alpha - \frac{\pi}{2} - \theta\right)}$	(5)
$v_{cap}(\alpha)$	$V_{bus\_max}\sin\alpha$	V_{bus_max}	$\sqrt{V_{bus\_max}^2 - \frac{P_o}{\pi f_{line} C_{in}}\left(\alpha - \frac{\pi}{2} - \theta\right)}$	(6)
$i_{cap}(\alpha)$	$2\pi f_{line} C_{in} V_{bus\_max}\cos\alpha$	0	$-P_o \Big/ \sqrt{V_{bus\_max}^2 - \frac{P_o}{\pi f_{line} C_{in}}\left(\alpha - \frac{\pi}{2} - \theta\right)}$	(7)
$i_D(\alpha)$	$2\pi f_{line} C_{in} V_{bus\_max}\cos\alpha$	0	0	(8)
$i_{SCR}(\alpha)$	0	0	$-P_o \Big/ \sqrt{V_{bus\_max}^2 - \frac{P_o}{\pi f_{line} C_{in}}\left(\alpha - \frac{\pi}{2} - \theta\right)}$	(9)
$i_{BD}(\alpha)$	$2\pi f_{line} C_{in} V_{bus\_max}\cos\alpha + \frac{P_o}{V_{bus\_max}\sin\alpha}$	$\frac{P_o}{V_{bus\_max}\sin\alpha}$	0	(10)

State 3: Capacitor discharging. When the difference of the capacitor voltage and the ac line voltage reaches the reverse breakdown voltage of the Zener diode ($V_{\rm bus\_max} - V_{\rm bus\_min}$), the Zener diode's breakdown current turns ON the SCR, so the capacitor is reconnected into the circuit. As capacitor discharges, the Zener diode resumes reverse blocking and the SCR gate current deceases, but the SCR stays on due to its latching characteristic. The bulk capacitor supplies the load until the capacitor voltage drops to $V_{\rm bus\_min}$, where the ac line voltage regains control and the SCR turns OFF naturally with the forward voltage dropping below its minimum holding-current threshold. The ac line voltage forward biases the antiparallel diode and starts to recharge the capacitor, which completes one operation cycle. Note that this analysis assumes full-load condition; under light-load condition, the slower slew-rate of the capacitor discharge will slightly increase the duration of State 3 and shrink State 1. However, the load condition does not affect the operation and components rating of the proposed method as $V_{\rm bus\_min}$ remains constant.

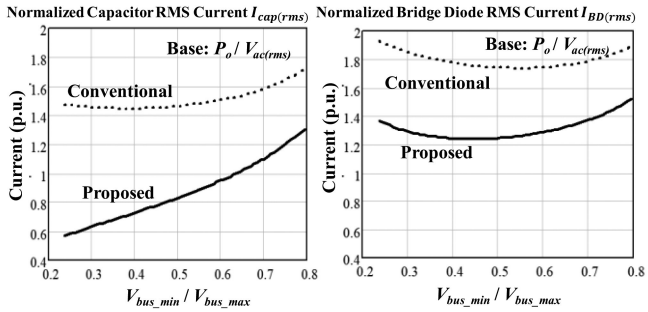
To summarize the operation principles, the SCR is turned ON by a threshold-setting Zener diode at ($V_{\rm bus\_max} - V_{\rm bus\_min}$) and is turned OFF naturally after ac line voltage takes over, realizing the capacitor's automatic connection. The line-conduction angle θ is configurable by the Zener diode's threshold voltage. Unlike employing active switches to control capacitor connections, the proposed method requires no additional sensing, control logics, or drivers to achieve this function, enabling a robust, high-density, and low-cost solution.

In order to evaluate the circuit performance of the proposed solution [see Fig 1(b)] compared to the conventional method [see Fig 1(a)], key voltages and currents that impact the components design and power loss of the proposed circuit are summarized in Table I. The bus voltage and the capacitor voltage supplying the load as a function of the instantaneous angle α in a half line cycle are given by (5) and (6), from which the blocking voltage for the SCR, the antiparallel diode, and the Zener diode can be derived and all equal to $V_{\rm bus\_max} - V_{\rm bus\_min}$. Practically, this blocking voltage should be designed in the range of tens of volts where a wide range of selection is available for high-performance and low-cost components.



(a) (b)

Fig. 5. Normalized (a) capacitor current and (b) diode bridge current at $V_{\rm bus\_min}/V_{\rm bus\_max} = 0.63$.



(a) (b)

Fig. 6. Normalized rms values of (a) capacitor current and (b) diode bridge current versus different $V_{\rm bus\_min}/V_{\rm bus\_max}$ ratios.

The equations of current for the capacitor $i_{\rm cap}$, the antiparallel diode i_D, the SCR $i_{\rm SCR}$, and the input diode bridge $i_{\rm BD}$ are provided in (7)–(10) for each state to evaluate the power loss performance of the proposed method. The current waveforms of $i_{\rm cap}$ and $i_{\rm BD}$ at $V_{\rm bus\_min}/V_{\rm bus\_max} = 0.63$ as an example are compared with the conventional method in Fig. 5, and they are normalized to the input current $P_o/V_{\rm ac}$ for generality. The rms values of the currents in Fig. 5 are calculated and plotted versus various voltage ratios $V_{\rm bus\_min}/V_{\rm bus\_max}$ in Fig. 6. It can be observed that the proposed method reduces the rms currents of both the capacitor and the diode bridge, which saves power

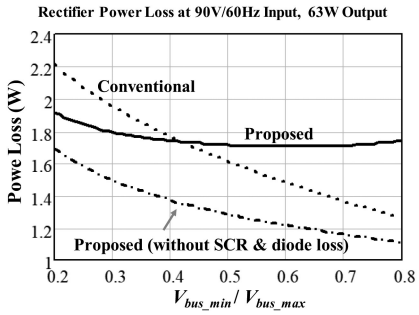


Fig. 7. Comparison of rectifier power loss on the prototype operating at 90-V/60-Hz input and $P_o = 63$-W output using the components in Table II.

TABLE II
RECTIFIER COMPONENT SELECTION

Components	Tested Circuits	
	Conventional	Proposed
Bulk Capacitor	ERK2GM220G16OT, 400V/88μF	400BXW56MEFC10X45, 400V/56μF
Bridge diode	Comchip Z4DGP406L-HF	Same
SCR	N/A	P0130AA, 100V/0.8A
Anti-parallel diode	N/A	NRVBAF360T3G, 60V/4A
Zener diode	N/A	DDZ9717S

Note: Design specifications: $V_{\mathrm{ac(rms)}} = 90$ V ($V_{\mathrm{bus\_max}} = 127$ V), $f_{\mathrm{line}} = 60$ Hz, $P_o = 63$ W (rectifier output power), $V_{\mathrm{bus\_min}} = 80$ V, and $V_{\mathrm{bus\_min}}/V_{\mathrm{bus\_max}} = 0.63$.

losses compared with conventional rectifiers. These power loss savings offset the additional conduction losses on the SCR and the antiparallel diode caused by i_{SCR} and i_D. Fig. 7 compares the calculated total rectifier power loss between the conventional and the proposed method on a prototype (see Table II) operating at 90-V/60-Hz input and 63-W output of the rectifier. The proposed method presents lower power loss than the conventional approach when the voltage ratio is below 0.42, but the power loss increases under higher voltage ratios due to conduction losses on the selected SCR and antiparallel diode. Note that the efficiency can be significantly improved over the entire range by using better SCR and diode components, as shown by the dash-dot line in Fig. 7. The assembled prototype and its corresponding experimental results are reported in the next section.

IV. EXPERIMENTAL VERIFICATION

The proposed rectifier solution [see Fig. 1(b)] was employed to optimize the conventional rectifier [see Fig. 1(a)] at the front end of a GaN-based active-clamp flyback (ACF) converter to achieve a higher power density for USB-PD charger applications. The bulk capacitors at the input side were replaced with smaller values, and the auxiliary SCR and diodes were soldered in series with the capacitors. The components used and the design specifications are listed in Table II, where the assembled prototype is shown in Fig. 8(a). Test results of the bus voltage and the input line current are shown in Fig. 9, which validates the operational theories. The ACF converter operates normally with the improved rectifier stage with an overall efficiency of 93.2%.

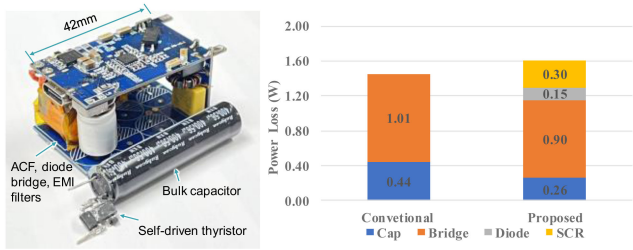


Fig. 8. (a) Prototype used to verify the proposed method for bulk capacitance reduction in the rectifier for a GaN-based ACF converter. (b) Rectifier loss breakdown comparison between conventional and proposed methods.

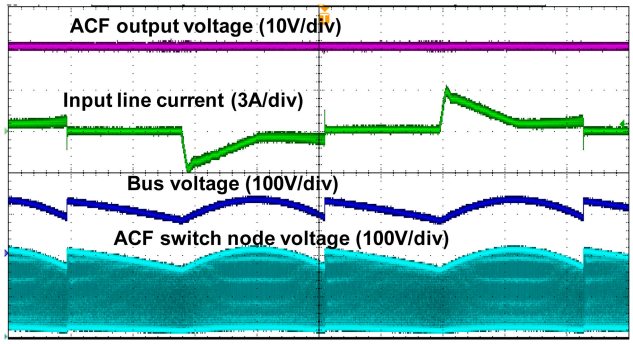


Fig. 9. Prototype test results showing the input line current, bus voltage, ACF switch node voltage, and output voltage.

As a result of the improved rectifier, the bulk capacitance is reduced from the original 88 to 56 μF, which realizes a capacitance reduction of 36.4% and a volume reduction of 29.7% compared to the conventional rectifier.

The power loss of the improved rectifier is measured and compared to the conventional solution. The loss breakdown between the two solutions is shown in Fig. 8(b). The losses on the capacitors and diode bridge are both lower using the improved method because of the lower rms currents (see Fig. 6). However, the total loss of the proposed method is 0.16 W higher due to the conduction losses on the SCR and diode inserted. It should be noted that the efficiency difference is negligible for a 60-W converter, but the total volume of the capacitors is reduced by 30% using this simple, low-cost, and self-driven solution. Using lower conduction-loss SCR will further improve the efficiency, and alternative self-driven devices to replace the SCR is being explored.

V. CONCLUSION

A bulk-capacitance reduction method was discussed for the rectifier stage used in ac–dc converters. This method uses a self-driven thyristor circuit comprising only three components to extend the ac line supply angle by two times, thereby realizing a lower requirement on the capacitance value needed for the same voltage ripple. Detailed design equations and loss analysis of the circuit were given. This method is verified in the rectifier used for a GaN-based ACF ac–dc converter, where the capacitor volume is reduced by 29.7% with nearly the same

efficiency as the conventional solution. This work provided a commercially viable solution for high power-density USB-PD charger design and can be extended to other ac–dc converter applications.

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