An Inrush Current Limiting Method for Grid-Connected Converters Considering Grid Voltage Disturbances

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***Abstract*— To support the electric power grid, some grid-connected converters are required to ride through abnormal grid conditions, including voltage disturbances. However, at the moment, when a grid voltage disturbance happens, a large inrush current could be induced due to the large difference between the grid and converter output pulsewidth modulation (PWM) voltages. This inrush current could be more severe in the faster switching SiC-based multilevel converter, which only needs a small filter inductance to meet its normal operation requirements, such as harmonics and peak ripple currents. In this article, a PWM mask method is used to limit the inrush current. With this method, the inrush current can be effectively limited to a preset value and can help the converter ride through grid voltage disturbances. The method is validated through experiments conducted on a single-phase SiC-based five-level converter considering low voltage, high voltage, and phase angle disturbances.**

***Index Terms*— Grid voltage disturbances, inrush current limiting, low-voltage ride through, SiC, voltage angle disturbance.**

I. Introduction

With the increasing penetration of wind, solar photovoltaic (PV), and energy storage, grid-connected power electronics converters are more widely used in the electric power system (EPS). To ensure the stability, resilience, and robustness of the EPS, these grid-connected converters need to ride through abnormal grid conditions, including grid voltage disturbances [1].

In the wind and solar PV applications, the voltage ride through (VRT) has been widely discussed, including the overvoltage issue in the dc link in wind converters [2], the overcurrent limitation in PV converters [3], topology characteristics during the low-voltage ride through (LVRT) [4], phase-locked loop (PLL) with fast and smooth transient response [5], and the control algorithm for grid support [6].

Grid voltage disturbances can also cause inrush current in a grid-connected converter. Assuming a voltage source converter (VSC) topology, when the grid voltage amplitude or angle suddenly changes, the converter output pulsewidth modulation (PWM) voltage cannot be immediately changed, due to the control delay and limited regulation bandwidth. Consequently, a large voltage difference can drop on the converter ac filter inductor, leading to a high inductor current rising/falling rate, and therefore, an inrush current occurs during the control delay period. A longer converter control delay and a smaller filter inductance will result in a larger inrush current. This phenomenon can be found in the simulation and experiment results of published works [7]–[10]. However, its impact on converters is rarely discussed either because it is not the focus of these papers or because the inrush current is not that large to be a concern because of the large filter inductance.

Due to the low switching loss of SiC devices, the switching frequency of SiC-based grid-connected converter can be increased to reduce the size of passives and achieve higher power density and lower cost if only considering the normal operation. Nevertheless, when considering the abnormal grid conditions, such as grid voltage disturbances, the design of passives will be affected. As will be explained later in this article, although the control delay decreases with the increased switching frequency, it is not linearly decreased due to fixed delays caused by filters in the loop (voltage sampling filter, PLL filter, and so on). With a smaller filter inductor, the inrush current could be significant in the SiC-based converters, which may exceed the semiconductor device capability without proper current limiting measures. Increasing the ac filter inductance can reduce the inrush current, but it increases the

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converter size and cost. Therefore, a control method that can limit the inrush current of the grid-connected converter during grid voltage disturbances can help to realize the benefits of SiC-based converters with high switching frequency.

To improve the dynamic response of grid-connected converters and avoid large overcurrent during the grid voltage disturbance, the grid voltage feedforward control is usually adopted. The main idea is to include the sampled grid voltage in PWM reference voltage and its corresponding duty cycle calculation. When the grid voltage changes, the converter output voltage can change correspondingly. Different realization approaches have been introduced in the literature, including grid voltage feedforward through a proportional coefficient and low-pass filter (LPF) [11], directly adding the grid voltage to PWM reference voltage and the duty cycle calculation [12], and using either the fundamental component of the grid voltage or the frequency limited grid voltage, which is used to reduce the sensitivity to grid disturbance and improve the converter stability [13]. However, the grid voltage feedforward control relies on the grid voltage sampling, which introduces sampling delay and some additional filter delays if used. Besides, the inherent converter control delay still exists in the grid voltage feedforward loop. Therefore, even with grid voltage feedforward control, the inevitable delays are larger than one control cycle and still cannot limit a large inrush current when the filter inductance is small.

There are some control delay compensation methods proposed to reduce the impact of control delay on the converter predictive control [14], [15]. However, these methods are based on precise modeling of the converter and the system it is connected to. Their performance is highly sensitive to the accuracy of the modeling. Since grid voltage disturbances are mostly caused by faults and are unpredictable, it is not practical for the converter control to predict and compensate for the impact of the control delay at the transient of the grid voltage disturbance. Therefore, control delay compensation does not work for the grid-connected converter because of the unpredictable grid conditions.

To suppress the fast-rising inrush current during a short period, compared to a software-based method, a hardware-based method is more suitable. In [16], a triple-loop short-circuit current limiter and protection control strategy are proposed to limit the overload or short circuit in a three-phase inverter. A current hysteretic loop is used to determine whether the PWM pulses need to be temporarily masked or not, to suppress the fast-rising current. However, no detailed experiment results are introduced in this article, and the method is not tested in the grid-connected converter, which has a different and more complicated control.

In this article, the method used in [16] is extended to the grid-connected converter, aiming at addressing the inrush current during grid voltage disturbances due to the converter control delays and the small filter inductance. The cause for the inrush current is analyzed first. Then, the PWM mask method principles, impact, design, implementation, and verification are provided. This article is an extension of [17], and the main improvements are given as follows.

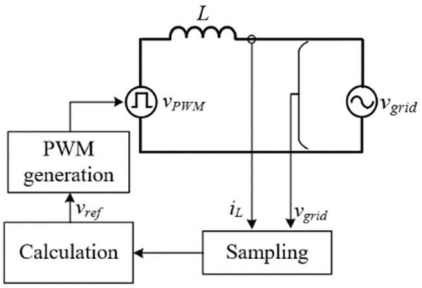

Fig. 1. General control diagram of voltage source inverter.

1) Converter control delays related to the inrush current are more comprehensively identified.
2) The method is extended from LVRT to more grid voltage disturbances, including low voltage disturbance, high voltage disturbance, and phase angle change.
3) The impact of the method on the converter control is discussed.
4) The experiment tests are extended from LVRT to low voltage disturbance, high voltage disturbance, and phase angle change.

The rest of this article is organized as follows. In Section II, the reason for the inrush current considering grid voltage disturbances is theoretically analyzed, and delays related to the inrush current are identified. Then, the operating principle, design considerations, and implementation of the PWM mask method are provided in Section III. In Section IV, experiment tests considering different grid voltage disturbances are provided. Finally, this article concludes with Section V.

II. Inrush Current Analysis During Grid Voltage Disturbances

The grid-connected converter controls its ac current by controlling its PWM voltage so that the voltage on the inductor is controlled. The difference between the converter output PWM voltage and the grid voltage causes the current changes. If the grid voltage changes suddenly, the converter voltage is desired to be correspondingly changed to avoid the current change beyond the desired range.

A. Cause for the Inrush Current

As shown in Fig. 1, the grid-connected VSC has the control process of sampling, calculation, and PWM generation. The converter output power is controlled through the filter inductor current control, and the differential equation of the filter inductor L is

$$v_L(t) = L\frac{di_L(t)}{dt} = v_{\mathrm{PWM}}(t) - v_{\mathrm{grid}}(t). \tag{1}$$

Through sampling the grid voltage, v_{grid}, and PLL, the controller obtains the grid voltage amplitude and angle. A voltage reference, v_{ref}, is generated by the controller and output through the PWM modulation and device switching, to control the inductor current, i_L, following the reference. Therefore, the

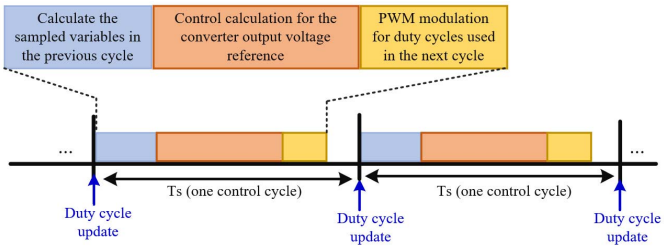

Fig. 2. Control process of the grid-connected converters.

grid voltage amplitude and phase angle information are critical for the grid-connected converter control.

In the steady-state operation, the per-unit inductance value can be small, especially, in SiC-based converters because of their high switching frequencies. In this case, the averaged value of the PWM voltage is close to the grid voltage under normal operation. However, when the grid voltage, v_{grid}, has a sudden change, due to the control delays, the converter cannot immediately change its output voltage to maintain the inductor current. Then, the voltage difference between the inductor terminals suddenly increases, depending on how large the grid voltage changes. The inductor current will also increase, and an inrush current will occur, which can be estimated as

$$\Delta i_L \approx \frac{v_{\text{grid0}} - v_{\text{grid1}}}{L} T_d \tag{2}$$

where v_{grid0} and v_{grid1} are the grid instantaneous voltages before the sudden change and after the sudden change, respectively, and T_d is the total delay time, which consists of all the delays in the converter control loop, including sampling, calculation, PWM modulation, and device switching. From (2), it can be found that a larger grid voltage change and a longer control loop delay result in a higher inrush current. The grid voltage change is mainly determined by the grid conditions, while the control loop delay is related to the converter controller.

B. Grid Voltage Sampling Delay

There are several different sampling strategies, one commonly used strategy is sampling signals multiple times in each converter control cycle and then calculating their averaged values. The averaged results will be used to execute control calculation in the next control cycle, so one control cycle delay is induced in the sampling process. The sampling delay is denoted as

$$T_{\text{sample\_delay}} = T_s \tag{3}$$

where T_s is the control period, which usually equals the switching period.

Besides, some regulation circuits, consisting of LPFs, are commonly adopted to filter and process the analog signals before they are sampled by the analog-to-digital converter (ADC) or other equivalent devices. The LPF, if used, also introduces some delay, which is denoted as $T_{\text{Volt\_filter}}$.

C. Control Delay

The control process of the grid-connected converter is shown in Fig. 2. The sampling data are calculated at the beginning of each control cycle and then used as the input for the converter controller. Based on the control strategy, the converter controller calculates the new output voltage reference. Then, the voltage reference is converted into duty cycles for different switches by the PWM modulation function. However, the new duty cycles calculated in each control cycle cannot be applied to the PWM generator until the duty cycle is updated, which is usually at the end of each control cycle. As a result, the converter PWM voltage output, v_{PWM}, will be updated in the next switching cycle. Therefore, there is an inherent control delay, T_{c_delay}, which is around one and a half control cycles, i.e.,

$$T_{c\_\text{delay}} = 1.5 T_s. \tag{4}$$

D. Grid Voltage Feedforward Delay

As introduced in Section II, the grid voltage feedforward control is widely used in the grid-connected converter to improve its dynamic response to the grid disturbance. It can be realized in either the *dq* synchronous frame or the *abc* domain.

In the *dq* synchronous frame, the feedforward *dq*-axis voltages, v_d and v_q, come from the grid voltage PLL. Considering the unbalanced grid voltage during abnormal grid conditions, the positive and negative sequences of the grid voltage may need to be decoupled with a decoupling network and/or filter [18], [19]. The decoupling process introduces a long delay, resulting in a slower PLL dynamic response, which negatively affects the grid voltage feedforward performances.

Compared to the *dq* domain-based feedforward control, the feedforward control in the *abc* domain gets a much faster grid voltage tracking performance because no decoupling network is needed, but control stability issues may happen due to the sampling noises. Therefore, some analog or digital filters may still be needed, which introduces some delay too.

Overall, the delay introduced by the grid voltage feedforward control is denoted as $T_{\text{FF\_delay}}$.

E. Total Delay Time

Without the grid voltage feedforward control, when the grid voltage suddenly changes, the current control loop can also regulate the voltage reference output, and eventually, the new converter output voltage will be close to the new grid voltage. However, the current regulation speed is slower than that of the grid voltage feedforward control. Therefore, two control loops, i.e., the current control loop and the grid voltage feedforward loop, work together to help the converter perform during the grid voltage disturbance. To simplify the analysis, the total delay time, T_d, is assumed to be the sum of all the delays in the grid voltage feedforward loop, which include the grid voltage sampling delay $T_{\text{sample\_delay}}$, voltage sampling LPF delay $T_{\text{volt\_filter}}$, control delay T_{c_delay}, and the feedforward delay $T_{\text{FF\_delay}}$, i.e.,

$$T_d = T_{\text{sample\_delay}} + T_{\text{volt\_filter}} + T_{c\_\text{delay}} + T_{\text{FF\_delay}}. \tag{5}$$

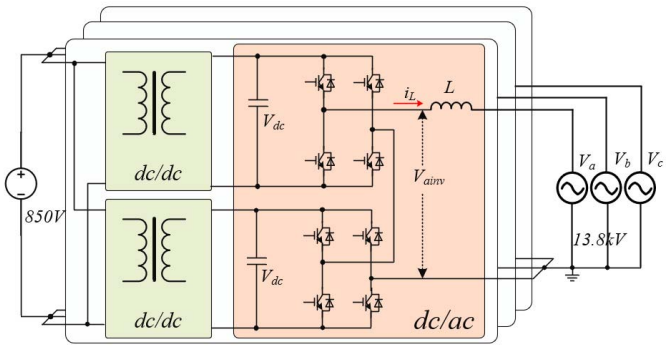

Fig. 3. PCS converter topology.

$T_{\text{sample\_delay}}$ and T_{c_delay} are almost linearly proportional to the control and switching period. $T_{\text{volt\_filter}}$ and $T_{\text{FF\_delay}}$ are mainly caused by filters, which are usually designed to pass through the fundamental frequency but filter out the high-frequency harmonics and noises. Generally, the filter crossover frequencies increase less than the amount of switching frequency increases. Therefore, the total delay time is a decreasing concave-up function of the switching frequency.

Substituting (3) and (4) into (5) results

$$T_d = 2.5T_s + T_{\text{Volt\_filter}} + T_{\text{FF\_delay}}. \tag{6}$$

The minimum T_d can be estimated by assuming that the voltage sampling filter delay and the feedforward delay are neglectable, and then,

$$T_{d\_\text{min}} = 2.5T_s + 0 + 0 = 2.5T_s. \tag{7}$$

F. Per-Unit Inrush Current

The per-unit inrush current value can be written as

$$\Delta i_{L\_\text{pu}} = \frac{\Delta i_L}{I_{\text{base}}} = \frac{\frac{v_{\text{grid0}} - v_{\text{grid1}}}{L} T_d}{\frac{V_{\text{base}}}{Z_{\text{base}}}} = \frac{\omega \cdot \Delta v_{\text{grid\_pu}}}{L_{\text{pu}}} T_d \tag{8}$$

where I_{base}, V_{base}, and Z_{base} are the base value of the converter current, voltage, and impedance, respectively, ω is the fundamental angular frequency in rad/s, $\Delta v_{\text{grid\_pu}}$ is the per-unit grid voltage change, and L_{pu} is the per-unit filter inductance.

From (8), it can be found under a constant per-unit grid voltage change, the per-unit inrush current value is linearly proportional to the total delay time and inversely proportional to the per-unit filter inductance value.

G. Example

To give a clear idea about how large the inrush current could be, a SiC-based multilevel converter is taken as an example. As shown in Fig. 3, a three-phase four-wire power conditioning system (PCS) converter is used to connect an 850-V dc grid to the 13.8-kV ac grid. The converter parameters of the dc/ac stage are shown in Table I. The ac-side filter inductance is around 0.009 p.u., which is selected based on the grid-side current harmonic requirement due to the high switching frequency and multilevel voltage.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
AC grid root mean square (RMS) voltage (line-to-line)	13.8 kV
MV dc-link voltage V_{dc}	6.7 kV
PCS converter power rating	100 kVA
Filter inductor L	44 mH (0.009 p.u.)
Switching frequency of each device	10 kHz
Sampling and control frequency	10 kHz

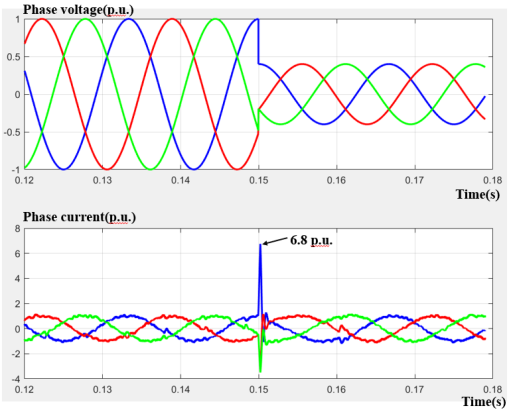

Fig. 4. Simulation waveforms of the grid voltage sudden drop.

Assume that the grid voltage suddenly changes from 1.0 to 0.4 p.u., and the total control delay is $2.5T_s$. Based on (2), the inrush current is

$$\Delta i_L = \frac{\frac{13.8\ \text{kV}}{\sqrt{3}} \times \sqrt{2} \times (1.0 - 0.4)}{44\ \text{mH}} \times 250\ \mu\text{s} = 39\ \text{A} \tag{9}$$

and its per-unit value is

$$\Delta i_{L\_\text{pu}} = \frac{\Delta i_L}{I_{\text{base}}} = \frac{39\ \text{A}}{5.9\ \text{A}} = 6.5\ \text{p.u.} \tag{10}$$

The corresponding simulation waveforms are shown in Fig. 4. At 0.15 s, the grid voltage suddenly drops from 1.0 to 0.4 p.u., and the maximum phase current is around 6.8 p.u.

III. PWM MASK METHOD TO LIMIT THE INRUSH CURRENT

To limit the inrush current and avoid the use of a large filter inductor, a hardware-based PWM mask method is adopted. It temporarily masks the PWMs when the ac current amplitude exceeds a preset value and releases the PWMs when the current amplitude reduces below another preset value. The following introduces the key considerations of the method.

A. PWM Mask Method

To make it clear, the method is introduced based on the dc/ac stage in Fig. 3, which is redrawn in Fig. 5, but this

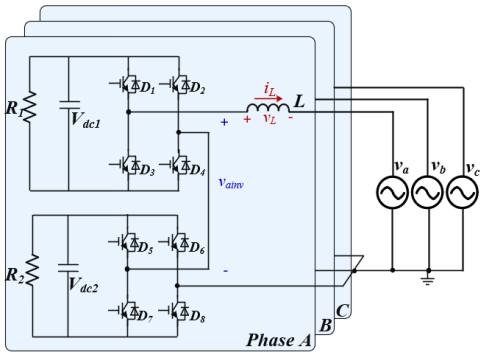

Fig. 5. Cascaded H-bridge-based grid-connected converter.

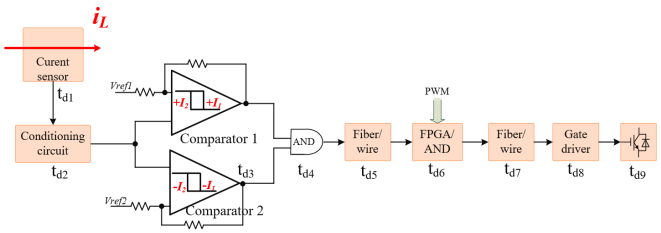

Fig. 6. PWM mask control loop.

method can be easily extended to other topologies. Since the three phases in Fig. 5 are identical, the following analysis is only based on phase A.

In this case, (1) can be rewritten as

$$v_L = L\frac{di_L}{dt} = v_{a\text{inv}} - v_a. \tag{11}$$

Assume that the grid voltage, v_a, and the inductor current, i_L, are positive at the beginning. Since the inductance is small, the PWM average voltage during one switching cycle, $v_{a\text{inv}}$, should be close to v_a. When v_a suddenly decreases, the inductor voltage, v_L, will be positive, and the inductor current increases, resulting in a positive inrush current. If the PWM pulses for all the devices in this phase are temporarily masked, all switches will be turned off. Then, the inrush current flows through diodes D_2, D_3, D_6, and D_7, and $v_{a\text{inv}}$ will be $-(V_{\text{dc1}}+V_{\text{dc2}})$, which is smaller than v_a, so v_L becomes negative and the inrush current decreases. Hence, the positive inrush current is limited.

On the other hand, if v_a suddenly increases, v_L becomes negative and i_L decreases, resulting in a negative inrush current. When PWM pulses are masked, the inrush current flows through diodes D_1, D_4, D_5, and D_8, and $v_{a\text{inv}}$ equals $V_{\text{dc1}} + V_{\text{dc2}}$, which assumes to be larger than v_a; then, v_L becomes positive and the inductor current increases. Then, the negative inrush current is limited.

As long as the overall dc-link voltage, $V_{\text{dc1}} + V_{\text{dc2}}$, is higher than the grid voltage amplitude, no matter which direction the grid voltage changes, when PWMs are masked, the inductor voltage polarity will be reversed, and the inductor current will change in the opposite direction. Then, the inrush current is limited.

B. PWM Mask Implementation

To realize ultrafast response (much faster than the digital controller), the PWM mask is implemented with a hardware-based method, and the circuit scheme is shown in Fig. 6. The inductor current is sampled by the current sensor, which already exists in the converter. A conditioning circuit is used to filter out the high-frequency noise and regulate the signal to be within a proper voltage range. The signal is then sent to the comparator to determine whether the PWMs need to be masked or not. Since the inductor current is alternating between positive and negative, two comparators are used to compare the signal with the references at both the positive and negative polarities. Hysteresis is adopted in the comparator design considering the noise immunity and switching loss, which will be introduced later. I_1 and I_2 in Fig. 6 are the corresponding inductor current threshold values of the two comparators for PWM mask and release, respectively. The comparator outputs are combined by an AND gate so that either the positive inrush current or the negative inrush current can trigger the PWM mask. The AND gate output signal is transferred to the converter controller board to determine whether the corresponding PWM signals need to be masked or released, which can be realized in a field-programmable gate array (FPGA) or logic circuitry. After that, the gate signals are transferred to the gate driver to drive the devices.

C. PWM Mask Threshold Value Ith1

The PWMs need to be masked when the inductor current exceeds a threshold value, I_{th1}. The determination of I_{th1} needs to consider the converter steady-state operation current and the instantaneous overcurrent protection or the device overcurrent capability.

First, I_{th1} should be larger than the converter maximum peak current, $I_{\text{pk\_ss}}$, in the steady-state operation to avoid false triggering. Also, I_{th1} needs to be smaller than the minimum converter instantaneous overcurrent protection values, which includes both the hardware instantaneous overcurrent protection, $I_{\text{ins\_OC\_hw}}$, such as device desaturation protection, and the software instantaneous overcurrent protection, $I_{\text{ins\_OC\_sw}}$. This aims at preventing the converter from tripping during grid voltage disturbances. Since the overcurrent protection values are within the device capability, this criterion can also make sure that the limited inrush current does not exceed the device capability.

Therefore, the PWM mask threshold value, I_{th1}, should be within the range of

$$I_{\text{pk\_ss}} < I_{\text{th1}} < \min(I_{\text{ins\_OC\_hw}}, I_{\text{ins\_OC\_sw}}) \tag{12}$$

and some margins at both the lower side and the higher side are necessary to make it more robust.

D. PWM Release Threshold Value Ith2

The PWMs need to be released when the current decreases to a certain value. The determination of the PWM release threshold value, I_{th2}, needs to consider the device switching loss as well as the current variation range.

As discussed above, when the PWMs are masked, the current amplitude starts to decrease. If the PWMs are released once the inductor current is smaller than I_{th1}, the current will increase again if the controller still has not responded to the grid voltage change. Then, the current will quickly exceed I_{th1}, and the PWMs will be masked and released again, back and force. This results in a high equivalent switching frequency and also high switching losses. A smaller release threshold value leads to a longer time for the inductor current to decrease after the PWMs are masked, and therefore, the fewer switching actions the devices will have.

Therefore, the range of I_{th2} could be

$$0 < I_{\text{th2}} < I_{\text{th1}}. \tag{13}$$

However, the smaller I_{th2} results in a larger current variation, and the converter controller response may be impacted, taking a long time to recover from the disturbance to the steady state.

E. Impact of the PWM Mask Control Loop Delay

The PWM mask control loop is straightforward, but it also introduces a control delay, which needs to be considered in the threshold value determination. As shown in Fig. 6, each stage in the loop introduces a delay, from t_{d1} to t_{d9}, and the total PWM mask control delay T_{d_pm} can be estimated as

$$T_{d\_\text{pm}} = \sum_{k=1}^{9} t_{dk}. \tag{14}$$

The PWM mask control loop delay impacts the real maximum inrush current. If the inductor current increases to I_1 at time $t = 0$, the PWMs will not be masked until $t = T_{d\_\text{pm}}$. During this period, the inductor current will keep increasing, and finally, the maximum inrush current will be higher than I_1. Therefore, to limit the inrush current at the threshold value, I_{th1}, the comparators threshold value, I_1, should be

$$I_1 \approx I_{\text{th1}} - \frac{\Delta V_a}{L} T_{d_{\text{pm}}}. \tag{15}$$

Similarly, I_2 should be

$$I_2 \approx I_{\text{th2}} + \frac{\Delta V_a}{L} T_{d\_\text{pm}}. \tag{16}$$

Usually, T_{d_pm} is small, in the nanosecond range, due to the small hardware signal delay time, so its impact on the inrush current limitation is small. However, if there are any components that introduce a large delay, their impact cannot be neglected.

F. PWM Mask Process

The scheme of the PWM mask process during the grid voltage change is shown in Fig. 7. A grid voltage suddenly changes at time t_1, and the inductor current starts to increase. At time t_2, the inductor current exceeds I_1, but PWMs will not be masked until time t_3 due to current sampling and the PWM mask control delay. At time t_3, all PWMs in the phase are masked, the inductor current starts to decrease, and the PWMs are released at time t_4. However, at time t_4, the converter controller may still have not detected or responded

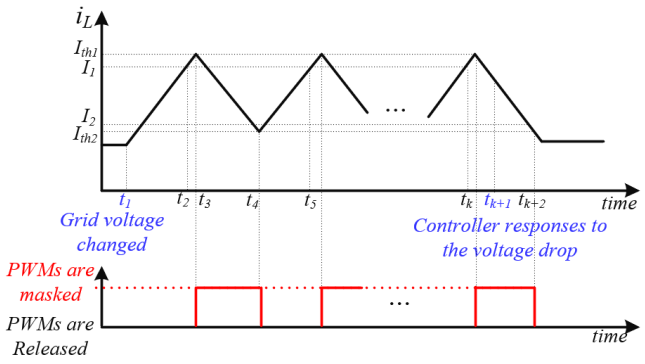

Fig. 7. Scheme of the PWM mask process.

to the grid voltage change, and then, the inductor current will increase again. Until time $t = t_{k+1}$, the converter controller has detected the grid voltage change and started to regulate its output voltage based on the new grid voltage, the inductor current can be regulated by the controller to its reference after the PWMs are released.

G. Relationship to the Converter Control

The PWM mask method does not negatively affect the regular converter controller because the following conditions hold.

1) The PWM mask will only be enabled when the inrush current is higher than I_1, which should not occur during the converter steady-state operation.
2) When the PWMs are masked, the converter outputs either the positive or negative dc-link voltage to limit the inductor current increasing. Without the PWM mask function, the converter current controller will also change the converter output voltage to control the current back to normal. However, this could take several control cycles and is slower than the PWM mask function.
3) When the inrush current drops back to the normal range, the PWMs will be released, and the converter controller can continue its control.

Therefore, the PWM mask method helps the converter controller to limit the inrush current. It works as a hardware-based feedforward control, and the difference is that it only provides either positive dc-link voltage or negative dc-link voltage.

H. Considerations for Different Grid Voltage Disturbances

The grid voltage disturbances include voltage amplitude change and angle change, and the former consists of low voltage disturbance and high voltage disturbance.

For low voltage disturbance, the PWM mask function can effectively limit the inrush current since the dc-link voltages are always higher than the grid voltage and the inductor current will be reduced when charging the dc-link capacitors.

For high voltage disturbance, if the grid voltage is lower than the dc-link voltage, the method will have the same results as the low voltage disturbances. However, if the grid voltage is higher than the dc-link voltage, the inrush current may not be effectively limited since the inductor voltage cannot

be inverted after the PWMs are masked. However, with the method, the inductor current increase rate can be reduced, and it can help the converter to ride through short overvoltage conditions. To ride through long-term overvoltage conditions, the converter has to be designed considering the maximum grid voltage, which is, however, not the focus of this article.

The voltage angle change is also a severe condition since it takes some time for the converter PLL to catch up with the new angle. The exact delay time depends on the dynamic performance of the PLL controller. For example, in [20], based on the hardware-in-the-loop (HIL) test results, the response time of the PLL to a 60° change is around 8 ms for a PLL with a 50-Hz filter. During this delay time, the angle difference between the converter output voltage and the real grid voltage increases, which leads to a large voltage difference on the filter inductor, and therefore, an overcurrent occurs. With a small filter inductance, the sudden change of the grid voltage may result in an extremely large inrush current, as can be seen in the later experiment test results. With the PWM mask method, the inrush current induced during the grid voltage angle change can be effectively limited.

IV. Experimental Verification

To validate the analysis and the effectiveness of the approach, an experimental setup is built, and the approach is tested under three different grid voltage disturbance conditions, including low voltage, high voltage, and voltage phase angle change.

A. Test Setup

As shown in (8), the inrush current induced by the grid voltage disturbance does not rely on the converter voltage and power ratings. Instead, it relates to the per-unit values of the grid voltage change and filter inductance, as well as the controller delay. Therefore, the PWM mask approach can be effectively validated in the small-scale prototype considering the per-unit values.

A small-scale prototype of the converter shown in Fig. 3 is built based on SiC MOSFET and used to validate the converter controller, including the PWM mask function. The test setup picture is shown in Fig. 8(a), and its scheme is shown in Fig. 8(b). Some main parameters of the component and control parameters are summarized in Table II.

A Si insulated-gate bipolar transistor (IGBT)-based three-phase two-level converter is used as the grid emulator, and the grid voltage amplitude and angle change can be easily emulated through the grid emulator converter controller. To provide fast grid voltage disturbance, the grid emulator does not have an ac output filter and open-loop control is used. The dc-link voltage is 150 V, and the grid voltage peak is 135 V, which is also the voltage base value of the test setup. The switching frequency of each device in the grid emulator is 10 kHz, and the equivalent switching frequency at the ac side is 20 kHz because of unipolar PWM modulation. A second-order *RC* LPF is used to observe the variation of the emulated grid voltage, and it does not impact the power loop because of the large resistance.

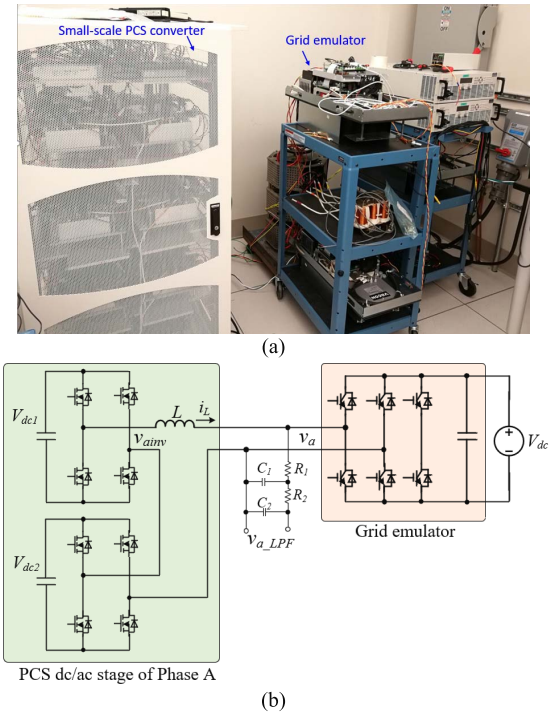

Fig. 8. Test setup: (a) picture and (b) scheme.

TABLE II
Experiment Setup Parameters

Component	Parameters	Value
Grid emulator	Dc-link voltage, V_{dc}	150 V
	Ac grid voltage peak (voltage base value)	135 V (1 p.u.)
	Ac voltage frequency	60 Hz
	Switching(control) frequency	10 kHz
	Ac-side equivalent switching frequency	20 kHz
PCS Converter	Switching(control) frequency	10 kHz
	Ac-side equivalent switching frequency	40 kHz
	Ac current base value	10 A (1 p.u.)
	Filter inductance L	670 uH (0.0187 p.u.)
	PWM mask threshold vale I_{th1}	25 A (2.5 p.u.)
	PWM release threshold value I_{th2}	15 A (1.5 p.u.)
	Dc-link voltage reference	V_{dc1}=V_{dc2}=80 V
The 2nd-order RC filter	Resistor	R_1=R_2=1 kΩ
	capacitor	C_1=C_2=22 nF
	Crossover frequency	7.23 kHz

Only one of the three phases in the PCS converter is used for the test because the PWM mask function should behave the same in the three-phase case. The dc loads do not impact the transient performance of the PCS converter during the grid voltage disturbance because of the short duration (hundreds of microseconds). Therefore, no load is applied on the two dc-links, and the single-phase PCS converter works as a static

synchronous compensator (STATCOM). The setup is valid for verifying the PWM mask function.

A single-phase PLL based on the second-order generalized integrator (SOGI) is used to obtain the grid voltage amplitude, frequency, and phase angle. The dc-link voltage control and voltage balancing control are also adopted. The grid voltage feedforward control is realized based on the PLL output voltage rather than the instantaneous sampled grid voltage considering the noise impact. Each device switches at 10 kHz, and the ac-side equivalent switching frequency is 40 kHz with phase shift unipolar PWM modulation. The grid-side voltage and current are sampled with VFC-110, and the converter calculates the average voltage and current once in each control cycle.

B. Low Voltage Disturbance Test

The low voltage disturbance test was first conducted, and Fig. 9 shows the waveforms of the ac-side voltages and current when the PWM mask function is disabled. The grid voltage suddenly dropped from 1 to 0.25 p.u. at time t_1, lasted for ten cycles (0.17 s), and then recovered back to 1 p.u. at time t_2. It can be found from Fig. 9(a) that the inrush current at the transient of grid voltage drop is around 50 A (5.0 p.u.), and the inrush current at the transient of grid voltage recovery is around 60 A (6.0 p.u.). Fig. 9(b) shows the zoomed-in waveforms at time t_1. The grid voltage v_a suddenly dropped (duty cycle suddenly changed) at time t_1, but the PCS output voltage, $v_{a\text{inv}}$, did not change until 200 μs later, which can be observed from the duty cycles of the PWM voltage, v_{a_inv}. During this period, the inductor current, i_L, quickly increased. After 200 μs from time t_1, the converter controller started to regular the current based on the current feedback, and it can be found that the PWM voltage duty cycles started to change. However, the PLL SOGI filter leads to a large PLL delay in the voltage feedforward control, so the voltage feedforward did not help the converter to respond to the grid voltage change at that time. Similar phenomena can be observed at the time of grid voltage recovery, which is t_2 in Fig. 9(c).

Then, the same test was conducted with the PWM mask function enabled, and the waveforms are shown in Fig. 10. From Fig. 10(a), it can be found that the inrush current was effectively limited at I_{th1}, i.e., 25 A (2.5 p.u.), at the transients of both the voltage dropping and recovery. The zoomed-in waveforms are shown in Fig. 10(b) and (c). It can be found that when the inrush current reached the PWM mask threshold value, the PWMs were masked, and the PCS converter output voltage is either the positive or the negative overall dc-link voltage. After the PWMs were masked, the inductor current absolute value started to reduce. Once the current decreased to be smaller than the PWM release threshold value, the PWMs were released, and the inductor current started to increase again because the converter controller has not responded to the grid voltage change, which follows the principle discussed in Section III.

C. High Voltage Disturbance Test

Then, the high voltage disturbance test was conducted, and the waveforms without the PWM mask function are shown in Fig. 11. To realize the high grid voltage, the dc-link voltage of the grid emulator was increased to 230 V, but the steady-state grid voltage peak was still maintained at 135 V (1 p.u.). The grid voltage suddenly increased to 220 V (1.53 p.u.) at time t_1, which was already higher than the total dc-link voltage of the PCS converter, i.e., 180 V. A large inrush current up to 52 A (5.2 p.u.) was induced. Besides, the modulator of the PCS converter was saturated, and the current was out of control, so the current had a large variation during the whole grid overvoltage period. It is different from the waveforms shown in the low voltage disturbance test, i.e., Fig. 9(a), in which the inrush current only happens at the transient of grid voltage change, while at the steady state of the low-voltage period, the current is still stable. After the grid voltage decreased back to 1 p.u., it took a long period for the PCS converter to control the current back to the steady state because of the large current variation.

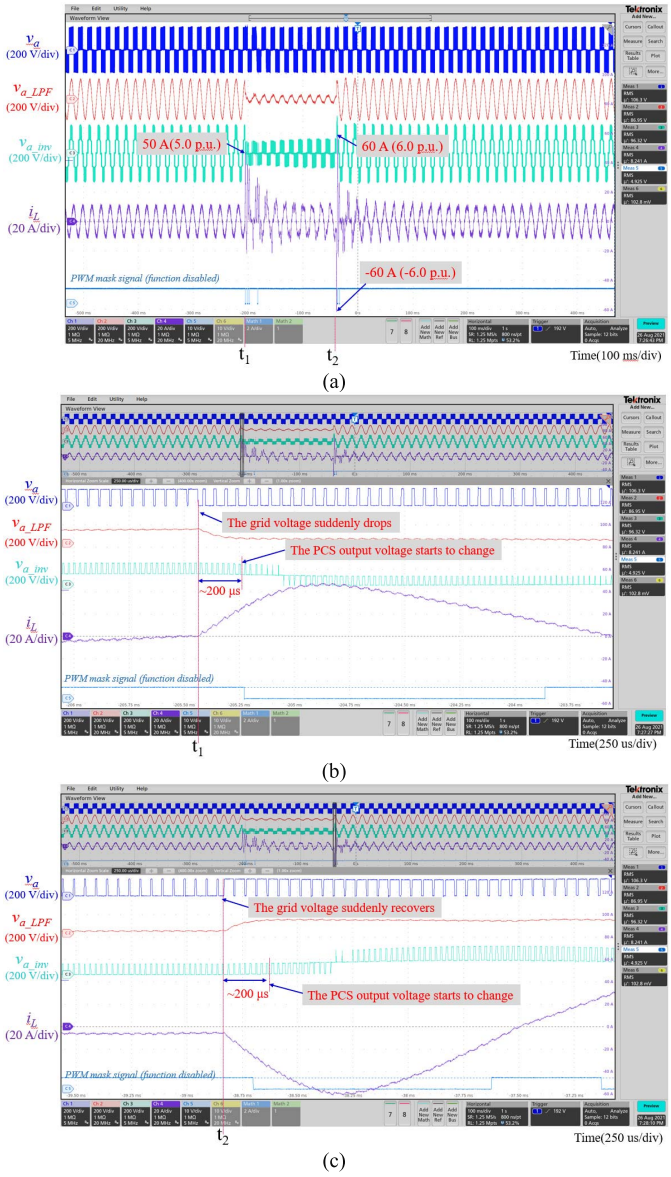

Fig. 9. Low voltage disturbance test waveforms without the PWM mask function: (a) overall waveforms, (b) zoomed-in at time t1, and (c) zoomed-in at time t2.

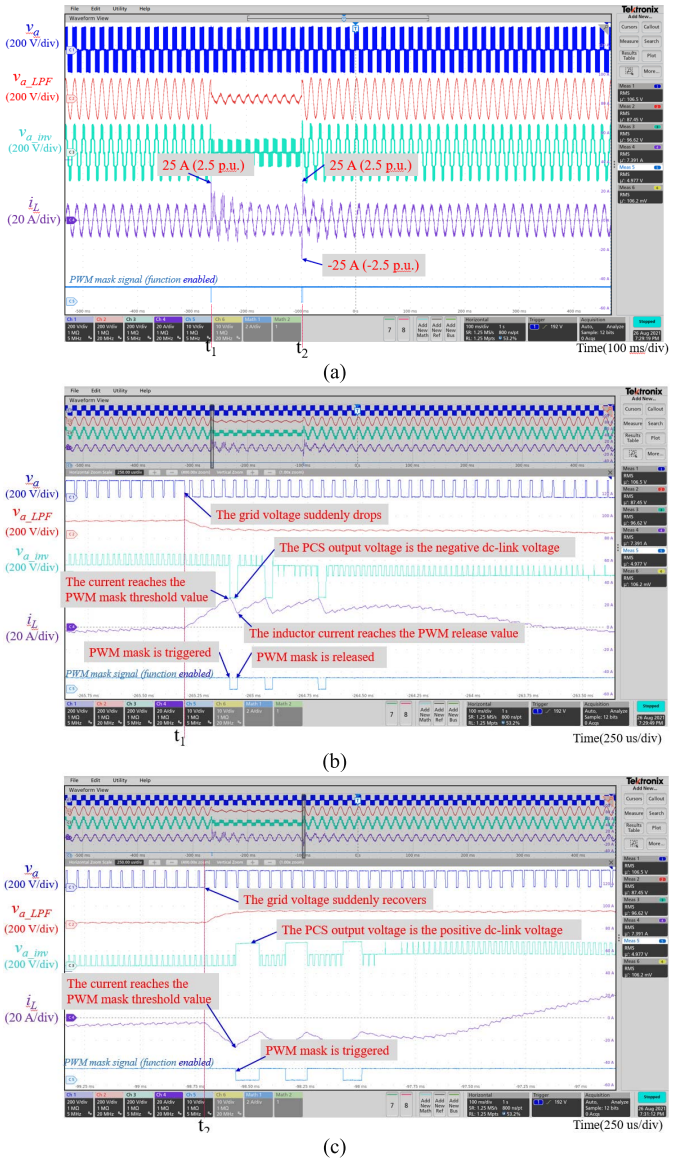

Fig. 10. Low voltage disturbance test waveforms with the PWM mask function: (a) overall waveforms, (b) zoomed-in at time t1, and (c) zoomed-in at time t2.

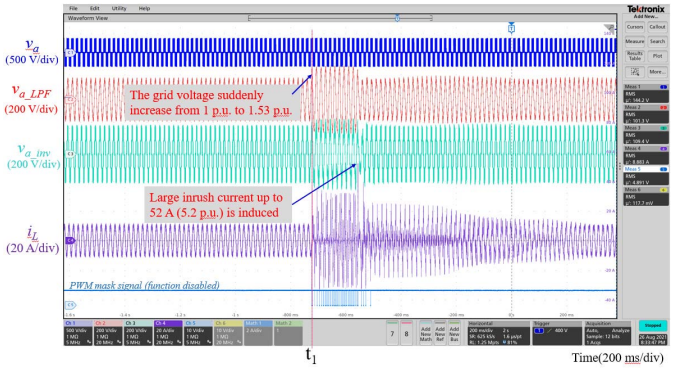

Fig. 11. High voltage disturbance test waveforms without the PWM mask function.

From the PCS output voltage waveforms, it can be found that the dc-link voltages of the PCS converter increased due to the modulation saturation. This is mainly because the grid

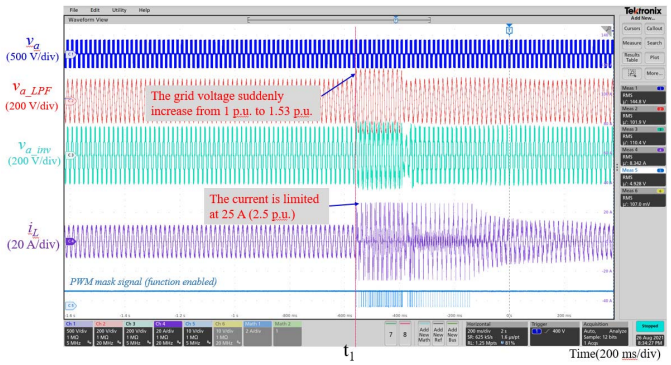

Fig. 12. High voltage disturbance test waveforms with the PWM mask function.

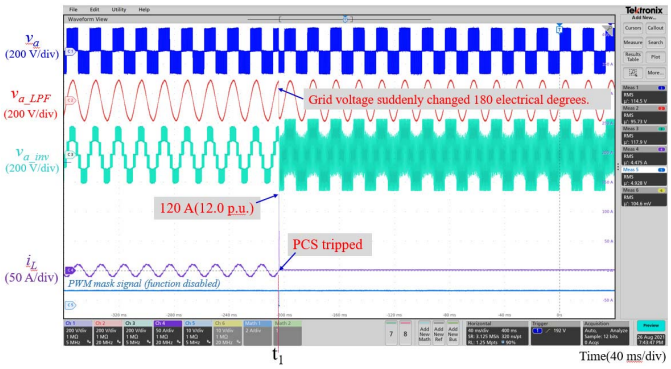

Fig. 13. Phase angle change test waveforms without the PWM mask function.

overvoltage is higher than the PCS converter dc-link voltage, and it puts more voltage stress on the devices. Therefore, in the real converter design, if the converter needs to ride through such a high grid voltage, it needs to be designed considering this.

Then, the same high voltage disturbance test was conducted with the PWM mask function, and the waveforms are shown in Fig. 12. Due to the insufficient dc-link voltage, the PCS converter also had modulation saturation, and the overcurrent occurred. However, thanks to the PWM mask function, the current peaks were limited at around 25 A (2.5 p.u.). Also, after the grid voltage was recovered, it took a shorter period for the converter to go back to the steady state, compared to the test without the PWM mask function.

Therefore, although the PWM mask function cannot avoid the modulation saturation or the current variation in the grid overvoltage conditions, where the grid voltage peak is higher than the dc-link voltage, it can still help to limit the current peaks.

D. Phase Angle Change Test

The grid voltage phase angle change test was also conducted without the PWM mask function first. The waveforms are shown in Fig. 13. The grid voltage angle suddenly changed 180 electrical degrees at time t_1, and a large inrush current up to 120 A (12 p.u.) was induced. The overcurrent protection of the PCS converter was triggered due to the extremely high inrush current, and the PCS converter tripped.

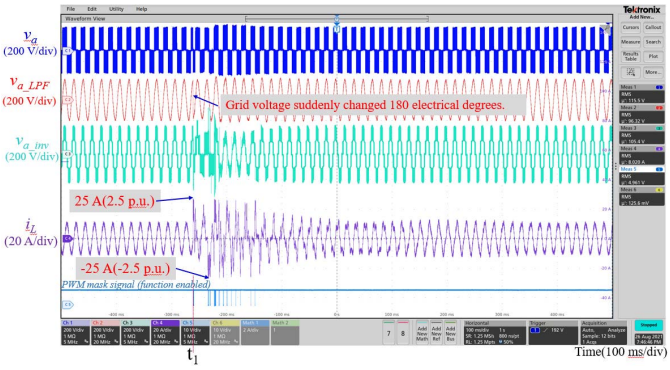

Fig. 14. Phase angle change test waveforms with the PWM mask function.

With the PWM mask function, the PCS converter rode through the same grid voltage phase angle change. As shown in Fig. 14, the grid voltage angle also changed 180 electrical degrees at time t_1, and the inrush current was successfully limited at 25 A (2.5 p.u.). Although a short period of current disturbance happened, which is because the PLL was trying to catch up with the new grid voltage angle, the PCS current finally went back to the steady state.

V. Conclusion

In this article, the PWM mask method is introduced to limit the inrush current of a grid-connected converter during grid voltage disturbances. The PWM mask method limits the inrush current by temporarily masking the PWM pulses. When the PWMs are masked, the inductor current flows through device diodes, and the voltage polarity applied on the inductor is reversed so that the inductor current is changed in the opposite direction. The determination of the PWM mask threshold values needs to consider the converter steady-state operation condition, overcurrent protection, switching losses during the disturbance, as well as the PWM mask control loop delay. Three different grid voltage disturbances, low voltage, high voltage, and phase angle change, are analyzed and tested. In the experiment tests, without the PWM mask function, the maximum inrush current during the low voltage, high voltage, and phase angle change is 6, 5.2, and 12 p.u., respectively. However, with the PWM mask method, they are all limited to their preset value, i.e., 2.5 p.u. With the PWM mask function, grid-connected converters can have more resilience to grid voltage disturbances.

Acknowledgment

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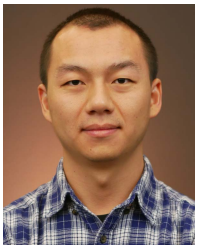

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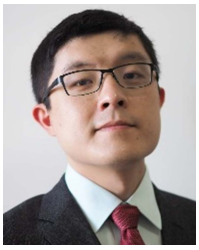

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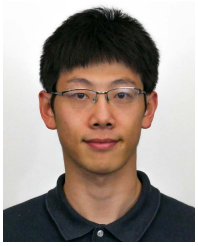

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