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RESEARCH ARTICLE

Design, Development, and Testing of a Flexible Combined Heat and Power (F-CHP) System With 10-kV SiC MOSFET-Based Power Conditioning System (PCS) Converter

HAIGUO LI[1,2], (Member, IEEE), ZIHAN GAO[1], (Student Member, IEEE), FEI WANG[1,3], (Fellow, IEEE), YIWEI MA[4], (Member, IEEE), YU SU[1], (Member, IEEE), DINGRUI LI[1], (Member, IEEE), PENGFEI YAO[5], (Member, IEEE), SHIQI JI[6], (Senior Member, IEEE), ZHE YANG[7], AND RUIRUI CHEN[1], (Member, IEEE)

[1]Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, Knoxville, TN 37996, USA
[2]ABB U.S. Research Center, Raleigh, NC 27606, USA
[3]Oak Ridge National Laboratory, Knoxville, TN 37831, USA
[4]Electric Power Research Institute (EPRI), Knoxville, TN 37932, USA
[5]China Huaneng Group, Beijing 100031, China
[6]Department of Electrical Engineering, Tsinghua University, Beijing 100084, China
[7]Monolithic Power System Inc., San Jose, CA 95119, USA

Corresponding author: Haiguo Li (hli96@alum.utk.edu)

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ABSTRACT This paper discusses the design, development, and testing of a flexible combined heat and power (F-CHP) system. It includes two parts: the power conditioning system (PCS) converter, which connects the system to the grid and is the key component to provide grid support services, and the F-CHP central controller, which accommodates the control of local sources, local loads, and the PCS converter. The functions and structures of the central controller are discussed. The central controller's system-level performances are verified with hardware-in-the-loop (HIL) tests, and the mode transition and grid transient performances are validated with power electronic converter-based hardware testbed (HTB) tests. The PCS converter is designed with 10-kV SiC MOSFETs. The grid requirements are considered in the 13.8-kV/1-MW PCS converter design, and the impact of different requirements on the converter design is identified. Also, converter scalability is studied with the paralleling operation. Two 13.8-kV/100-kW converter prototypes are developed to verify the converter design and scalability. The second prototype is an improved design of the first one; the volume is reduced by 49% and the efficiency at the rated output power is increased from 96.4% to 98.4%. The test results of the converter performances, grid support functions, and parallel operation are also discussed.

INDEX TERMS 10 kV SiC MOSFET, flexible combined heat and power (F-CHP) system, grid support, grid requirements, medium voltage converter, power conditioning system (PCS).

I. INTRODUCTION

As the penetration of intermittent renewable energy sources (RES), such as wind and solar, in the electric grid increases, the system needs more dispatchable power to balance the power generation and load consumption and maintain the stability of the grid. One solution is to build more energy storage systems, and another solution is to have more controllable loads and support from customers with

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distributed energy resources (DERs), for example, a customer with a combined heat and power (CHP) system.

A concept of flexible combined heat and power (F-CHP) system was recently proposed by the United States Department of Energy (DOE), aiming at getting dispatchable power from the CHP system [1]. Different from conventional CHP systems, which are sized only considering the customer's own power and thermal needs, the F-CHP system also considers additional power generation for grid support. With F-CHP, the grid operators can receive cost-effective dispatchable power and other ancillary grid support services, such as frequency and voltage support, and the F-CHP system owner can generate revenue from providing these services.

Although a power electronics converter interface is not required for the F-CHP system, it can bring many benefits to the grid and CHP customers [2]. Fig. 1 shows a demonstrated structure of an F-CHP system with a power electronics-based medium voltage (MV) ac to low voltage (LV) dc power conditioning system (PCS) as the interface between the MV distribution grid and local LV CHP sources and loads. The benefits of the PCS include: (i) Better integration of DERs in CHP system. For energy resources like PV, fuel cells, batteries, and microturbines, LV dc bus eliminates the need for dedicated dc/ac converters. Even for conventional turbine generators and reciprocating engine generators, the PCS, together with the LV dc/ac interface inverters in Fig.1, will enable the generator to operate at the optimal speed and unity power factor; (ii) Easier low/high voltage and frequency ride through because of the decoupled dynamics between the grid and the CHP system by the PCS; and (iii) Easier and smoother transition between the islanded-mode operation and grid-connected mode operation because of the fast response of the PCS. Furthermore, the PCS can provide additional system benefits, such as flexible voltage and frequency support, active harmonic filtering, and grid stability [3].

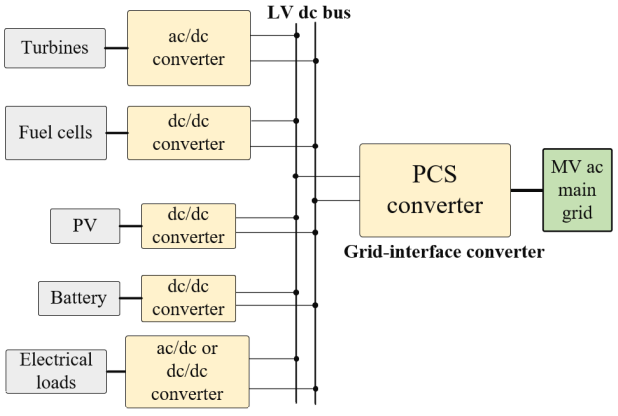


FIGURE 1. Power electronics-based F-CHP system.

Most of the CHP systems are in the power range of 1∼20 MW [4], [5], which requires a connection to the MV grid, typically 12 to 15 kV in North America. As a result, the PCS converter needs to be either a LV converter with a step-up transformer or a direct interfaced MV converter. The emerging high voltage (HV, >3.3 kV) silicon carbide (SiC) MOSFETs provide promising solutions for MV applications with advanced functionalities and low cost [6]. Compared to conventional silicon (Si) devices, SiC devices feature higher switching speed, lower switching loss, lower conduction loss, and higher maximum junction temperature [7], [8]. Therefore, a higher switching frequency can be realized in the SiC-based converter achieving the same or even higher efficiency [9]. As a result, the converter size can be reduced because of the smaller passive component and cooling system size, which can lead to lower converter cost [8], [10]. Also, high control bandwidth can be achieved with the high switching frequency, which brings system-level benefits, such as improved system stability and power quality [3]. In addition, compared to LV SiC devices, HV SiC devices facilitate the use of simpler topology and the direct connection with the MV grid without 50/60 Hz power transformers, which are heavy and bulky, and therefore the more compact, low-cost, and high-efficiency converter solution can be achieved [9], [11]. Therefore, in the F-CHP system, the HV SiC-based MV PCS converter brings more benefits.

There have been some research works and prototype demonstrations with HV SiC devices, including device characterization and modeling [12], [13], [14], solid-state transformers [9], [15], [16], solid-state circuit breakers [17], PV integration into the MV grid [10], [18], off-shore wind farm HVDC [19], and power conditioning system converter for asynchronous microgrids [20]. Many issues, challenges and improvement needs have been identified for components designed and approaches adopted for HV SiC-based converters because of the high voltage and high dv/dt of these HV SiC devices. These include: the gate drive and protection design considering the high dv/dt [21], [22], [23]; isolated gate drive power supply (GDPS) design considering the high insulation and low coupling capacitance requirements [24], [25], [26]; electric field management to realize high and reliable insulation [27]; the impact of parasitic capacitances on the device DPT-based dynamic characterization [28] and on the converter loss [29], [30]; sensor design considering the high dv/dt noise [31]; the MV converter testing approach [32]; and the insulation considerations [33], [34], [35], [36].

Moreover, to realize a seamless connection with the MV grid and to provide better grid support, the design of the PCS converter needs to consider grid requirements. IEEE Std. 1547 is a widely used standard for DERs, and it requires interconnection, operation modes, power quality, low- and high-voltage ride through (LVRT/HVRT), frequency ride through (FRT), and islanding [37]. Other grid conditions include grid faults, lightning surges, and unbalance. To provide the best grid support, the PCS converter needs not only to survive the grid's abnormal conditions but also to keep operating under most of these conditions. There are some research works considering the grid requirements in LV

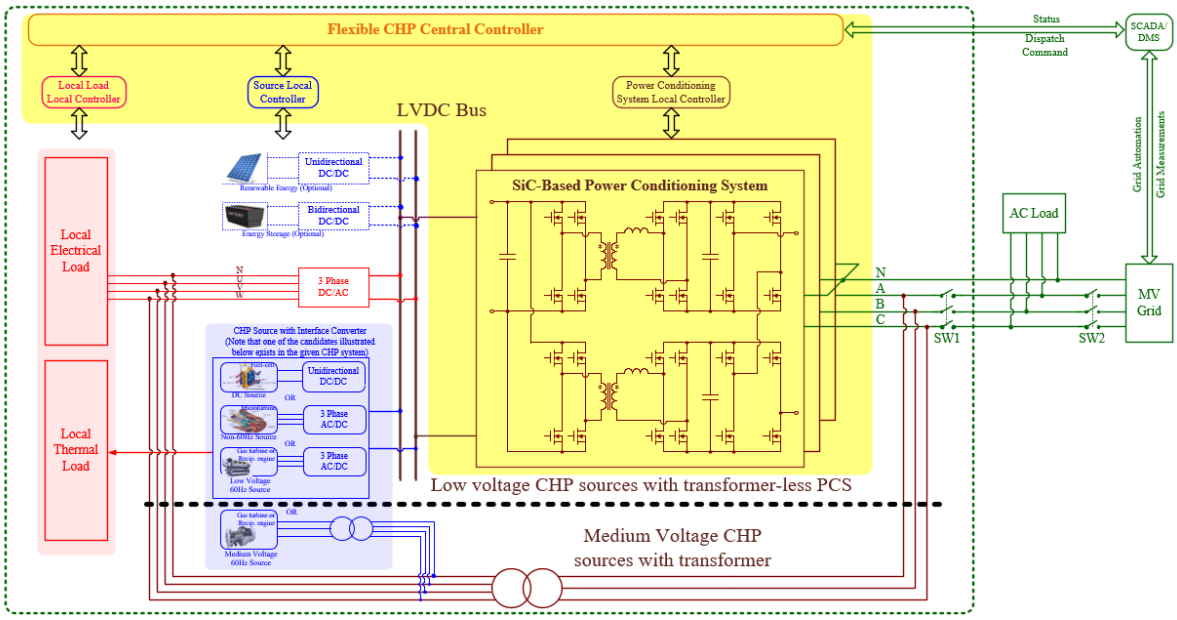


FIGURE 2. Configuration of the F-CHP system.

SiC-based converters, such as unbalanced grid voltage [38], [39], LVRT and HVRT [40], [41], fault ride through [42], [43], and MV SiC-based converters in terms of LVRT [44], [45], unbalance [46], and fault ride through. However, most of these works focused on converter control strategies, while the converter hardware design was rarely discussed.

A central controller is also critical to the F-CHP operation. The F-CHP central controller is similar to the central controller in a microgrid with similar control functions, including energy management, state machine, economic operation based on source and load forecasting, power balancing, protection coordination, model transitions, and data logging [47], [48]. The F-CHP central controller coordinates with local source and load controllers and can also communicate with the grid controller (SCADA/DMS), like in microgrid case. For the PCS-based F-CHP, the central controller also needs to coordinate with the PCS controller, similar to the case of the asynchronous microgrid [20].

Therefore, this paper presents the design, development, and testing of a PCS-based F-CHP system. The four main focuses are:

1) The 10 kV SiC-based MV converter hardware design considering grid requirements.
2) The MV converter hardware design, addressing challenges posed by fast switching SiC, such as high dv/dt, magnetic design considering high insulation, the impact of parasitic capacitances, and power loss reduction.
3) The MV converter testing and verifications.
4) The F-CHP central controller design and testing.

The rest of the paper is organized as follows. In Section II, the configuration, operation modes, and scalability of the proposed F-CHP system are first introduced. Then, the F-CHP central controller is discussed in Section III. In Section IV, the PCS converter design considering grid requirements is presented. In Section V, the first version of the MV PCS converter prototype design is provided, followed by its experimental results in Section VI. Next, the improvements of the second version of the MV PCS converter prototype are discussed in Section VII, followed by the experiments in Section VIII. In Section IX, the F-CHP central controller tests in the hardware-in-the-loop (HIL) and the power electronic converter-based hardware testbed (HTB) are presented. Finally, Section X concludes this paper.

II. THE F-CHP SYSTEM WITH POWER ELECTRONIC CONVERTERS

This section presents the configuration, operation modes, and scalability considerations of the proposed F-CHP system.

A. CONFIGURATION OF THE PROPOSED F-CHP SYSTEM

The configuration of the proposed F-CHP system is shown in Fig. 2. It consists of electrical sources, electrical loads, thermal loads, as well as the PCS converter. The electrical sources can be conventional CHP sources, such as the gas turbine or reciprocating engine, and non-50/60 Hz sources, for example, microturbines, or fuel cells. On the grid-side, the PCS converter is directly connected to the MV (e.g., 13.8 kV) distribution grid; on the CHP side, the PCS converter is connected to electrical sources and loads through a LV dc bus (e.g. 800 to 1000 V), considering CHP generators are mostly LV equipment (e.g. three-phase 480 to 690 V). A dc bus can simplify integration with sources needing power electronics interfaces, such as microturbines and fuel cells. Even for conventional 50/60 Hz synchronous generator interfaced sources, adding a power electronics interface

can be beneficial and more economical [49]. With the LV dc bus, renewable sources, such as PV, and battery-based energy storage systems (BESS), can also be integrated more efficiently.

The PCS adopts a two-stage topology. Because of the high blocking voltage of 10 kV SiC MOSFETs, a cascaded H-bridge (CHB) with two units for each phase is selected as the ac side topology, forming a five-level converter. Since all H-bridges in the three phases are identical, modular design can be achieved, which bring cost benefits and the flexibility for scaling. In addition, the CHB-based three-phase four-wire converter can be treated as three single-phase converters, so it can provide unbalanced support even with one phase having full load while other phases have no load. Dual active bridge (DAB) is selected as the dc/dc topology considering the bidirectional power transfer, soft switching, high voltage-step ratio, simple control, and low sensitivity to component parameters (inductance and capacitance). Also, the DAB converter realizes galvanic isolation, which can isolate faults between the LV dc side and the MV ac grid.

In addition to PCS, Fig. 2 also illustrates a central controller, which is essential to realizing F-CHP functions by coordinating the operation of local CHP sources, local loads, PCS, and the grid. As mentioned earlier, the F-CHP concept does not require the PCS. Fig. 2 shows the alternative connection through a 50/60 Hz transformer, which could also be used as a backup for the PCS-based approach. The focus of this paper is the PCS converter and the central controller, which are in yellow.

B. OPERATION MODES OF THE PROPOSED F-CHP SYSTEM

The F-CHP system can be operated similarly to a micro-grid. The two main operation modes of the F-CHP system are the grid-connected mode and the islanded mode. The F-CHP system operates in the grid-connected mode when the MV ac grid is available. In this mode, the system can exchange power with the ac grid based on the grid and local load needs. In normal operation, local CHP sources will supply local electrical and thermal load needs and can also supply electric energy/power to the grid per the arrangement between the utility and the CHP owner. The grid needs power/energy support, frequency/voltage support, and other ancillary services. In the grid-connected mode, the grid-side ac/dc stage of the PCS converter controls the MV dc bus voltage, while the CHP-side dc/dc stage controls the LV dc bus voltage. Therefore, to the grid, the PCS converter operates in grid following mode, and the local sources will control their power output.

When the MV ac grid is unavailable or required by the system operator, the F-CHP system can operate in the islanded mode. With the F-CHP central controller, the power balance between local sources and local loads on-site is achieved. Load shedding will happen when the overall power generation is less than the load consumption, and the critical loads have a higher priority to be supported than non-critical loads. In the islanded mode, if the F-CHP system has excessive power and is requested by the grid SCADA/DMS, it can also support the external balanced/unbalanced ac loads through the PCS converter. In this case, the dc/dc stage of the PCS converter controls the MV dc link voltage, and the dc/ac stage controls the MV ac side voltage and frequency, i.e., the PCS converter will operate in grid forming mode. The LV dc bus voltage can be controlled by the BESS if available, because of its fast power regulation speed. It can also be regulated by other sources.

C. SYSTEM SCALABILITY

Given that the F-CHP rating can range from 100s of kW to 10s of MW, it is desirable to have the PCS converter to be based on lower power rating modules (e.g., 1 MW module), and when needed, multiple such modules can be paralleled to meet the required power rating need. Aside from economic benefits, the modular design can also provide redundancy and better availability. On the other hand, it poses challenges to PCS design and control.

Three possible paralleling scenarios are shown in Fig. 3(a),(b), and (c). In Fig. 3(a), the F-CHP system only has one LV dc bus, and the PCS converters are paralleled at both the dc side and the ac side. In Fig. 3(b), the F-CHP system has multiple LV dc buses, and each dc bus has one PCS converter, connecting the dc bus to the same medium voltage (MV) ac grid. In Fig. 3(c), the F-CHP system has multiple LV dc buses, and each bus is connected to the MV ac grid by multiple PCS converters in parallel connection. In all three scenarios, the PCS converters are paralleled at the MV ac side, and the main difference is the LV dc side configuration. Moreover, multiple LV dc buses provide higher robustness in terms of dc bus faults. Fig. 3(a) can be easily extended to Fig. 3(b) and Fig. 3(c), and it needs almost all the techniques required for the paralleling control. Therefore Fig. 3(a) is selected as the focus paralleling scenario in this paper.

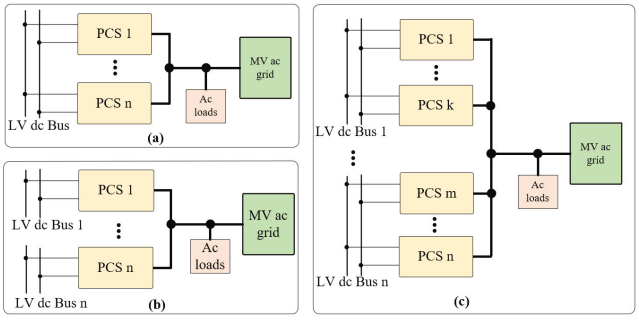


FIGURE 3. Converter paralleling with (a) both LV dc and MV ac, (b) only at MV ac, and (c) hybrid condition.

III. THE F-CHP SYSTEM'S CENTRAL CONTROLLER

As the brain of the F-CHP system, the central controller plays a key role in the system's control and communication with the grid operator. The function diagram of the proposed F-CHP system is shown in Fig. 4. The central controller

has functions of PV forecasting if PV sources are included, load forecasting, energy management, active power control coordination, protection coordination, data logging, and state machine.

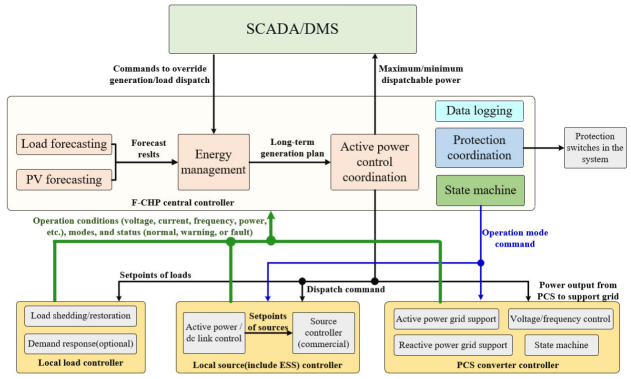


FIGURE 4. The function diagram of the F-CHP controllers.

A. LOAD AND PV FORECASTING

The goal of PV and load forecasting is to estimate the energy needs and decide the power command for sources (including ESS) based on the economical operation goal. Considering the capability of the F-CHP system to independently operate in islanded mode, the load forecasting function will use recent historical measurement data to make short-term forecasts. The Autoregressive Moving Average (ARMA) method [50], which is one of the simplest yet more reliable algorithms used for time-series data analytics, is used. Also, the load data of weekdays and weekends (also including holidays) is separated for load forecasting to obtain more accurate results.

The PV forecasting function also utilizes historical PV generation data available to the F-CHP controller to make short-term forecasts. To minimize the impact of weather, the PV forecasting function classifies days by the cloud cover conditions indicated by cloud cover indices and uses the ARMA, trained by the corresponding data set, to generate PV output forecasts.

B. ENERGY MANAGEMENT

The energy management function generates dispatch commands for the sources in the CHP system, as well as for the controllable loads served by the CHP system, utilizing the load and PV forecasting results. The dispatch is generated by solving optimization problems, usually mixed-integer linear programs that are specific to the current operating mode as well as the ownership of the CHP system.

In the grid-connected mode, for a time horizon of T (hours, multiples of 15 minutes, multiples of 5 minutes, etc.), the objective is to minimize the operation cost, which is

$$\sum_{i=1}^{T}\left(C^i_{CHP}+C^i_{import}+C^i_{DR}\right)+C_{Demand} \tag{1}$$

where i is the time step, $C^i_{CHP}, C^i_{import}, C^i_{DR}$ are costs associated with the CHP, energy import, and the demand response program, and C_{Demand} is the demand charge. The costs are defined as

$$C^i_{CHP}=a\times\left(P^i_{CHP}\right)^2+b\times P^i_{CHP}+c\times\left(H^i_{CHP}\right)^2+d\times H^i_{CHP}+e\times P^i_{CHP}\times H^i_{CHP}+f \tag{2}$$

$$C^i_{import}=\left(D^i-P^i_{CHP}-P^i_{PV}-P^i_{BESS}\right)\times \text{Price}^i \tag{3}$$

$$C^i_{DR}=-\frac{1}{\beta}\left(D^i_0-D^i\right)^2+\frac{D^i_0-\alpha}{\beta}(D^i_0-D^i) \tag{4}$$

$$C_{Demand}=D_{max}\times \text{DemandPrice} \tag{5}$$

where $P^i_{CHP}, P^i_{PV}, P^i_{BESS}$ are the power outputs of the CHP sources, PV, and ESS at the i^{th} time step, respectively; H^i_{CHP} is the heat output of the CHP at the i^{th} time step, and D^i is the dispatched demand at the i^{th} time step. $a, b, c, \ldots, f$ are parameters associated with the cost characteristics of the CHP system and are specified by the user. $Price^i$ is the electricity price at the i^{th} time step, and $DemandPrice$ is the price per kW of peak demand. α, β are coefficients associated with the elasticity of the load, defined as

$$D^i=\alpha+\beta\times P^i_{price} \tag{6}$$

Constraints include the maximum PV output, which comes from the PV forecast results, the maximum CHP output and ramping rate, the power and State of Charge (SoC) of the BESS, and the peak demand limitation.

In the islanded mode, the objective shifts to being able to serve as much load as possible, which mean the minimum of

$$-\sum_{t=1}^{T}D^i \tag{7}$$

Most of the constraints in the grid-connected mode, including the maximum PV and CHP output, CHP ramping rate, and the power and State of Charge (SoC) of the BESS still apply. Besides, some constraints unique to the islanded operation are

1) Power balance constraint

$$P^i_{BESS}+P^i_{PV}+P^i_{CHP}=D^i \tag{8}$$

2) Load dispatch constraints

$$D^i=a^i_1D^i_1+a^i_2D^i_2+\ldots+a^i_kD^i_k \tag{9}$$

where $a^i_1, a^i_2, \ldots, a^i_k$ are binary variables representing the on-off statuses of each controllable load.

C. ACTIVE POWER CONTROL COORDINATION

After the generation plan is optimized by the energy management function, the active power control coordination function generates the real-time setpoints for the sources, loads, and the PCS converter. The active power control function in source local controllers (LCs), load shedding and restoration in load LCs, and the active power and reactive power control in the PCS converter LC will carry out the setpoints.

The system operator may need to override the dispatch command provided by the energy management function. The

active power control coordination function also calculates the maximum or minimum power capability that the F-CHP system has. In addition, depending on the grid frequency, the F-CHP system may help to inject or absorb additional active power to participate in the system's primary frequency control. The overall data flow of this function is shown in Fig. 5.

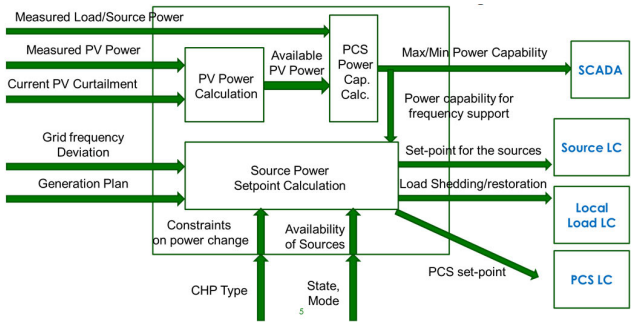


FIGURE 5. The overall data flow of the active power control coordination function.

D. DATA LOGGING

The data logging function is used to record the system operation conditions and status, such as the grid voltage and frequency, output power of different equipment, LV dc bus voltage, CHP turbine speed, BESS SoC, load power, etc., for later analysis or debugging.

E. PROTECTION COORDINATION

Depending on grid-connected or islanded operation modes, the system response after an ac-side short circuit fault may be different. In the grid-connected mode, the fault current is supplied by the ac grid, and the PCS will try to ride through the fault; while in the islanded mode, PCS supplies the fault current (with current limit) with reduced voltage. The protection coordination function monitors the state of the F-CHP system and gives updates to the protection settings of the relays to ensure the safe operation of the system.

In addition, during the fault ride-through or F-CHP system internal faults, the LV dc bus voltage may rise or drop rapidly due to the power imbalance between the generation and consumption. The protection coordination function will trigger switches as response to the load shedding.

F. THE STATE MACHINE

The state machine of the F-CHP central controller is shown in Fig. 6. It starts with the off state and goes to the ready-to-run state when the system is enabled. When starting up the system, if the ac grid is available, the system will start to the grid-connected mode. During the startup period, the PCS converter starts first to establish the LV dc bus voltage followed by the local sources and BESS. The loads will be started following the sources. When the ac grid is unavailable, the system starts to the islanded mode. The local sources and BESS are started first regulating the LV dc bus to the nominal voltage, and then the local sources will be started followed by the loads.

In the grid-connected mode, the PCS converter controls the LV dc bus voltage, and the ac side operates as a grid-following inverter. The CHP sources and BESS operate as current sources, following the power generation command from the central controller. However, during transients, such as mode transition between grid-connected mode and islanded mode or ac grid side LVRT, the power provided by the PCS may be limited and the LV dc bus voltage cannot be maintained within its nominal range. On the other hand, the turbine-based sources are slow in power regulation, and the PV panels are fast in terms of response speed, but power reservation is needed for transient support, which reduces the benefits. Because of its fast response, the BESS is designed to operate as a voltage source when the LV dc bus voltage is below a threshold value V_{th1} or higher than the other threshold value V_{th2}. To avoid conflicts between the PCS converter and BESS, a power-voltage droop curve as shown in Fig. 7 is adopted for the BESS, in which 1 p.u. refers to the rated power of the BESS.

When the ac grid is suddenly lost, once the PCS converter identifies the islanding it stops operating and gives up the role of LV dc bus voltage control. The central controller will also receive the islanding information, and it converts its mode from the grid-connected mode to the islanded mode. A command of controlling the LV dc bus voltage from the central controller will be sent to the BESS, and after receiving that command, the BESS will start to regulate the LV dc bus voltage without the droop curve shown in Fig. 7. Both the communication and mode transition take time. Therefore, during this period, the LV dc bus voltage could be close to either V_{min} or V_{max} shown in Fig. 7. The transition process of planned islanding is the same.

In the islanded mode, the BESS controls the LV dc bus voltage, and the other sources control their power output following the power generation command from the central controller, which balances the generation and load. The PCS converter can operate as a voltage source, controlling the ac voltage and frequency, to support the external ac loads. When the grid comes back, the BESS switches to the voltage control mode with the droop curve shown in Fig. 7 and the PCS converter starts operating and regulates the LV dc bus voltage.

It should be noted that the BESS and PV are not necessarily in the system. If the system does not have them, other sources can rake their roles. However, the power regulating speed of other sources may be slower than that of the BESS, and in this case, some energy buffer, such as capacitors, or load shedding/braking is needed to maintain the voltage during the transient.

All the active states (excluding the off state) can go to the fault state if any fault in the system happens, and the fault state can only go to the ready-to-run state. Therefore, if any

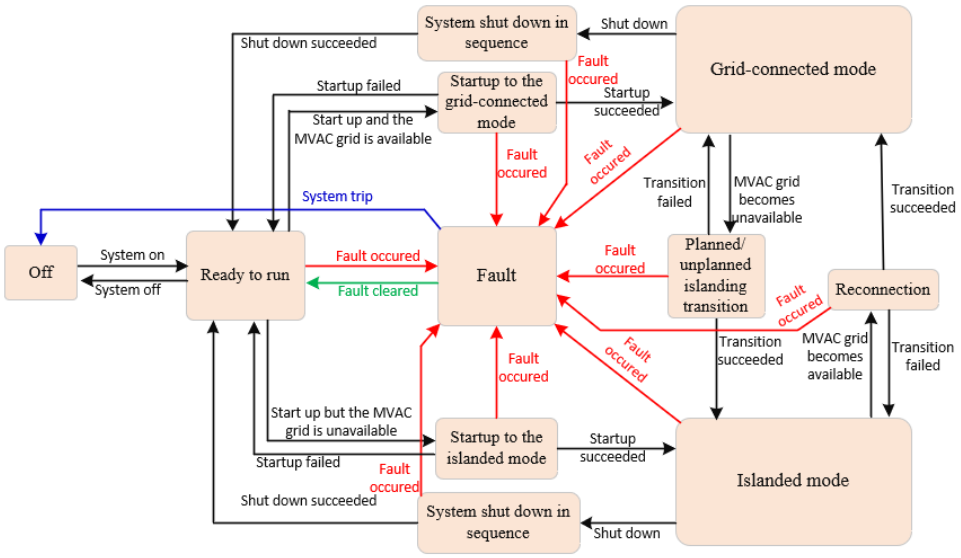


FIGURE 6. The state machine structure of the central controller.

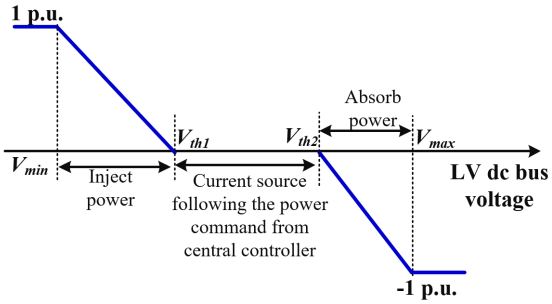


FIGURE 7. The operation mode and output power curve of the BESS in the grid-connected mode.

fault happens, the system must be restarted after the fault has been cleared.

IV. THE 13.8 kV/ 1 MW PCS CONVERTER DESIGN CONSIDERING GRID REQUIREMENTS

This section presents the impact of grid requirements on the converter design. The design requirements are first discussed, followed by the design comparison between without and with considering the grid requirements.

A. DESIGN REQUIREMENTS FOR THE PCS CONVERTER

The PCS converter plays a critical role in the grid support and grid services provided by the F-CHP system. To enhance the PCS's grid support functions, the converter design needs to consider the grid requirements. The converter design requirements are summarized in Table 1. The converter power rating is selected to be 1 MW, considering the parallel connection of multiple converters to achieve a higher power rating. The LV dc bus voltage is selected at 850 V, to support fuel cells, 480 V microturbine, 60 Hz CHP source,

TABLE 1. The converter design requirements.

Parameter	Value
Power rating	1 MW
LV side dc	850 V dc (±5%)
MV side voltage	13.8 V ac (-12% ~ +10%)
Power factor	Four quadrant operation
TRD of the MV ac current	<5%
Efficiency	98%
Maximum ambient temperature	35ºC
Cooling	Forced air or liquid
Ac side control bandwidth	Voltage control bandwidth >300 Hz Current control bandwidth > 1 kHz
Other requirements	1) Voltage ride through, frequency ride through, frequency and voltage support required in IEEE Std 1547 2) Grid faults 3) Lightning surge 4) Grid-connected mode and islanded mode operation and seamless transition 5) Unbalance support

and 480 V 4-wire local grids. The commonly used 13.8 kV ac grid in the United States is selected as the ac nominal voltage.

The PCS converter needs to operate in four quadrants. The ac grid side current total demand distortion (TDD) is required to be less than 5%, meeting the requirement in IEEE Std. 1547-2018 [37]. 98% of converter efficiency is required; the maximum ambient temperature is 35 °C for indoor application; and forced air or liquid cooling can be used. The ac side voltage (in the islanded mode) and current control bandwidth are required to be 300 Hz and 1 kHz, respectively, to enable more system-level benefits, such as active power filtering and stability. In addition, the converter design needs to consider grid requirements, including voltage ride-through,

frequency ride-through, and voltage and frequency supports, in IEEE Std. 1547-2018. Other grid conditions include grid faults, lightning surges, and unbalance.

B. THE BASELINE DESIGN

The baseline design is first conducted without considering grid requirements. the grid voltage is assumed to be in its normal operation range, 13.8kV (-12% $\sim$ +10%), but the BIL requirement is still considered for the ac side hardware design. The load change and mode transitions are also not considered.

1) THE DC/DC STAGE

a: DEVICE AND DEVICE COOLING

GE17042CCA3 1.7 kV/425 A SiC MOSFET half-bridge module is used for the LV side. For the MV side, two Wolfspeed 3rd-generation of 10 kV/300 mΩ (20 A) discrete SiC MOSFET dies in parallel are used, forming a 10 kV/40 A SiC MOSFET half-bridge power module. Both devices are sized based on the maximum current stress and efficiency requirement, considering 99% for the dc/dc stage, with the desired junction temperature of 100 °C and 75 °C for the LV and MV side devices respectively, and 10 kHz switching frequency. The 10 kV device's loss data is scaled up from the curve tracer and DPT results of the discrete device, and the power module's package and thermal resistance are scaled from values of the existing 10 kV SiC MOSFET power module [51]. The total device loss is estimated to be 1.29 kW, and the efficiency of the dc/dc stage, excluding the transformer, is 99.23%.

Water cooling is utilized for both the LV and MV side devices. Two ATS-CP-1004 cold plates are used to accommodate the full bridge at the LV side and the MV side, respectively, with a coolant flow rate of 1 GPM.

b: DC-LINK CAPACITOR

The dc-link capacitor in the baseline is designed considering the $\pm$5% voltage ripple. The required capacitance is 138 μF, and film capacitors are used considering their high reliability and current ripple capability.

c: TRANSFORMER DESIGN

The transformer design parameters are summarized in Table 2. Its magnetizing and leakage inductances are selected with the consideration of dc bias current tolerance and the impact on efficiency, as well as phase shift margin for control. To achieve light load dc/dc stage efficiency greater than 98.5% and transformer dc saturation current higher than 25 A, the magnetizing inductance is selected to be 1.5 mH. The leakage inductance is designed to be 35 uH, to achieve a full load efficiency higher than 99.2% and keep full power phase shift no less than 20% of the half switching cycle so that abundant control resolution for the entire output range can be realized.

TABLE 2. Transformer design summary.

Parameters	Values
Core	VAC W160, 6 sets in parallel
Flux density	0.655 T
Magnetic gap	0.1 mm*2
Core loss	237 W
Current density	2.6 A/mm^2
Window utilization	0.3
Primary winding	7 turns, 1 layer
	Litz wire 16.8 mm*7.83 mm, 6911 strand
Secondary winding	56 turns, 2 layers
	Litz wire, 4.6 mm*3.6 mm, 868 strand
Winding loss	142 W
Fin height	8 cm
Temperature rise	67 °C (Ansys/Icepak)
Efficiency	99.77%
Volume	12 L
Weight	23 kg

To minimize the size of the transformer, FR3 natural ester oil, which has a much higher insulation capability than air, is considered as the insulation material for the transformer. Partial discharge (PD) tests are conducted, and >5.5 kV/mm PD free is achieved in the lab condition, and 5 kV/mm is considered in the insulation design for long-term operation. As a result, a 3 mm oil gap is required considering the maximum voltage stress, which is the total MV dc link voltage, i.e., 14 kV.

Because of the mismatch among components (such as device switching delay, $R_{ds,on}$ difference, etc.), a dc bias current of higher than 10% of the rated current, can be induced considering the worst condition. To avoid the transformer saturation or overdesign of the maximum flux density, a closed-loop dc bias current control is proposed based on the second-order harmonic current detected by utilizing the non-linearity of ferrite sheet saturation [52]. With this control, the transformer only needs to tolerate a dc bias current of 1% of the rated winding current, which is of the detection accuracy of the control circuit.

The transformer's loss mainly consists of the core loss and winding loss. The nanocrystalline core is used because of its low core loss density, and the core loss is estimated to be 237 W using the improved Generalized Steinmetz Equation (iGSE) method. The magnetic gap is small compared to the distance between the winding wire and the gap, so the gap loss is neglected. Litz wire is used for windings to minimize the skin effect, and the proximity effect is considered by the ac resistance factor. The total winding loss is estimated to be 142 W.

With the loss estimated, the transformer thermal design is conducted. The whole transformer is fully enclosed in an aluminum case with fins on the outside surface for heat dissipation with natural air cooling. With Ansys/Icepak, the temperature rise is estimated to be 67 °C, which results in a maximum temperature of 102 °C with the maximum ambient temperature.

The dc/dc stage baseline design results are summarized in Table 3.

2) THE DC/AC STAGE

a: DEVICE AND DEVICE COOLING

The switching frequency of the dc/ac stage is determined at 10 kHz to achieve the control bandwidth requirement. The 10 kV SiC MOSFET is also scaled up based on the Wolfspeed 3rd-generation of 10 kV/300 mΩ (20 A) discrete die. The total loss of each device position is 370 W, of which 190 W is the switching loss and 180 W is the conduction loss.

Water cooling is adopted, and the ATS-CP-1004 cold plate is selected to accommodate two half-bridge modules of each H-bridge. With a coolant flow rate of 1 GPM, the temperature rise between the outlet coolant and the inlet coolant is around 6 °C.

b: DC-LINK CAPACITOR

The dc-link voltage is selected at 6.3 kV, considering the maximum ac grid voltage (13.8 kV +10%). The MV dc-link capacitor is selected based on the voltage rating, voltage ripple, current rating, as well as temperature rise. Due to the single-phase topology, the main voltage variation on the MV dc-link is the 2nd-order ripple, and it is limited to ±5%, considering the safe operating voltage of the 10 kV device and the ac-side power quality. As a result, the required capacitance is 114 μF, and four 2 kV/440 μF TDK film capacitors B25620B1447K983 are in series connection. The capacitor temperature rise is estimated to be 3.1 °C, based on the power loss and thermal resistance.

c: AC FILTER INDUCTOR

The ac filter inductor is sized based on the MV ac side's current harmonic requirements. Because of the high switching frequency and multi-level topology, only 4.4 mH (0.009 p.u.) inductance is required. The inductor is designed with 2 sets of AMCC1000 amorphous cores. The core loss is estimated by the iGSE method with the current waveform from MATLAB simulation [53]. Because of the direct interface to the 13.8 kV grid, besides the 14 kV steady-state operation voltage stress, the inductor design has to consider grid insulation requirements, including 31 kV low-frequency short-term insulation capability, as well as the 95 kV lightning surge in IEC 60071-1 [54]. Epoxy-based encapsulation design is adopted, and the insulation distance is selected to achieve a dielectric strength of 6 kV/mm considering the reliability of long-term operation.

Then, the thermal simulation was conducted through Ansys/Icepak. The hot spot is located in the winding, and the temperature rise is 84 °C [55].

d: AC-SIDE COMPONENTS

Since the PCS converter may start from the MV ac grid side, a pre-charge circuit is needed to avoid a large inrush current during the start-up. The widely used pre-charge resistor plus bypass relay solution is used, and the pre-charge resistor is selected at 10 kΩ, achieving a pre-charge period of 10 seconds and an average power rating of 281 W. The resistor TAP600K10KE, which has a power rating of 600 W is selected. It has a continuous dielectric strength of 6 kV RMS, and a short-term (1 min) of 12 kV RMS, so it can meet the PCS converter requirement. A double pole single throw relay, named RL 38-h, is selected. It has an insulating voltage of 10 kV ac, and a current rating of 30 A per pole. To meet the current rating, the two poles can be connected in parallel, then a total of 60 A can be achieved.

Arresters are installed at the MV ac side terminals to protect the converter from lightning or switching transient surges. The arrester selection is based on the system voltage level. Based on the selection guide in [56], the SIEMENS arrester 3EK7 120-3AC4 is selected.

Moreover, the ac grid-side fuse and mechanical switches are selected based on the voltage and current rating. The dc/ac stage baseline design results are summarized in Table 4.

TABLE 3. Baseline design summary of the DC/DC stage.

	Baseline
Device Selection	• LV side: 1.7 kV/425 A SiC MOSFET scaled from GE17042CCA3 die; Total size: 1.9 L; weight: 3.6 kg • MV side: 10 kV/40 A SiC MOSFET scaled from wolfspeed 10 kV/300 mΩ die; Total size: 1.9 L; weight: 3.6 kg
Cooling	• Liquid cooling • Cold plate: ATS-CP-1004 for each full bridge with • Total size: 6.7 L, weight: 13.2 kg
MV MF Transformer Parameter	• Voltage: 850 V/6.7 kV • Current: 230 A / 29 A • Leakage: 35 µH • Magnetizing Inductance:1.5 mH • Insulation voltage: 13.4 kV dc with high-frequency and high dv/dt • Total size: 70 L; weight: 138 kg
LVDC Capacitor	• 900 V/138 µF film capacitor • Size: 3.4 L, Weight: 4.2 kg

C. DESIGN CONSIDERING SYSTEM OR GRID REQUIREMENTS

1) THE DC/DC STAGE

a: THE DAB TRANSFORMER CONSIDERING THE HIGHER INSULATION REQUIREMENTS

According to grid requirements, the MFT should reach 31 kV 1-minute insulation and 95 kV BIL. As a result, a 6 mm oil gap is required by the 31 kV 1-minute insulation, and an 8.5 mm oil gap is required by 95 kV BIL considering a time factor of 0.45. Thus, the minimal insulation clearance is designed to be 8.5 mm, and the size and weight of the transformer become 16 L and 23.5 kg, respectively.

b: LV DC CAPACITOR CONSIDERING SYSTEM TRANSIENTS

The LV dc link capacitors have been designed to maintain the LV dc bus voltage during sudden load or source power changes on the dc or ac side. In the grid-connected mode, the worst case is that the PCS converter requires a sudden power change from 0 to 100% of its power rating. Assuming the dc/dc converter's control loop has a delay of 5 switching

TABLE 4. Baseline design summary of the dc/ac stage.

Components	Baseline
Device	• Efficiency: 99%; • 10 kV / 60 A SiC MOSFET; • Junction temperature under normal operation: 150 ºC; • Size: 2.34 L; weight: 2.4 kg;
Cooling	• Water cooling; • Inlet coolant temperature: ≤76 ºC; • Flow rate: 1 GPM; • Cold plate size: 3.34 L; weight: 6.6 kg;
Dc-link Capacitor	• Dc-link voltage: 6.3 kV (±5%); • Dc-link capacitance: 114 uF; • Capacitor: TDK B25620B1447K983(4 in series); • Size: 68.5 L; weight: 68.4 kg;
Inductor	• Inductance: 4.4 mH; • Current: 44 Arms / 63 Apk; • Size: 20.1 L; weight: 69 kg;
Arrester	• none
Pre-charge circuit	• Resistor: TAP600K10KE; relay: RL 38-h; • Size: 4.1 L; weight: 7.5 kg;
Fuse	• Littelfuse 15NLE50E; • Size: 8.3 L; weight: 6 kg;
Switch	• ABB VSC12; • Size: 32 L; weight: 20 kg;

cycles, the LV dc capacitance needs to be 3.7 mF to limit the voltage change below 150 V, with which the system can still operate in the short term. In the islanded mode, the battery controls the LV dc voltage, while the PCS ac side voltage could still have a sudden voltage drop when a sudden power change occurs at the external ac load, depending on the impedance between the PCS converter and the battery. Assuming a long cable of 500 m, with the capability of the rated current, between the PCS and the battery, the impedance is estimated to be 90 μH inductance and 0.3 Ω resistance. The LV dc capacitance should be at least 5.1 mF to maintain a voltage variation of less than 150 V. Therefore, 36 TDK B25655P4607J011 450 V/600 μF film capacitors are connected as 2 series 18 parallel, forming a 900 V/5.4 mF capacitor bank. The total capacitor size is 18 L, and the weight becomes 28.8 kg.

2) THE DC/AC STAGE

a: LOW VOLTAGE RIDE THROUGH

During the transient of grid voltage drop, the converter's duty cycle cannot immediately change, and so a large voltage difference occurs between the two terminals of the ac filter inductor. Due to the small filter inductor, a large inrush current could be induced. Besides, because of the inrush current, dc-link overvoltage could also occur.

Increasing the inductance can reduce the inrush current, but the size and cost of the inductor will also increase. Therefore, a PWM mask approach is proposed to temporarily turn off the PWM waveforms when the inrush current is larger than a preset value [57]. When the devices are all turned off, the current flows through the body diode of the SiC MOSFETs, and the polarity of the voltage drop on the inductor will be reversed so that the current can be reduced. When the current is lower than a preset release value, the PWMs are released with the current duty cycle.

Although the inrush current can be effectively limited by the PWM mask approach, when the grid voltage is low, the power delivery is also low due to the current limit. As a result, the power balance needs to be maintained by another power source or energy storage, such as a battery or capacitor (for the short term).

b: HIGH VOLTAGE RIDE THROUGH

The temporary high voltage could also occur in the grid, and in IEEE Std. 1547-2018 it is required to ride through 1.2 p.u. grid voltage. The dc-link voltage reference is increased from 6.3 kV to 6.7 kV, considering slight modulation saturation and the maximum voltage stress (7 kV) on the 10 kV device. Meanwhile, the capacitance is changed to 99 μF to limit the 2^{nd}-order voltage ripple within ±5%.

c: GRID FAULTS

During a grid fault, the temporary overvoltage could be more than 1.2 p.u, depending on the system's grounding configuration and wire configuration. For the three-phase four-wire system, the overvoltage could be between 1.25 p.u. and 1.5 p.u. [58]. Riding through the overvoltage of higher than 1.2 p.u. is not required in the standard and riding though 1.5 p.u. overvoltage requires a third cascaded power unit, which reduces the dc-link voltage utilization in normal operation and increases the converter cost. Therefore, the converter is designed to temporarily stop operation once the voltage is higher than 1.2 p.u. and restart within 3 seconds when the grid voltage is lower than 1.2 p.u.

When the grid voltage is higher than 1.2 p.u., modulation saturation occurs, and the current is out of control. As a result, inrush current and dc-link overvoltage happen. Therefore, the converter has to stop switching to avoid damage to the 10 kV SiC devices. The dc-link capacitors and the dc-link busbars can be designed to have a sufficient voltage rating corresponding to the voltage with the temporary dc-link overvoltage. To avoid a higher dc-link overvoltage caused by the charge of the ac filter inductor and realize quick restart when the grid voltage drops below 1.2 p.u., a dynamic braking circuit (DBC) is adopted on the dc-link. The DBC consists of a discharge resistor bank and semiconductor switches, which could be Si devices. When the dc-link voltage is higher than 8.2 kV, the DBC operates until the dc-link voltage is below 8 kV. When the grid voltage is lower than 1.2 p.u., the DBC operates again to quickly discharge the dc-link voltage to be below 7 kV so that the converter can restart with a safe dc-link voltage. Three IXYS 4.7 kV/2 A Si MOSFETs (IXTL2N470) are connected in series as the braking switch, considering their lower cost and small current rating. Two Vishay 5 kΩ thick film chassis mount resistors (LPS0800L5001KB) are selected to be connected in series. Each resistor has a voltage rating of 5 kV dc, and a short-term energy rating of 1.5 kJ

TABLE 5. Summary of the grid requirements impact on the converter design.

Grid/design requirements	Requirement details	Impact on converter design
Voltage ride through	▪The converter needs to ride through the low voltage range of [0, 0.88 p.u.], and ride through the high voltage range of [1.1 p.u., 1.2 p.u.]	▪Inrush current, which can be effectively limited by the PWM mask function, e.g., 2 p.u. ▪The dc-link voltage needs to increase to 6.67 kV to accommodate the 1.2 p.u. grid voltage with an acceptable PWM modulation saturation ▪Power control coordination between the dc/dc stage and the dc/ac stage and between the PCS converter and other resources on the LV dc bus
Grid faults	▪Follow the voltage ride-through requirements if the overvoltage is lower than 1.2 p.u. ▪If the fault causes overvoltage of more than 1.2 p.u., the converter can temporarily stop working, but when the grid voltage is recovered, the converter needs to restart within 3 s	▪Inrush current, up to 5 p.u. ▪Dc-link overvoltage, up to 9.3 kV ▪Extra braking circuit, to reduce the Dc-link overvoltage to 8 kV during the fault period, and to quickly discharge the Dc-link after the fault is clear so that the converter can realize restart within 1 s
Frequency ride through	▪The continuous operation frequency range is [58.8 Hz, 61.2 Hz] ▪Ride through the low-frequency range of [50 Hz, 58.8 Hz] and the high-frequency range of [61.2 Hz, 66 Hz] with a period of 299 s	▪No inrush and large dc-link overvoltage ▪Need larger dc-link capacitance to limit the dc-link voltage ripple when operating at the lowest fundamental frequency
Grid voltage angle change	▪Ride through 20 electrical degrees of positive-sequence phase angle change within a sub-cycle-to-cycle time frame and up to 60 electrical degrees of individual phase angle change	▪Inrush current exists due to the voltage suddenly changes, but can be effectively limited by the PWM mask function ▪Dc-link voltage variation, but no need for hardware change
Lightning surge	▪Avoid damage or trip when a lightning surge occurs	▪Inrush current, up to 5 p.u. ▪Dc-link overvoltage, which is not too large because of the short period ▪Converter internal component insulation needs to consider the potential of the neutral point during the lightning transient

(@ 0.3 s), which can meet both the insulation and energy dissipation requirements.

d: FREQUENCY RIDE THROUGH AND VOLTAGE ANGLE VARIATION

In IEEE Std. 1547-2018, it is required that, for a 60 Hz system, the DER needs to ride through low frequency down to 50 Hz and high frequency up to 66 Hz for 299 seconds. Besides, 20 electrical degrees of positive-sequence phase angle change within a sub-cycle-to-cycle time frame and up to 60 electrical degrees of individual phase angle change are required to ride through.

Based on the Simulink-based simulation results, the frequency variation has little impact on the converter operation because of the low rate of change of frequency (ROCOF) defined in the standard. However, the 2nd-order voltage ripple on the dc-link becomes larger when the frequency decreases. Therefore, the dc-link capacitance needs to be increased to 119 μF to limit the 2nd-order voltage ripple within $\pm$5%. In addition, the voltage phase angle's sudden change leads to the sudden change of the voltage between the ac filter inductor, which results in an inrush current. This issue can also be solved with the PWM mask approach [57].

e: LIGHTNING SURGE

Although the arrester clamps the lightning surge to a certain voltage (37 kV @ 10 kA), the clamped voltage is still much higher than the overall dc-link voltage (13.4 kV). Then, the large voltage difference between the ac filter inductor's two terminals results in an inrush current [59]. Besides, the PWM mask function cannot effectively limit the inrush current. Because of the short period, the dc-link overvoltage is not severe. However, the potential of the converter components to the ground could be high during the surge transient. This is dependent on the neutral-to-ground impedance, which shares the voltage difference with the ac filter inductor.

Increasing the inductance can decrease the inrush current but also increase the inductor size and cost. Designing the inductor with high inrush current capability and sizing the SiC MOSFETs with higher inrush current is the alternative, which can result in a smaller inductor size.

f: IMPACT ON HARDWARE DESIGN

The impact of grid requirements on the converter design is summarized in Table 5. Starting from the baseline design, the dc-link voltage changes from 6.3 kV to 6.67 kV after considering the high voltage ride through. The capacitance, which is sized based on $\pm$5% 2nd-order voltage ripple, changes from 114 μF to 99 μF after considering the high voltage ride through and then increases to 119 μF after considering the frequency ride through. However, the film capacitor products are not seamless in terms of voltage rating and capacitance value. The capacitor selected in the baseline design is still used after considering grid requirements, however, the voltage and capacitance margin is reduced.

The inrush current needs to be considered in the inductor design to make sure it does not saturate. In cases of LVRT, HVRT, faults, grid voltage angle change, and lightning, a larger filter inductance leads to a smaller inrush current. Therefore, the inductor design has two choices:

- Same inductance with large inrush current capability.
- Larger inductance with small inrush current capability.

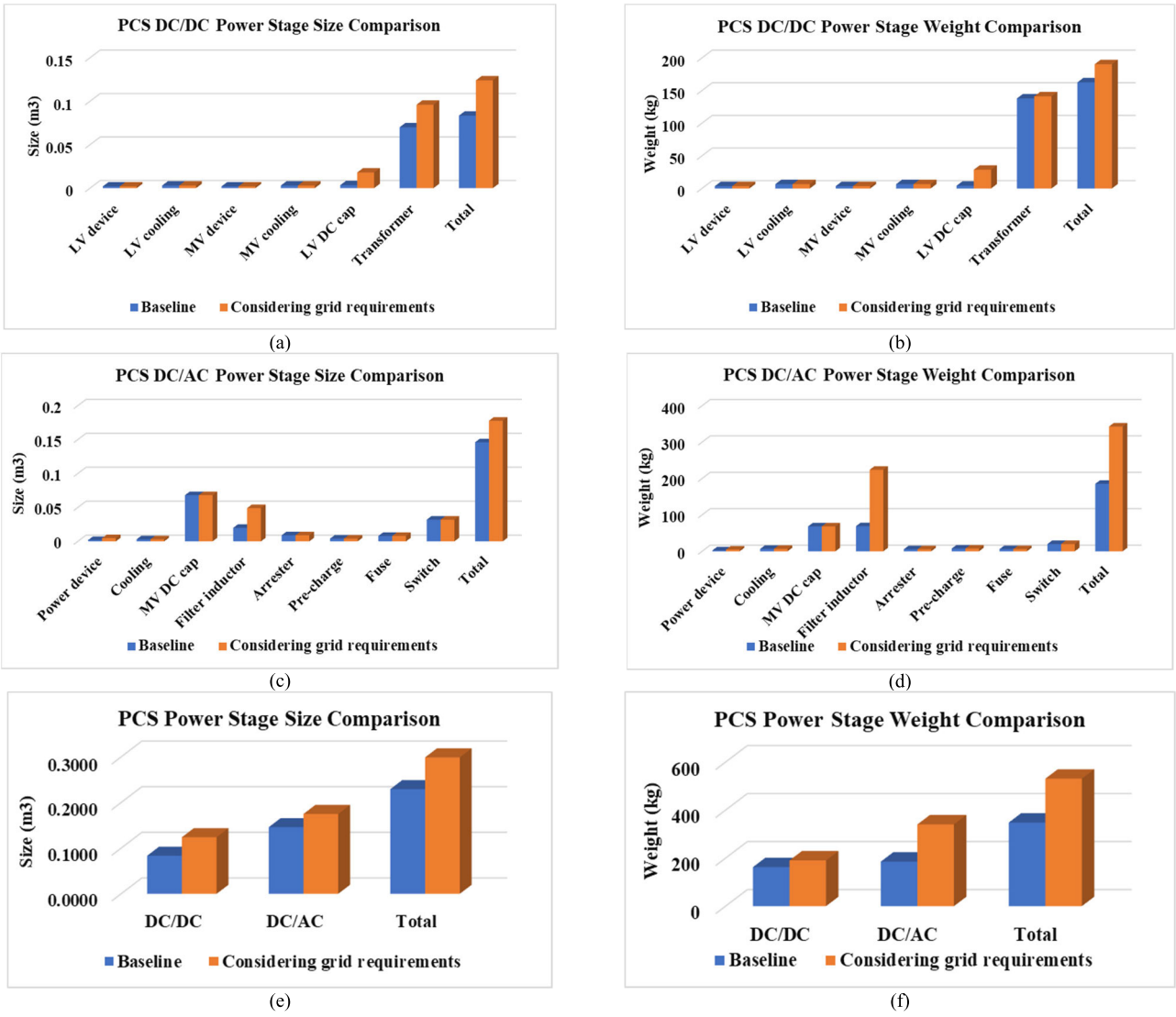


FIGURE 8. Comparison of (a) the dc/dc stage size, (b) the dc/dc stage weight, (c) the dc/ac stage size, (d) the dc/ac stage weight, (e) the PCS size, and (f) the PCS weight between the baseline design and the design considering grid requirements.

Since changing the inductance does not change the grid voltage variation and time duration, based on the required inductor core size, a larger inductance leads to a larger core, and thus a larger inductor size. Therefore, the inductance will not be changed, instead, the inrush current of the inductor will be designed up to the worst case, which is 5 p.u. The inductor's overall size and weight are around 16,410 cm^3 and 74.5 kg, respectively.

The inrush current also flows through the 10 kV SiC MOSFET, either the channel or the body diode. Assume the 10 kV SiC MOSFET can also achieve 3 times short period current capability through thermal and package design as the commercialized LV SiC devices. Then, to withstand the 5 p.u. inrush current, the device's current rating needs to be 1.67 p.u., i.e., 100 A, which means each device needs 5 dies in parallel. This increases the scaled half-bridge power module size and weight to 390 cm^3 and 0.4 kg, respectively.

D. DESIGN COMPARISON

The PCS dc/dc power stage size and weight comparison, the dc/ac power stage size and weight comparison, as well as the total power stage size and weight comparison between the baseline design and the design considering grid requirements, are shown in Fig. 8 (a), (b), (c), (d), (e), (f), respectively. The main impact on the dc/dc stage is the larger LV dc capacitor for transient voltage balancing and the higher insulation for the transformer, which results in a 49% size increase and a 17% weight increase.

For the dc/ac stage, grid requirements change the device, dc-link capacitor, as well as the ac filter inductor. Due to the limitation of available capacitor products, the capacitor size and weight change are not reflected, and the main size and weight change come from the ac filter. Compared to the baseline design, after considering grid requirements, the dc/ac power stage size and weight are increased by 22% and 85%, respectively.

After considering grid requirements, the total PCS converter size and weight are increased by 32% and 53% respectively.

V. THE FIRST 13.8 kV/ 100 KW PCS CONVERTER PROTOTYPE DESIGN AND DEVELOPMENTS

To verify the converter design, a 10 kV SiC MOSFET-based 13.8 kV/ 100 kW PCS converter prototype is designed and developed following the same design approaches of the 1 MW converter in Section IV. The subsystem hardware design and development, addressing different challenges, are discussed in this section.

A. LV POWER STAGE

The picture of the LV power stage is shown in Fig. 9. At the LV dc side, 1.7 kV/40 A SiC MOSFETs (C2M0080170P) from Cree are used, and each H-bridge uses one heat sink with forced-air cooling. The gate drive uses the same schematics as that for the MV devices and will be discussed later. Films capacitors are used as the dc-link capacitors and PCB-based busbar is used.

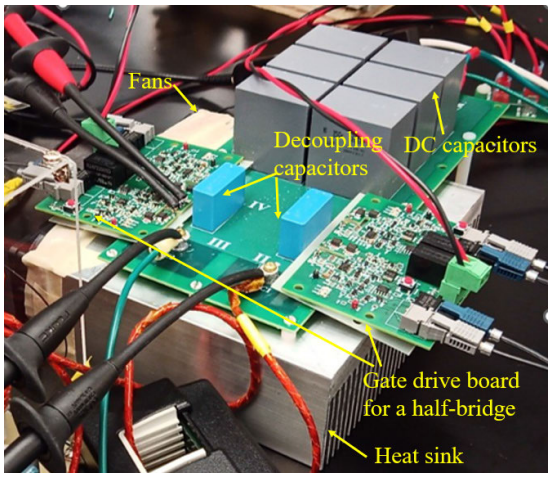


FIGURE 9. Picture of the LV power stage.

B. MV MF TRANSFORMER

The main structure of the MV MF transformer is shown in Fig. 10. To achieve high efficiency and power density, the nanocrystalline core is used in the transformer. The MV winding is encapsulated with silicone elastomer to achieve insulation capability up to 12 kV ac peak [60]. The MV winding is also coated with copper paint and the coating layer is grounded to provide shielding and confine the high electric field inside the dry-type insulation, which can avoid partial discharge in the outside air. The core-type structure is adopted so that the leakage inductance of 300 μH (LV side) for the dc/dc converter can be integrated.

C. GATE DRIVE

Increasing the gate drive turn-on voltage helps to reduce the conduction loss, but the saturation current in a short circuit

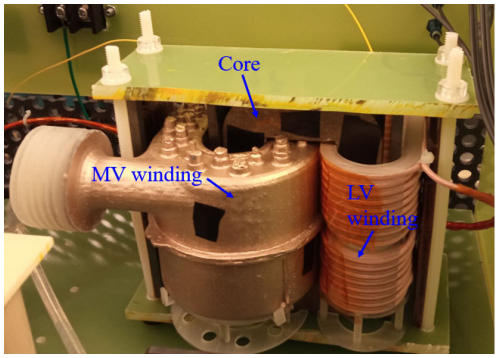


FIGURE 10. Photograph of the MV MF transformer.

is also high. As a tradeoff between them, the turn-on voltage for the 10 kV SiC MOSFET is determined at 15 V. Since this device features a high ratio of input capacitance to the miller capacitance, crosstalk is not a concern. To ensure a reliable turn-off, -5 V is selected as the turn-off voltage. In addition, the turn-on and turn-off gate resistances are selected to be 15 Ω and 3 Ω, respectively, to achieve a low switching loss and limit the average dv/dt to 50 V/ns.

The main function diagram of the gate driver is shown in Fig. 11. The signal transfer between the converter controller and each gate driver is based on fiber optic, considering the insulation requirement and high dv/dt. A status feedback circuitry is used to generate a short low voltage pulse on the rising and falling edge of the PWM signal, and the final feedback signal sent back to the converter controller is the combination of the short pulse and the fault signal, which consists of the under-voltage lockout (UVLO) and the desaturation protection. For desaturation protection, the fault signal will be latched. A protection reset unit is used to unlock the fault signal with 24 continuous PWM pulses if the fault disappears. The fault signal also controls the gate signal, masks the PWM signal, and also provides a soft turn-off.

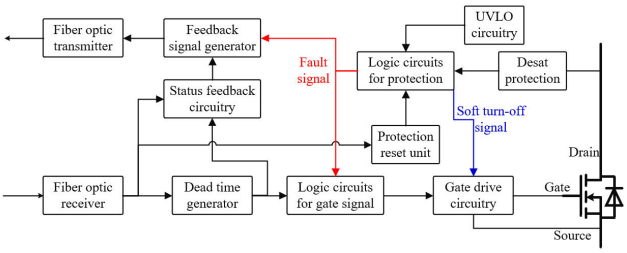


FIGURE 11. Function diagram of the designed 10 kV SiC MOSFET gate driver.

D. MV POWER STAGE

The Wolfspeed 3rd-generation of 10 kV/300 mΩ discrete SiC MOSFET is used. It has a non-isolated package with the die soldered on a copper plate, which is also the drain terminal and heat dissipation plate. The device losses are estimated with the previous DPT results in [20], and the device cooling is designed based on the loss estimation. As shown in Fig. 12,

four devices (a half-bridge in the dc/dc stage and a half-bridge in the dc/ac stage) are in one air duct with two fans, one on each side. The fans are supplied by the primary-side input dc voltage of the MV GDPS, therefore, the 100 mm distance between the fan and the power stage is designed to achieve the insulation capability. Because of the non-isolated device package, each device has its individual heatsink, which is isolated from other heatsinks. The heatsinks are floated from the air duct to increase the creepage distance, and the clearance distance between two adjacent heatsinks is around 20 mm. The maximum heat sink's temperature rise is estimated to be 38 °C with Ansys Icepak finite element method (FEM)-based simulation.

The four 10 kV SiC MOSFETs are mounted beneath the gate drive board, as shown in Fig. 12. In addition, a non-isolated dc/dc board is utilized for each device gate drive to convert the 24 V from the MV GDPS [24] to +15 V, +5 V, and −5 V. Also, 3.3 kV SiC Schottky diodes are used are the desaturation protection diodes, and they are mounted on another daughter board.

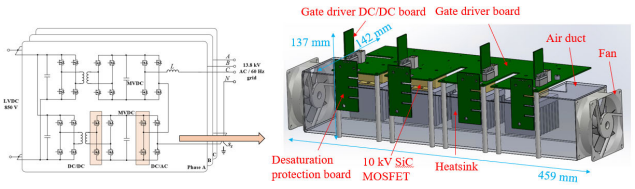


FIGURE 12. Device driving and cooling mechanical scheme.

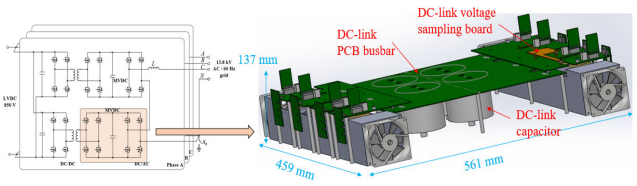


FIGURE 13. MV stage structure with PCB-based dc-link busbar.

Because of the low current rating, the PCB-based dc-link busbar is utilized. As shown in Fig. 13, four 2 kV/40 μF film capacitors are series connected by the PCB busbar, and it also connects with two gate drive boards. The dc-link voltage sampling board is located on one of the two gate drive boards, and it shares the MV GDPS for one of the low-side MOSFETs.

E. MV AC FILTER INDUCTOR

The MV ac filter inductor is designed considering the ac side power quality, the grid transients, and the grid insulation requirements [36]. As shown in Fig. 14, the winding is encapsulated with silicone elastomer TC-4605, and a surface shielding layer with copper is used to fully stress the high voltage on the insulation material to avoid partial discharge in the air gap between the core and the winding. The inductor passes 12 kV RMS partial discharge inception voltage (PDIV), 46 kV (>1 minute) dc hi-pot test, and the one-hour single-phase converter full rating test.

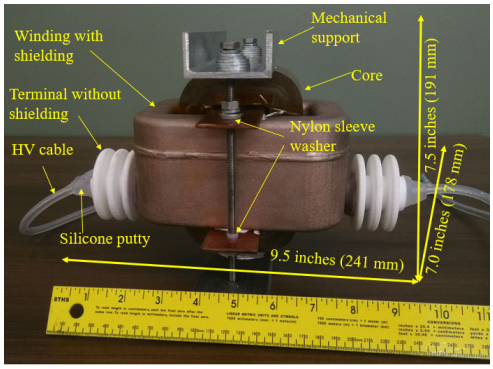


FIGURE 14. The MV ac filter inductor [36].

F. MV GDPS

The MV GDPS is designed based on the transformer discussed in [24]. However, the topology is changed from the primary-side regulated (PSR) flyback converter to the PSR Fly-buck converter, which is more robust to the common mode noise [61]. Because the feedback voltage in the PSR Fly-buck converter is the voltage on a capacitor, but in the PSR flyback converter the feedback voltage is the voltage of the switching node, which is much more sensitive to the common mode noise.

G. CONVERTER CONTROLLER

The main controller board for the converter includes two pairs of FPGA and DSP. Each pair of DSP and FPGA controls either the dc/dc or dc/ac stage. The DSP does the control and communicates with the F-CHP central controller, and the FPGA generates the PWM signals and interfaces with current and voltage sensors, which are based on voltage-to-frequency (VFC) converters. Fiber optics are used to do communication between controllers and the power stage. The detailed structure and assembled controller board are shown in Fig. 15. After assembly, the controller board is then mounted into a shielded controller box, with controller power supplies and line EMI filters, to suppress interferences from MV converters during operation.

H. THE CONVERTER MECHANICAL DESIGN

Because of the modularity of the converter, modular design is adopted in the prototype. As shown in Fig. 16, each power unit consists of one dc/dc stage and one dc/ac stage. The control signals are transferred with fiber optic, and the fiber optic connectors, auxiliary power supply connectors, and LV dc input terminals, are all located on the power unit's front panel, as shown in Fig. 17. The MV ac side output terminals are led out from the rear panel. Also, the airflow direction is from the rear panel to the front panel.

The three-phase converter prototype is shown in Fig. 18. The converter controller is mounted on the outside surface

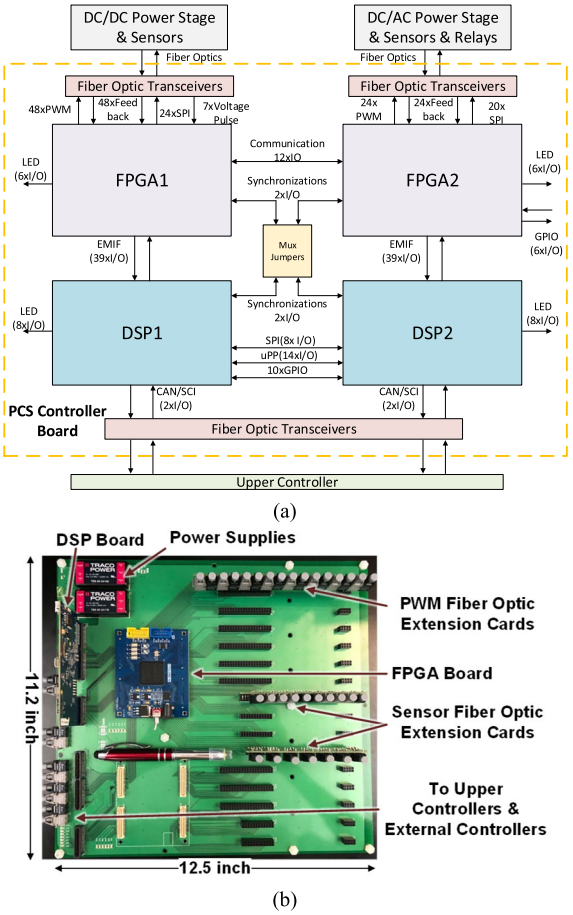


FIGURE 15. The (a) diagram and (b) picture of the PCS converter controller.

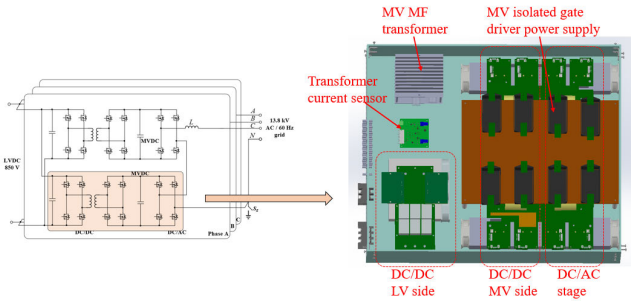


FIGURE 16. Structure of one power unit.

of the converter's side panel to minimize noise interference. Inside the converter cabinet, six power units are located vertically. The ac filter inductors, ac side voltage and current sampling boards, the ac/dc auxiliary power supply, and input and output connectors are all located on the bottom level in the cabinet.

VI. EXPERIMENTAL TESTS OF THE FIRST 13.8 KV/ 100 KW PCS CONVERTER PROTOTYPE

During the prototype development process, component tests, power unit tests, single-phase tests, and three-phase tests are

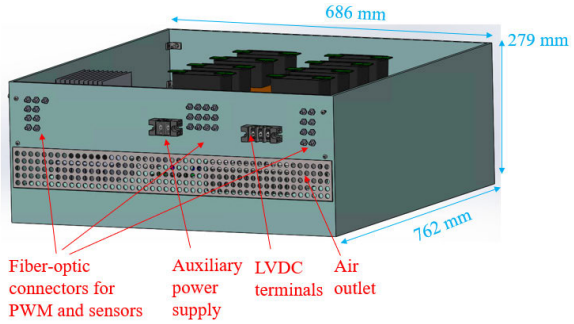


FIGURE 17. Front view of the power unit.

FIGURE 18. The three-phase converter prototype.

conducted in sequence. When all three single phases are fully tested, they are assembled into the three-phase converter prototype. In this section, the single-phase and three-phase converter tests are discussed.

A. SINGLE-PHASE FULL RATING TEST

The single-phase tests are conducted with the setup shown in Fig. 19, aiming at verifying the converter design and efficiency. The single-phase converter is supplied from the LV dc side, and the MV ac side is connected to a resistor bank through an 8 kV/120 V transformer.

The MV ac side PWM voltage, sinusoidal voltage, and current waveforms are shown in Fig. 20. Five-level voltage is achieved, and the rated voltage and current output are reached. The single-phase test is continuously conducted for more than 1 hour, to verify the thermal performance of magnetics. The surface temperature of the transformer and inductor core and windings are monitored with fiber optic temperature sensors. The temperature rise of the DAB transformer is measured to be 110 °C, and that of the MV ac filter inductor is measured to be 88 °C.

B. CONVERTER EFFICIENCY

The converter efficiency is calculated based on the input and output power measurement with the WT3000E power analyzer. The LV dc voltage is directly sampled by the power analyzer, and the current is measured with an external current sensor (LEM IT 400-S) because of the high current rating and easy connection. Due to the high voltage, the

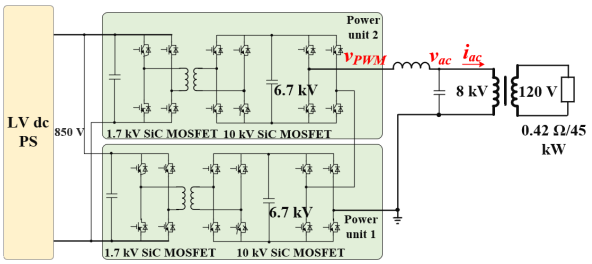


FIGURE 19. Test setup diagram for the single-phase test.

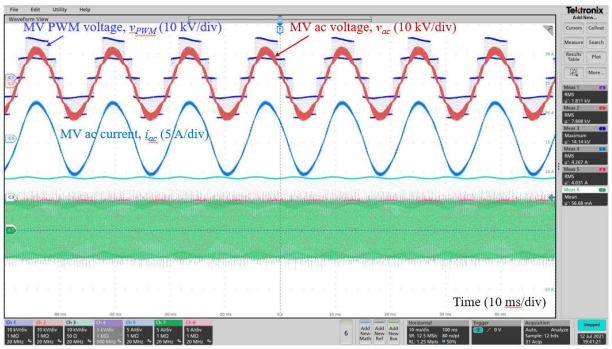


FIGURE 20. MV ac side waveforms of the single-phase test in the rated condition.

MV ac voltage is measured by the power analyzer through a resistor divider. The resistor divider ratio is calculated based on the resistance measurement with Tektronix Keithley 2100 digital multimeter, considering the input impedance of the power analyzer. Because of the high voltage and insulation requirement, the MV ac current is measured with an external current sensor (LEM IT 60-S) with a high insulation wire going through it.

As shown in Fig. 21, with 10 kHz switching frequency and conventional phase shift PWM modulation for the dc/ac stage, the converter peak efficiency is only around 93.3%, which is much lower than the design goal, i.e., 98% Three main reasons are found:

1) The used 10 kV SiC MOSFETs have a much higher switching loss than the DPT test conducted in [20].
2) The parasitic capacitance of the DAB transformer and the ac filter inductor introduces a lot of power losses.
3) The leakage flux of the DAB transformer also leads to power loss [60], [62], of which the modification is discussed in Section VII-C.

To improve efficiency, three approaches are adopted:

1) The switching frequency of the dc/ac stage is changed from 10 kHz to 3 kHz. To maintain the control bandwidth, the control frequency is changed from 10 kHz to 12 kHz, adopting the control approach used in [63].
2) A PWM modulation strategy is proposed to reduce the parasitic capacitance loss induced by the DAB transformer [30]. The main idea is to reduce the equivalent frequency of the dc-links so that the voltage frequencies on the DAB transformer parasitic capacitances are also reduced.
3) The inductor winding shielding is changed from solid grounding to grounding with a high impedance (1 MΩ). This also reduces the voltage frequency on the inductor parasitic capacitance. However, with high impedance grounding, the inductor shielding layer has some potential, and sufficient distance needs to be maintained between the inductor case and the surrounding parts.

With these approaches, the converter efficiency is significantly improved, with a peak efficiency of 96.4%, as shown in Fig. 21.

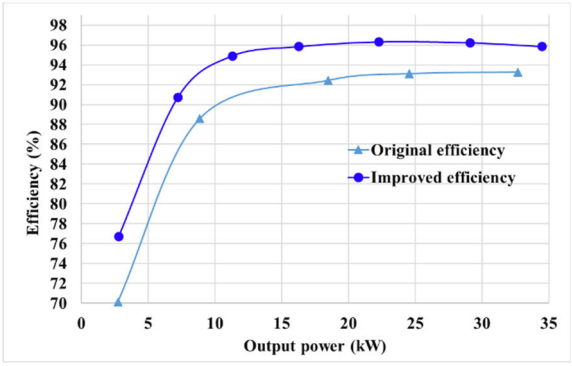


FIGURE 21. The single-phase converter efficiency.

C. THREE-PHASE FULL RATING TEST

With the three single-phase converters fully tested, the three-phase converter is assembled, and the setup shown in Fig. 22 is used for the three-phase test. The converter is still supplied with the LV dc power supply from the LV dc side, and the MV ac side is connected to three single-phase R-C loads with 250 Ω resistance and 1.25 μF capacitance.

The MV ac side voltage and current waveforms with the rated voltage and current output are shown in Fig. 23. In addition, through doing FFT for the ac voltage and current, the voltage and current TRD (also THD in the rated condition), considering up to 50th-order, is 2.72% and 0.79%, respectively. Also, the individual harmonic is also below the requirement in IEEE Std. 1547 and IEEE Std. 519.

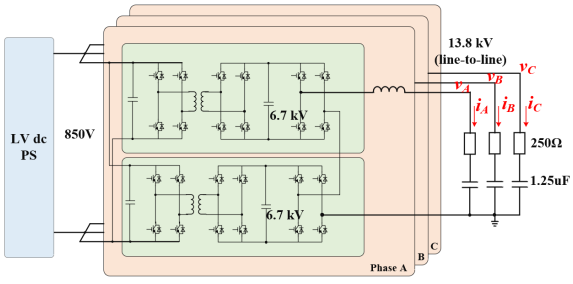


FIGURE 22. The test setup diagram of the three-phase test.

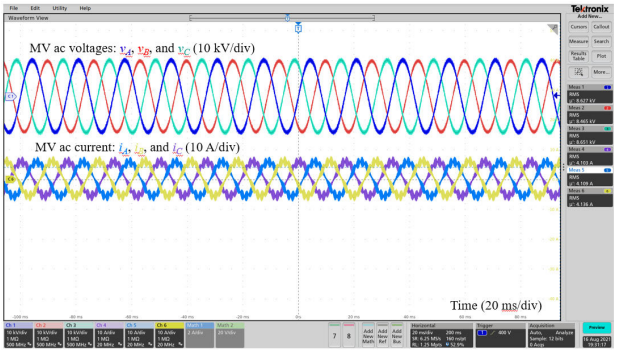


FIGURE 23. The MV ac side voltage and current waveforms in the three-phase test under the rated voltage and current conditions.

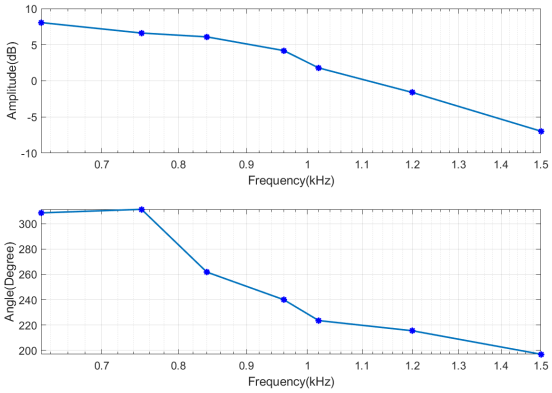


FIGURE 25. The ac current control bandwidth test results.

D. AC VOLTAGE AND CURRENT CONTROL BANDWITH

The ac side voltage and current control bandwidths are tested with frequency injection and sweep. A specific harmonic is injected into the d-axis voltage reference, and the d-axis voltage feedback is measured. By doing FFT analysis for the injected and feedback data arrays in a constant period, which is several fundamental cycles. The amplitude and phase angle of the injected and feedback signal under the injected frequency can be calculated, and the open-loop gain and angle difference can be obtained. More harmonic frequency can be repeated with the same process, and the open-loop gain and phase angle are drawn in Fig. 24. Based on the definition of the open-loop transfer function, the control bandwidth is the zero-crossing frequency of the gain, which is 300 Hz. The phase margin is around 59°. The same approach is used for the current control loop, and the open-loop gain and phase angle of the current control loop are shown in Fig. 25. The control bandwidth is 1.1 kHz, and the phase margin is 40°. Therefore, both the ac voltage and current control bandwidths requirements, which are 300 Hz and 1 kHz, respectively, are achieved.

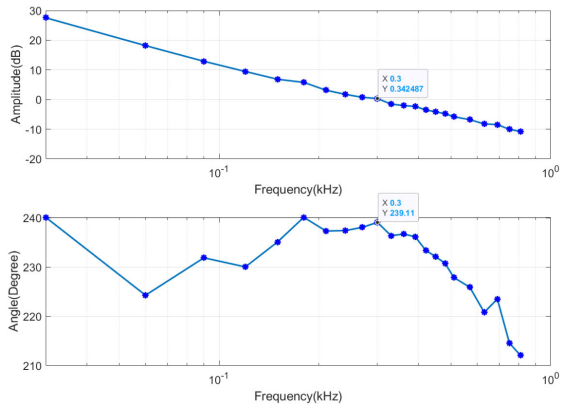


FIGURE 24. The ac voltage control bandwidth test results.

E. GRID FUNCTION TESTS

A MV test platform is designed and developed for the grid function tests, as shown in Fig. 26 [32]. A LV three-phase two-level converter is connected in parallel with the MV PCS converter at both the LV dc side and the MV ac side (with step-up transformers). The LV converter is used as the grid emulator in the grid-connected mode tests and as the loads in the islanded mode test. With the converter, the grid voltage and frequency can be easily controlled and changed, emulating different grid conditions.

With the testbed, the Var (voltage) support, frequency ride through, low voltage ride through, high voltage ride through, ac overvoltage and Undervoltage protection, and over frequency and under frequency protection in the grid-connected mode, and the balanced and unbalanced load support in the islanded mode are all tested [32].

VII. THE SECOND 13.8 KV/ 100 KW PCS CONVERTER PROTOTYPE

To study the paralleling and scalability of the MV PCS converter, another PCS converter prototype needs to be built, and improvement designs are conducted. Based on the experience and testing results obtained from the first converter (version-1), significant size and efficiency improvements are achieved in the second converter (version-2) through improving design for several components and better mechanical design.

A. THE IMPROVEMENT OF THE MV POWER STAGE

The dc-link capacitors are changed to AVX FFVE6N0356K7X, which does not have the bottom stud so the space can be saved. The dc-link layout is also improved. As shown in Fig. 27, the four dc-link capacitors are physically located in a line, and the large dc-link PCB in the version-1 design is divided into two smaller PCBs. One small PCB is used to connect the four capacitors in series and mount the voltage balancing resistors, and the other one is used to connect the dc-link to the devices and gate driver boards. Because of the better flux cancellation effect and the smaller internal stray inductance of the dc capacitors, compared to the version-1 design, the commutation loop inductance of the improved design reduces from 528 nH to 397 nH. Through these changes, the volume of the MV power stage is reduced by 66%.

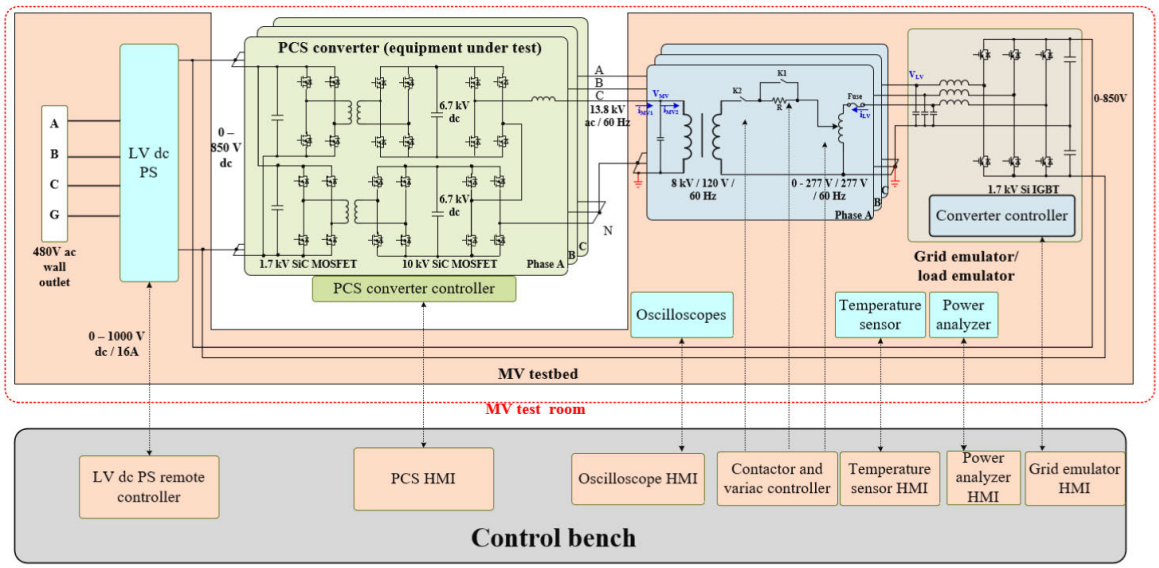


FIGURE 26. The MV testbed for grid function tests.

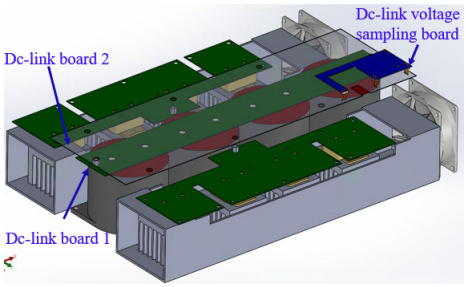


FIGURE 27. The improved dc-link design.

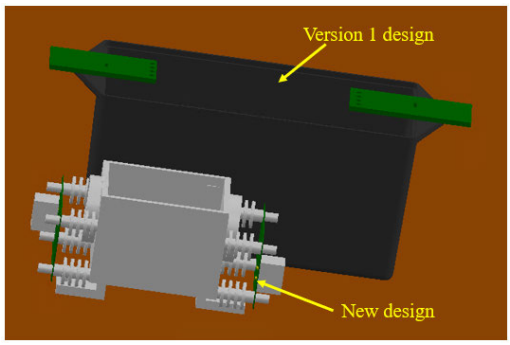


FIGURE 28. The improved GDPS.

B. THE IMPROVEMENT OF THE MV ISOLATED GDPS

The isolated GDPS design is also improved [61]. The comparison between the version-1 design and the improved design is shown in Fig. 28. PSR Fly-buck topology is adopted, considering the common mode noise immunity and control simplicity. A toroid core is used to achieve the required inductance with minimized size. The GDPS transformer is encapsulated with SilGel 613, which has good electric strength so that the insulation distance can be reduced, and the transformer size can be small. The creepage distance is achieved with bushing surrounding the two side terminals and bushing on the PCB board standoffs, which further minimizes the volume of the GDPS. With the improved design, the GDPS volume is reduced by 70% meeting the same insulation capability and power rating requirements. Also, the coupling capacitance is reduced from 1.85 pF to 1.0 pF by adopting a new winding structure, which helps to reduce the common-mode noise through the MV GDPS.

C. THE IMPROVEMENT OF THE MV TRANSFORMER

As discussed in Section VI-B, the version-1 MV MF transformer has high leakage eddy current loss and high parasitic capacitance, affecting the converter efficiency. To reduce the leakage flux induced eddy current loss in the nanocrystalline transformer core, a new leakage integration is adopted, which is shown in Fig. 29. The shell-type structure is selected to reduce the leakage flux induced by the winding structure while adding ferrite bridges to create extra leakage loop and hence increase the leakage inductance back to the desired value [60].

To reduce the parasitic capacitance due to the dry-type insulation and ground shielding, a partial shielding method is used for the MV winding insulation. Only the MV winding surfaces directly facing LV windings and transformer core are shielded, while the other surfaces remain unshielded so that the electric field is only blocked where discharge to the other potentials is likely to take place [60]. With this method, the parasitic capacitance is reduced from 216 pF to 107 pF, so the parasitic capacitance-induced switching loss can also be reduced. Fig. 30 shows the selective shielding and simulation results. According to the simulation result, for the shielded areas, the electric field

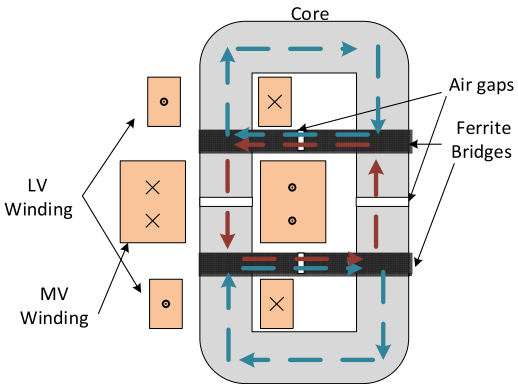
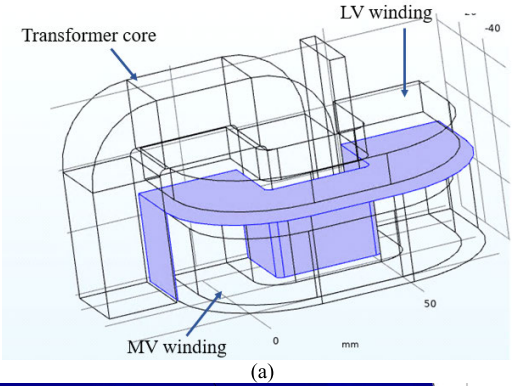
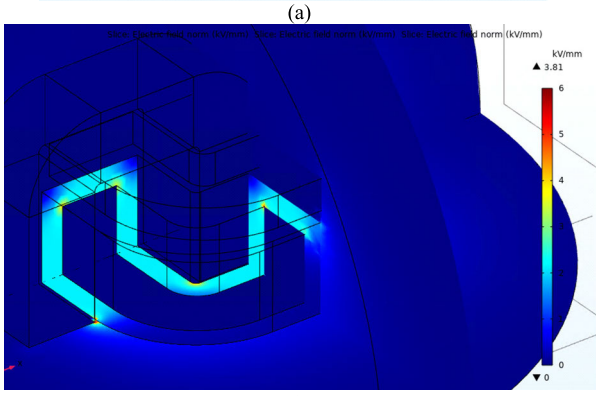


FIGURE 29. The structure of low-loss leakage integrated MV MF transformer.

is concentrated within the dry-type insulation, so that the air gaps between MV winding, transformer core, and LV windings will have no electric field. For the area without shielding, the electric field can be extended to the air, and both the inside and outside of the dry-type winding have a relatively low electric field so that no breakdown will happen during operation. As the electric field may concentrate on the boundary between shielded and unshielded surfaces, silicone putty is used to cover the boundary line, so that the high electric field can also be restricted from corona discharge [60].



(a)



(b)

FIGURE 30. (a) The selective shielding and (b) the simulation result of the improved MV MF transformer design.

D. THE IMPROVEMENT OF THE LV POWER STAGE

To improve efficiency and power density, the LV power stage is redesigned. Another SiC MOSFET (MSC035SMA070) is used, and the LV conduction loss is reduced by approximately 50%, though the switching loss remains similar. In addition, as the loss is reduced, the heat sinks can be shrunk, so that the density is improved by 30%, as shown in Fig. 31.

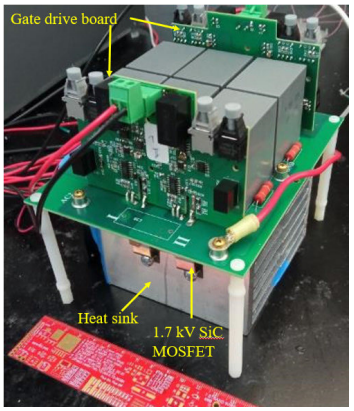


FIGURE 31. The improved LV power stage.

E. THE IMPROVED VERSION OF THE POWER UNIT

The improved power unit is shown in Fig. 32, and its dimensions are 15.5 inches × 8 inches × 27 inches. Compared to the version-1 power unit, the improved power unit volume is reduced by 64%.

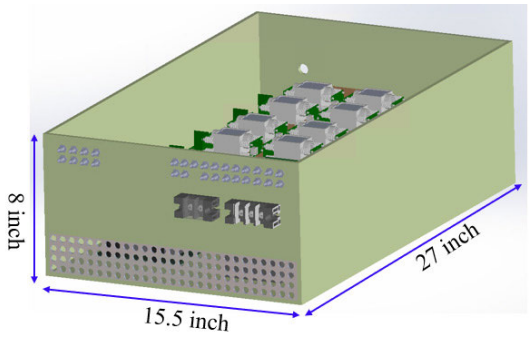


FIGURE 32. The improved power unit.

F. THE SECOND PCS CONVERTER PROTOTYPE

The second 13.8 kV/100 kW PCS converter prototype developed following the improved design is shown in Fig. 33, and its dimensions are 40 inches × 31.562 inches × 43.875 inches. Compared to the first version, the second version achieves a volume reduction of 49%.

VIII. EXPERIMENTAL TESTS OF THE SECOND 13.8 KV/100 KW PCS CONVERTER PROTOTYPE AND THE PARALLELING TESTS

This section discusses the testing results of the second prototype and paralleling test of the two prototypes.

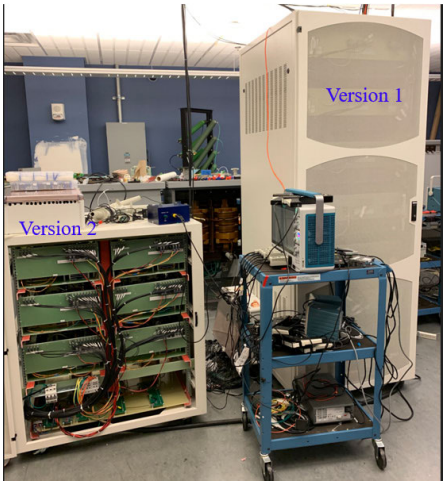


FIGURE 33. The PCS prototypes.

A. EFFICIENCY TEST RESULTS

The converter efficiency is measured with the same approach as the version-1 converter, and the peak efficiency is 98.4% at the rated output power, as shown in Fig. 34. Therefore, compared to the first converter, the efficiency of the second one is increased by 2 percentage points. The efficiency improvement mainly comes from three parts:

a) 10 kV SiC MOSFETs with less loss are used. Two different versions of devices are used in the two converters. Compared to the 10 kV devices used in the version-2 converter, the devices used in the version-1 converter have a similar turn-off loss but a 2x turn-on loss.

b) Smaller parasitic capacitance-related loss because of the smaller parasitic capacitance from the MV transformer and the GDPS.

c) The smaller leakage flux-related power losses in the MV transformers because of the adoption of an optimized leakage integration strategy.

d) The smaller LV power stage loss because the 1.7 kV SiC MOSFETs with lower on-resistance are used.

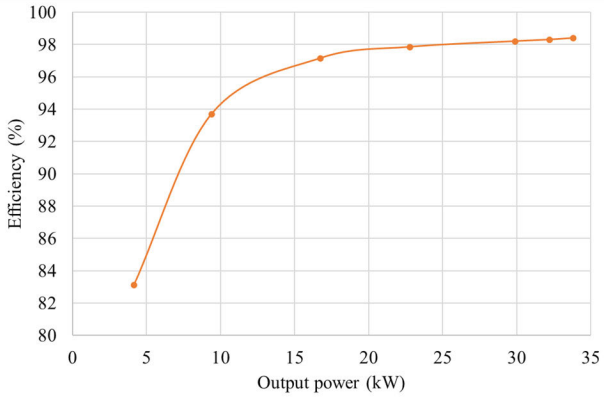


FIGURE 34. The measured efficiency of the second 13.8 kV/100 kW PCS converter.

B. THREE-PHASE FULL RATING TEST

The three-phase tests are conducted with the same setup shown in Fig. 22, achieving the full voltage and power ratings, and the ac side voltage and current waveforms in the rated voltage and current output are shown in Fig. 35.

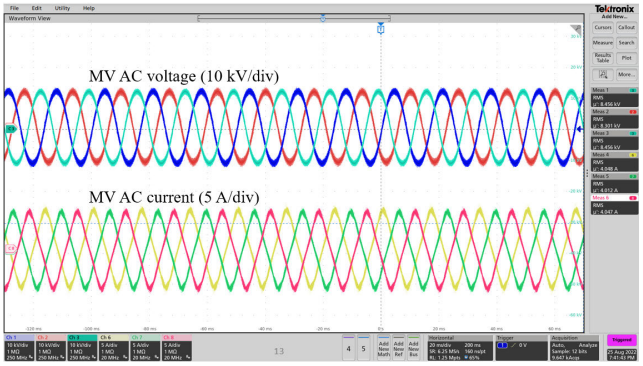


FIGURE 35. The ac side voltage and current waveforms in the three-phase 13.8 kV/100 kVA test.

C. PARALLELING TESTS

The paralleling test setup scheme is shown in Fig. 36. The two PCS converters are in parallel connection at both the LV dc side and the MV ac side. The LV dc is supplied by a LV dc power supply, and PCS converters control the MV ac voltage and frequency, supporting external ac loads. To achieve the power balance and minimize the switching-frequency circulating current, the two PCS converters are operated in master-slave mode. PCS1 operates in master mode, controlling the ac voltage and frequency. It has a voltage angle generator, which generates the phase angle at each switching cycle based on the frequency requirement, and an outer voltage loop, which generates the current reference. PCS2 operates in slave mode, and it controls the current based on the current reference and angle command from the PCS1. Moreover, the two converters share their operation status so that they can start and stop simultaneously.

The MV ac side voltage and current waveforms at rated voltage (13.8 kV line-to-line) are shown in Fig. 37. The MV ac voltages are controlled to be the reference, and the load current is equally shared between PCS 1 and PCS2, which also shows that the circulating current is small.

IX. THE F-CHP CENTRAL CONTROLLER TEST

Two test approaches are used to test the F-CHP system central controller: the HIL and the HTB tests. The HIL test is mainly used for tests of system-level long-term functions, and the central controller and local controllers are integrated using actual communications. The controller hardware and software are tested through various communication and operation scenarios. This allows mimicking the actual implementation in the field, where all control functions are enabled, and inputs and outputs of the controllers are transferred at the same time. The interoperability of the control functions can be tested, and their coupling can be studied. The reliability

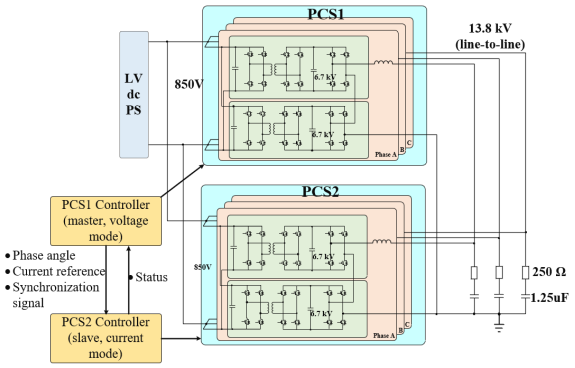


FIGURE 36. The paralleling test setup.

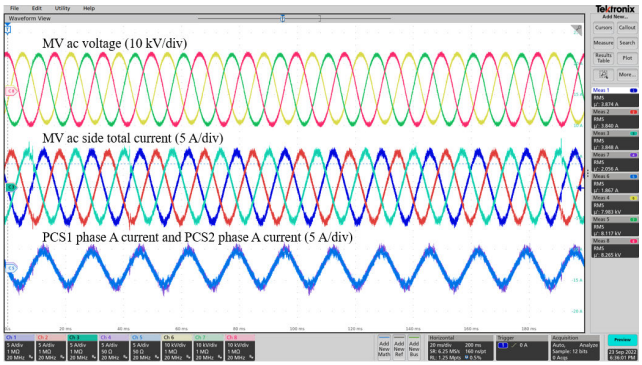


FIGURE 37. MV ac side voltage and current waveforms of the paralleling test.

and robustness of the controllers are also investigated and improved during this stage of testing.

The HTB is a power electronics-based testbed, which utilizes the fast, accurate, and flexible closed-loop control of power electronics converters to mimic the static and dynamic behaviors of electrical power components, and it can overcome many issues with digital emulators and conventional hardware-based grid emulators [64], [65]. It mainly aims at testing the transient conditions of the system and the performances of the power electronics converters and controllers.

A. THE HIL TESTS

The architecture of the HIL test is shown in Fig. 38. The central controller, local source and load controllers, and the PCS converter controller are implemented in several CompactRIOs, which are real-time embedded industrial controllers. An Opal-RT real-time controller is used to simulate the system operation, and the system simulation mode is developed with MATLAB and then converted to Opal-T HIL format. The central controller communicates with the local controllers and the PCS converter controller, receiving operating status and issuing control commands, through a DNP3 communication protocol, which is commonly used among the distribution utilities' SCADA system.

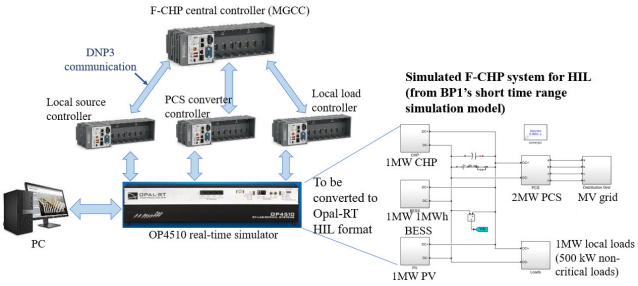


FIGURE 38. Architecture of the HIL test.

Several scenarios are successfully tested with the HIL tests:

1) Black start, which includes system start-up from both islanded and grid-connected conditions.

2) Grid-connected operation. In this case, the grid functions, including frequency support and voltage support are tested. In addition, economic dispatch, which is realized with the energy management function, is tested.

3) Islanded operation. In this mode, the load and source power changes are applied to verify system performances.

4) Reconnection, which means the system transfers from the islanded mode to the grid-connected mode.

5) Grid faults and islanding. The grid faults are applied to both the grid-connected mode and the islanded mode tests.

6) Internal component fault handling, which tests the system response after the internal source failure, especially load-shedding performances.

B. THE HTB TESTS

The architecture of the HTB is shown in Fig. 39, and the hardware picture is shown in Fig. 40 [64]. A small-scale PCS converter, with the same topology and converter controller, is built, to verify the PCS performances in the tests. Moreover, three three-phase two-level converters C1, C2, and C3 are used to emulate different components in the F-CHP system. In the grid-connected mode, converter C1 is used to emulate the MV ac grid. Since it is a three-phase four-wire converter, it can emulate both balanced and unbalanced faults of the MV ac grid by controlling the positive, negative, and zero-sequence voltage. In the islanded mode, the MV ac grid is not available, so C1 is used as the external balanced/unbalanced ac loads. Converters C2 and C3 are connected as three dc/dc converters, respectively. The three dc/dc converters in C2 are used to emulate the CHP source, PV, and battery, respectively. Similarly, the three dc/dc converters in C3 are used to emulate one critical load and two non-critical loads, respectively. PV and load profiles are respectively predefined in their converter controller.

The following tests are conducted [64]:

1) PCS starts up from both islanded and grid-connected conditions.
2) The grid-connected operation, including ac grid fault conditions.
3) Islanded operation without and with external balanced and unbalanced load support.

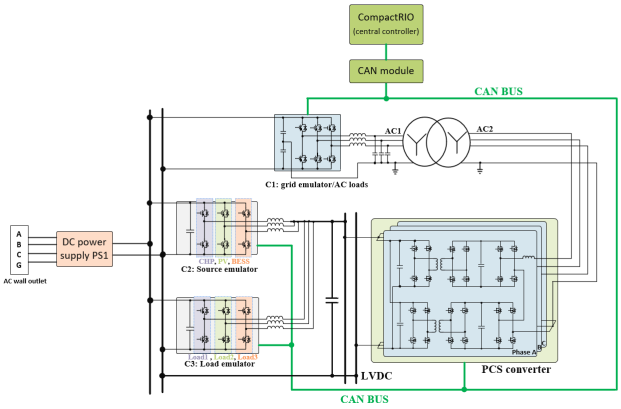


FIGURE 39. Architecture of the HTB test.

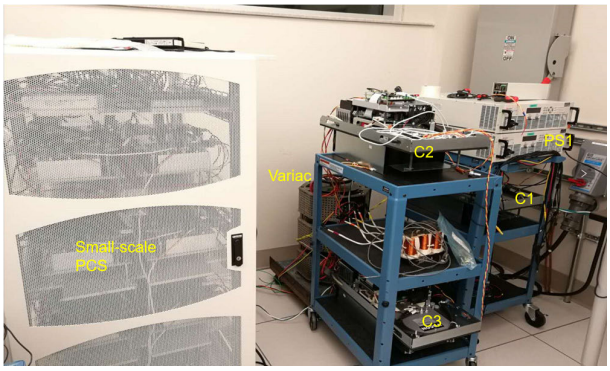


FIGURE 40. Hardware picture of the HTB test setup.

Mode transitions, including planned is landing, unplanned islanding, and reconnection.

X. CONCLUSION

This article discusses the development and control of a power electronics-based F-CHP system, which can provide dispatchable power and other grid support services, such as voltage and frequency support, to the MV ac grid, facilitating the penetration of renewable resources in the grid. There are two focuses. The first one is the PCS converter, which interfaces with the ac grid and provides grid support services. The other part is the F-CHP central controller, which accommodates the system's local source controllers, local load controllers, and the PCS converter controller. The main contribution and accomplishment of this article include:

1) The proposed 10 kV SiC MOSFET-based PCS converter provides a direct MV ac grid interface (no 50/60 Hz transformer needed) with a simple topology. Compared to the LV converter plus transformer solution or LV power semiconductor-based multilevel converter, it brings efficiency and power density benefits. Also, because of the high switching frequency, high control bandwidth is achieved, which enables other grid benefits, such as fast transient response, stability enhancement, and harmonic filtering.
2) The MV PCS converter is designed considering grid requirements and grid abnormal conditions, which increases its reliability and enhances its grid support services.
3) Although the emerging 10 kV SiC MOSFETs bring both converter-level and system-level benefits, there are also many challenges due to the high voltage stress and high dv/dt. The design of the gate drive, MV GDPS, MV MF transformer, the MV filter inductor, as well as the cooling and mechanical design, is discussed considering the insulation requirement, parasitic minimization, and power density improvement.
4) Two 13.8 kV/100 kW converter prototypes are successfully developed and tested to the rated voltage and power ratings. With the high switching frequency, the ac side current and voltage control bandwidths are tested to be 1.1 kHz and 300 Hz, respectively. In the version-2 PCS converter, the peak efficiency of 98.4% is achieved. Moreover, the grid-side functions, such as voltage support, voltage ride through, frequency ride through, and protections, are all tested. Also, the PCS converter paralleling operation has been studied and tested with 2 prototypes in parallel.
5) The controller of the F-CHP system is also proposed. and the central controller is discussed in detail. HIL tests are conducted to verify the long-term functions of the central controller, and HTB tests are used to validate the short-term and transient (grid faults, mode transitions, etc.) performance of the controller and the hardware system.

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HAIGUO LI (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from The University of Tennessee, Knoxville, TN, USA, in 2022.

From May 2022 to September 2022, he was a Research Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee. Since October 2022, he has been a Power Electronics Scientist with the ABB U.S. Research Center, ABB Inc., Raleigh, NC, USA. His research interests include inverter-based resources, grid-forming inverters, virtual synchronous generator-based inverters, grid-connected converter design, control, and test, wide-bandgap devices and their application in power electronics, and MV high-power converter design and control.

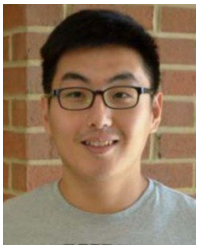
ZIHAN GAO (Student Member, IEEE) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2018. He is currently pursuing the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

He is a Graduate Research Assistant with the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT), Department of Electrical Engineering and Computer Science, The University of Tennessee. His research interests include medium voltage dc/dc converters and medium voltage medium frequency transformers.

FEI (FRED) WANG (Fellow, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1982, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 1985 and 1990, respectively.

He was a Research Scientist with the Electric Power Laboratory, University of Southern California, from 1990 to 1992. In 1992, he joined the GE Power Systems Engineering Department, Schenectady, NY, USA, as an Application Engineer. From 1994 to 2000, he was a Senior Product Development Engineer with GE Industrial Systems, Salem, VA, USA. From 2000 to 2001, he was the Manager of the Electronic and Photonic Systems Technology Laboratory, GE Global Research Center, Schenectady, and Shanghai, China. In 2001, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, as a Research Associate Professor and became an Associate Professor, in 2004. From 2003 to 2009, he was the CPES Technical Director. Since 2009, he has been with The University of Tennessee and the Oak Ridge National Laboratory, Knoxville, TN, USA, as a Professor and the Condra Chair of Excellence in Power Electronics. He is a founding member and the Technical Director of the multi-university NSF/DOE Engineering Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT) led by The University of Tennessee. His research interests include power electronics and power systems. He is a fellow of the U.S. National Academy of Inventors.

YIWEI MA (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2009 and 2011, respectively, and the Ph.D. degree in electrical engineering from The University of Tennessee, Knoxville, TN, USA, in 2019. He is currently a Research Engineer with the Electric Power Research Institute, Knoxville. His research interests include modeling and control of power electronics interfacing converters for renewable energy sources, multilevel converters, and microgrids.

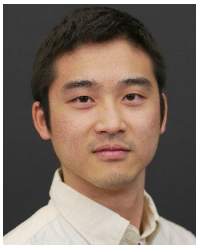


YU SU (Member, IEEE) received the B.Eng. degree from Tsinghua University, Beijing, China, in 2015. He is currently pursuing the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA. His research interests include microgrid design and control optimization, renewable integration in electrical power systems, and the applications of machine learning methods in power systems.

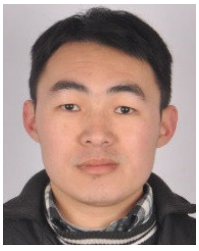
DINGRUI LI (Member, IEEE) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2017. He is currently pursuing the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA. His research interests include control of power converters, medium voltage converters, power converters in grid applications, multi-level converters, and microgrid control.

PENGFEI YAO (Member, IEEE) was born in Inner Mongolia, China, in 1992. He received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2015 and 2020, respectively. From May 2019 to June 2020, he was a Visiting Scholar with the Center for Ultra-Wide Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, TN, USA. He is currently with China Huaneng Group. His research interests include offshore wind power generation, grid integration of multiple energy, including renewable energy, and design and control of grid-connected high-power isolated dc–dc converters.

SHIQI JI (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2010 and 2015, respectively. Since 2015, he has been with the Center for Ultra-Wide Area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, TN, USA, and became a Research Assistant Professor, in 2019. Since 2020, he has been with Tsinghua University, as an Assistant Professor, and then became an Associate Professor, in 2021. He has authored or coauthored more than 50 technical articles. His research interests include semiconductor device modeling, medium-voltage and high-power converter design, high-voltage SiC device characterization and application techniques, and grid-connected converter design.



ZHE YANG received the B.S. and M.S. degrees in electrical engineering from The University of Hong Kong, in 2014 and 2016, respectively, and the Ph.D. degree in electrical engineering from The University of Tennessee, in 2021. He is currently a Senior Applications Engineer with Monolithic Power Systems Inc., San Jose, CA, USA. His research interests include converter design and optimization, and the application of wide bandgap devices.



RUIRUI CHEN (Member, IEEE) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2010, the M.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2013, and the Ph.D. degree in electrical engineering from The University of Tennessee, Knoxville, TN, USA, in 2020.

From 2013 to 2015, he was an Electrical Engineer with FSP-Powerland Technology Inc., China. Since 2020, he has been a Research Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee. His research interests include wide bandgap devices and applications, medium voltage power electronics, cryogenic power electronics, multilevel converters, EMI, and high-efficiency high-power density converters for electrified transportation and grid applications.