

# Development of High-Power Bidirectional DC Solid-State Power Controller for Aircraft Applications

Zhou Dong<sup>ID</sup>, Graduate Student Member, IEEE, Ren Ren<sup>ID</sup>, Member, IEEE, and Fei Wang<sup>ID</sup>, Fellow, IEEE

**Abstract**—The high-power solid-state power controller (SSPC) will be a critical component for the future electrified aircraft propulsion system. This article presents the development of a 1 kV 500 A bidirectional dc SSPC using SiC power modules and transient voltage suppression (TVS) diodes. The design procedure and implementation of the SSPC are presented in detail and the system level influence is discussed. Due to the limited power of a single switch, parallel and/or series connections of switches are necessary for high-power SSPCs, and the corresponding challenges are investigated with possible solutions. In addition, the high peak-to-average clamping voltage ratio caused by  $Ldi/dt$  of the turn-off current commutation and foldback characteristics of high-power TVS diodes is addressed. Finally, the testing setups for the high-power SSPC are presented, and all key functions are tested for the SSPC. The power rating and the specific power of the developed SSPC are superior to state-of-the-art counterparts to show the advantage of the developed one.

**Index Terms**—Electrified aircraft, SiC power module, solid-state circuit breaker, solid-state power controller, TVS diode.

## I. INTRODUCTION

THE electrified aircraft propulsion (EAP) system uses electric motors to fully or partially replace conventional engines to propel aircraft [1]. The benefits of EAP include increased propulsive efficiency, reduced CO<sub>2</sub> emission, and lower noise levels [2]–[4]. For the development of the EAP system, protection is critical to ensure the safety and reliability of aviation.

EAP systems often involve a power electronics enabled dc distribution, which suffers from high fault current due to the large dc-link capacitors and low fault impedance. Moreover,

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Zhou Dong is with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail: zdong9@vols.utk.edu).

Ren Ren is with the Monolithic Power System, Inc., San Jose, CA 95119 USA (e-mail: rren3@vols.utk.edu).

Fei Wang is with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA, and also with the Oak Ridge National Laboratory, Oak Ridge, TN 37830 USA (e-mail: fred.wang@utk.edu).

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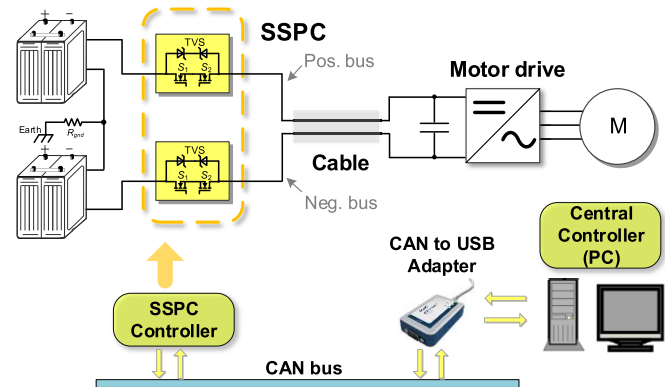


Fig. 1. DC SSPC in a simplified EAP system.

there are no zero-crossing points for the dc distribution load current. Conventional mechanical circuit-breakers normally have a protection time of several milliseconds, which cannot meet the EAP protection requirements due to the weak surge capability of power electronics devices [5]. The emerging solid-state power-controller (SSPC) with several or tens of microseconds protection time promises to provide reliable protection for the EAP system.

An example of using the dc SSPC in a simplified EAP system is shown in Fig. 1. In the system, the SSPC is inserted between the batteries and the cable connected to a downstream motor drive. Two SSPC cells are on the positive and negative buses, respectively, to maintain symmetry and limit the maximum voltage stress from each bus to the ground. With batteries as the source, the SSPC needs to be bidirectional so that it can operate with both charging and discharging modes.

Compared to simple solid-state circuit breakers (SSCBs), SSPCs incorporate more functions including remote control, soft start, ground fault indicator, and condition monitoring [6]. These functions enable smarter coordination with other protection devices in the system and better adaptability in the EAP system. Besides these functions, high specific power is also required for SSPCs in the EAP system.

For future EAP systems, the power rating can achieve the megawatt range and beyond, and the voltage rating can be increased to the medium voltage level [1]. However, the published SSPCs, including commercial products and academic research studies, still have very limited power and voltage ratings. Table I lists reported high-power or high-voltage commercial SSPC products and academic prototypes. For commercial products, the maximum power rating is only

TABLE I  
REPORTED HIGH-POWER OR HIGH-VOLTAGE SSPCS

	Part number or reference	$V_{rated}$ (V)	$I_{rated}$ (I)	$P_{rated}$ (kW)
Commercial products	DDC 28001000N0pb	270	150	40.5
	DDC RP-2A000000X-2C0	28	1100	30.8
	Micropac 53290-270-060	270	60	16.2
	Astronics 1426-10-A8	28	200	5.6
	Sensitron SPDP100D375	375	100	37.5
	Sensitron SPDC150D28	28	150	4.2
Academic work	Leach P800	28	150	4.2
	T. Feehally [7]	270	200	54
	M. Terorde [8]	540	10	5.4
	Y. Guo [9]	320	120	38.4
	Z. Huang [10]	540	100	54

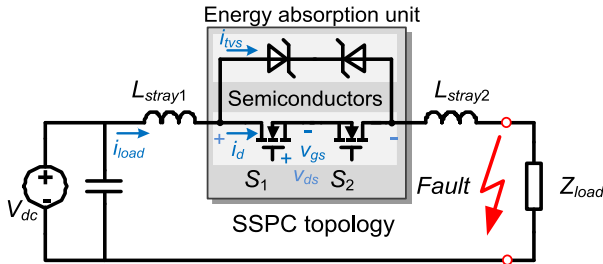


Fig. 2. Common SSPC topology.

40.5 kW, and the maximum voltage rating is only 375 V. For academic prototypes, the one with the highest power rating can be found is 54 kW SSPC developed in [7] and [10], and the one with highest voltage rating is a 540 V unit developed in [8] and [10].

There is a clear need to push the voltage and power rating higher for future EAP applications. However, developing high-power and high-voltage SSPCs poses additional challenges. The main challenges come from the required high power rating components. The required components in the SSPC mainly include power semiconductor switches and the energy absorption unit in Fig. 2.

Due to the lack of power semiconductor switches with sufficient current or voltage ratings, parallel and/or series connections of switches for higher power and voltage ratings are needed. Paralleling of discrete MOSFETs is commonly used in many SSPCs [7], [8], [10], [11]. The advantage is the low cost and flexible gate resistance of each switch. However, the overall size of the switches is large, which would sacrifice the power density. Instead, the power module integrated with multiple-paralleled bare dies can achieve high power density and the required current rating at the same time. However, the high turn-off current of the SSPC during fault may pose some additional challenges for power module design. For example, unwanted gate oscillations are observed in [10] and [12] when turning off high currents. On the other hand, the series connection of switches brings fewer concerns because the voltage balance benefits from the energy absorption unit.

For the energy absorption unit, the transient voltage suppression (TVS) diode is an attractive solution to the metal oxide varistor (MOV) owing to faster response speed and lower clamping ratio. Moreover, the MOV has a degradation issue,

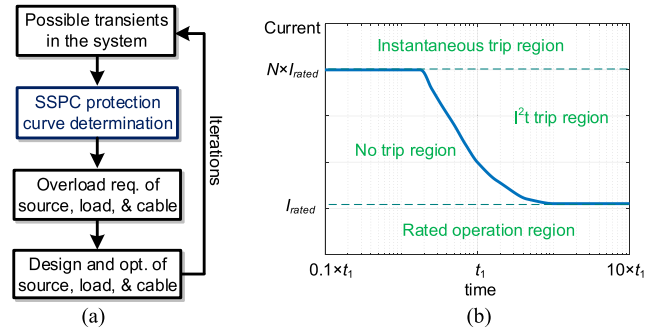


Fig. 3. System-level influence of the SSPC design and a typical protection curve. (a) System-level influence. (b) Typical protection curve.

which makes it not suitable for aircraft applications [13], [14]. The low-power TVS diode normally has a very low clamping factor (ratio of clamping voltage to breakdown voltage), and a typical value is around 1.33 [15]. However, for high-power TVS diodes, to withstand the large power during the transient, the foldback technique is required. This characteristic has seldom been discussed in published literature, although some of the tested waveforms can be noticed with such a phenomenon [11]. An alternative solution is to parallel low-power TVS diodes to achieve a high power rating [16]. However, the positive temperature coefficient and possible mismatch of TVS diode breakdown voltage make it challenging to distribute current evenly for multiple-paralleled TVS diodes, which is not preferred by manufacturers [17].

In this article, the challenges of constructing high-power semiconductor switches and using high-power TVS diodes are discussed in detail. Moreover, the influence of the SSPC on system optimization is discussed and a comprehensive design procedure is provided. Finally, the development and test of a bidirectional dc SSPC with 1 kV 500 A (500 kW) rated condition is presented.

The remainder of this article is organized as follows. Section II describes the system-level influence and design procedure of the SSPC. Sections III and IV are mainly about the electrical design, which includes the two key topics: the switch selection and the TVS diode selection. Section III analyzes the challenges of paralleling and series of switching cells. Then in Section IV, the high peak-to-average clamping ratio issue caused by the commutation  $Ldi/dt$  voltage and the foldback characteristic of high-power TVS diodes are discussed. Section V introduces the implementation of the hardware and software. In Section VI, the test setups and results are presented. Finally, Section VII concludes the article.

## II. DESIGN PROCEDURE OF SSPC

The SSPC design and protection curve determination procedures are discussed in this section.

### A. Overall SSPC Design and Protection Curve Determination Procedure

As a critical part of the system, SSPC design can be part of the system optimization as shown in Fig. 3(a). The key

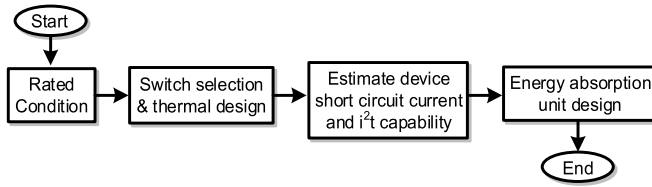


Fig. 4. SSPC design procedure.

factor that can influence the system is the protection curve. A typical protection curve is shown in Fig. 3(b). It normally includes an instantaneous trip region for the short circuit protection and an overload or  $i^2t$  trip region for the overload protection [18]. The reason for the time delay of protection in the  $i^2t$  trip region is to minimize the nuisance trips caused by the possible transients in the system, e.g., inrush current. Therefore, the SSPC protection curve can be determined by these possible transients. With the determined protection curve, the weakest points in the current path can be protected, which could be the load, source, cable, or switch itself [19]. Thus, the overload requirements of the load, source, and cable can be influenced by the protection curve. These overload requirements can influence the design and optimization of these parts, which in turn also influences possible transients in the system. Thus, a scientific way to determine the protection curve requires some iterations in the system-level study. With different systems, the normalized protection curves can be very different, e.g., the instantaneous trip current ranges from  $1.5 \times$  to  $11 \times$  of the rated current in [7]–[10] and [20]–[24].

However, the detail of the entire system is not always known. In this case, the protection curve can be simplified to be determined by the device capability using the device and thermal design satisfying the rated condition and efficiency requirements. The overall SSPC design procedure in this article is shown in Fig. 4. First, the device is selected and the thermal management system is designed based on the rated condition requirement. Then, the short circuit current and  $i^2t$  curve of the SSPC is determined by the device capability. After that, the energy absorption unit is designed based on the instantaneous trip current and line inductance requirements.

### B. Design Specifications and Topology Selection

The design specifications of the SSPC are listed in Table II with the required functions. The required high efficiency and specific power make the design challenging. Note that the rated voltage around 1 kV is mainly for near-term EAP applications. Higher voltage and power may be required for SSPCs in future EAP systems. However, the challenges addressed and techniques used in this article should also be applicable to those specifications.

Commonly used topologies for SSPCs have been discussed in [25]. Among them, the one shown in Fig. 2 with a power semiconductor switch paralleled with the TVS diode as the energy absorption unit is selected owing to high reliability with the simplest structure and the minimum number of components. Note that this topology only includes one SSPC

TABLE II  
SSPC SPECIFICATIONS

Type	Bidirectional DC
Operation	4-quadrant switch (can block voltage in both directions when open and conduct current in both directions when closed)
Rated voltage $V_{rated}$	1 kV
Rated current $I_{rated}$	500 A
Efficiency	>99.5%
Specific power	>100 kW/kg
Protection curve	Based on the device's capability
Protections	Over-current and short circuit protections
Control	Close, open, reset via CAN bus command
Other function	Soft start and ground fault indicator
Indication	Switch status, current, voltage, temperature, and fault type
Cable inductance	5 $\mu$ H

cell while in Fig. 1 the bipolar structure requires two cells in series.

### III. DEVICE SELECTION, THERMAL DESIGN, AND PARALLELED AND SERIES SWITCHES

In this section, the selection of the device and the thermal design are conducted to meet the high efficiency and specific power requirements. More importantly, the challenges of paralleling and series of switches in high power SSPCs are identified and possible solutions are discussed.

#### A. Device Selection and Thermal Design

Device selection and thermal design are critical to the specific power and efficiency of the SSPC. High power SiC power modules with multiple paralleled bare dies are suitable for the voltage and current range with the low conduction loss and small required surface area for the thermal design.

Two SiC power modules HT3220 [16] from Cree company are paralleled for the 500 A-rated condition. The module has a common-source structure and is intended for bidirectional applications. The device loss in the SSPC is mainly the conduction loss. For each module, the conduction loss is calculated as

$$P_{\text{cond}} = \left( \frac{I_{\text{rated}}}{N_p} \right)^2 (R_{\text{dson,f}} + R_{\text{dson,r}}) \quad (1)$$

where  $N_p$  is the number of paralleled power modules, and  $R_{\text{dson,f}}$  and  $R_{\text{dson,r}}$  are the forward and reverse on-resistance of the device, respectively. With  $R_{\text{dson,f}} = 5.2 \text{ m}\Omega$  and  $R_{\text{dson,r}} = 4.4 \text{ m}\Omega$ , the conduction loss of each module is calculated as 600 W. The loss for the two paralleled modules is 1200 W. For two series SSPC cells, the overall loss is 2400 W.

Liquid cooling is used for thermal management because of its low thermal resistance. Based on the required thermal resistance and surface area of the devices, a cold plate Wakefield-Vette-120 960 is selected with a thermal sheet TG-A126X as the thermal interface material. The cold plate has a double-sided cooling structure, so the device can be placed on both sides of the cold plate to reduce half of the required

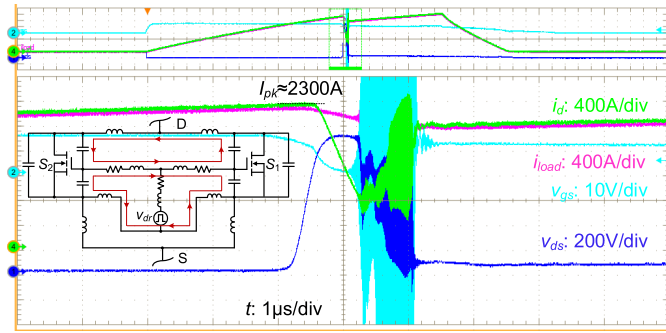


Fig. 5. Waveform of power module gate oscillation due to paralleled bare dies with a paralleled MOSFET circuit in it.

surface area. The operating junction temperature  $T_j$  can be calculated by

$$T_j = T_{cl} + P_{cond,f} R_{th,jc} + N_p P_{cond} (R_{th,tim} + R_{th,cp}) \quad (2)$$

where,  $R_{th,jc}$ ,  $R_{th,tim}$ , and  $R_{th,cp}$  are thermal resistance of power module junction to case per switch position, thermal interface material, and the cold plate, respectively.  $P_{cond,f}$  is the forward conduction loss corresponding to  $R_{dson,f}$ . The two sides of the cold plate have different thermal resistance, and the top side has a larger thermal resistance, which is used in the calculation. With the values of  $R_{th,jc}$ ,  $R_{th,tim}$ , and  $R_{th,cp}$  to be 0.07, 0.006, and 0.016 °C/W, respectively, the estimated  $T_j$  is 74.2 °C with the coolant temperature  $T_{cl} = 25$  °C.

### B. Paralleled Switches and Protection Curve Determination

Paralleling switches can cause the static current imbalance, the dynamic current imbalance, and the potential paralleling instability issues. For SSPCs, since there are no high-frequency repetitive switching actions, the dynamic current imbalance has a minor impact. Thus, the main discussions are on parallel instability and static current balancing.

The paralleling instability issue is found for multiple bare dies paralleled in one power module when turning off a high fault current. The differential mode gate voltage oscillation happens at high voltage and current stresses, due to the high transconductance in that region [26], [27]. The issue is severe for SiC MOSFETs with channel length modulation and is likely to happen in SSPC applications with high turn-off currents. An example waveform of the turn-off failure due to the bare die parallel instability induced by the small inner gate resistance of each bare die is shown in Fig. 5. The waveform is tested using the circuit in Fig. 2. For the power module used, the highest turn-off current without the gate oscillation can only achieve 1 kA at a junction temperature of 90 °C [12]. The concern could be minimized by optimizing the inner gate resistance of each bare die with the development and maturation of high-power SiC power modules. However, in this case, we have to adapt the protection curve of the SSPC within the device safety operating area (SOA) to avoid gate oscillation.

The power module contains ten SiC dies CPM2-1200-0025B (1.2 kV, 90 A-rated) per switch position [28], and

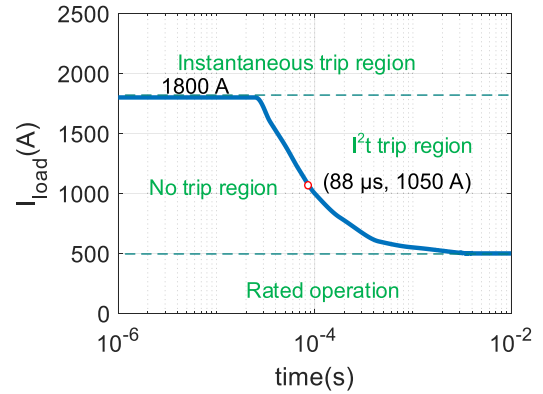


Fig. 6. Determined protection curve of the SSPC.

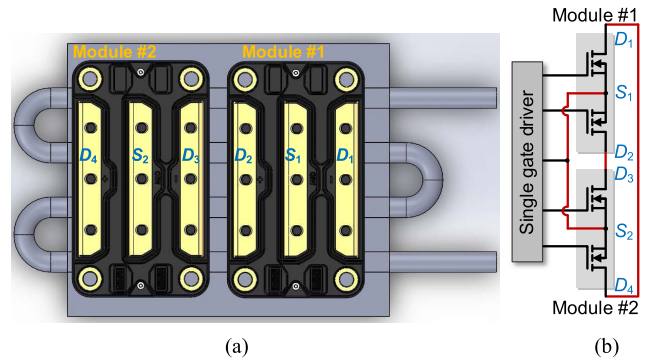


Fig. 7. Placement and connection of paralleled power modules. (a) Module placement. (b) Connection.

based on the SOA curve of the datasheet, each die can withstand 250 A surge current for around 100 μs. Thus, theoretically, for two paralleled modules with 20 dies, the overall surge capability can achieve around 5 kA for 100 μs. However, the module has to be limited with a turn-off current of 1 kA at 90 °C to avoid possible instability issues [12]. Thus, the instantaneous trip value is determined as 1.8 kA for two modules in parallel. For the  $i^2t$  capability, the device is characterized by the selected cold plate. The detailed characterization method and results can be found in [18]. The real-time junction temperature can be estimated during the characterization by the measured  $R_{dson}$  of the device. In this study, the  $i^2t$  region of the protection curve is conservatively estimated by a temperature increase of less than 5 °C to make sure the junction temperature of the power module is lower than 90 °C. The determined protection curve is shown in Fig. 6.

For paralleled power modules, this instability issue can be easily avoided because the gate resistance of each power module is flexible to change.

On the other hand, the static current balance of power modules benefits from the positive temperature coefficient of SiC MOSFETs. Using connection in Fig. 7, the paralleled switches are in different modules so that the steady-state current can be shared more evenly owing to the temperature difference between the two modules with the lower thermal coupling.

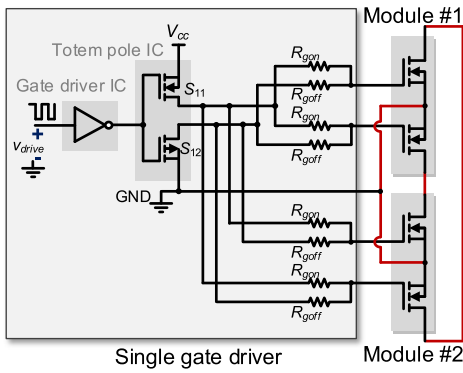


Fig. 8. Shared gate driver for paralleled SSPC modules.

### C. Shared Gate Driver

To save the auxiliary power supplies, a shared gate driver is used for two paralleled common-source power modules with separated gate resistance for each switch position as shown in Fig. 7(b). The detailed gate driver circuit is given in Fig. 8. To ensure enough driving capability of the gate driver, a totem pole IC SQJ500AEP from Vishay with 9.2 m $\Omega$  sink resistance and 27 m $\Omega$  source resistance is cascaded after a gate driver IC IXDI609 from IXYS. The gate drive resistances  $R_{gon}$  and  $R_{goff}$  for each switch in the module are 10 and 2.5  $\Omega$ , respectively. The logic of the input driving signal  $v_{drive}$  is the same as the driving voltage by selecting the driver IC IXDI609 to be an inverting one.

### D. Series Switches

For 1 kV rated voltage, two SSPC cells are in series for the bipolar structure and higher voltage rating. The paralleled TVS diodes are helpful to clamp and balance the voltage across each series switch even with a certain timing mismatch during the transient. During steady state, the voltage could be unbalanced due to different leakage currents or insulation resistances of two series switching cells. To overcome the issue, each SSPC cell is paralleled with a 50 k $\Omega$  resistor to help with the static voltage balance.

## IV. TVS DIODE SELECTION AND HIGH PEAK-TO-AVERAGE CLAMPING RATIO OF HIGH POWER TVS DIODE

The selection of the TVS diode is introduced, which follows a similar approach for selecting a low-power TVS diode [29]. Some mismatches about the clamping voltage are observed during the implementation and test, which is discussed in this section.

### A. TVS Diode Selection

The selection of the TVS diode is based on the voltage and energy requirements. The voltage requirements include: 1) overall standoff voltage should be larger than the dc input voltage and 2) peak clamping voltage should be lower than the voltage rating of the paralleled switches. The absorption

energy requirement needs to consider the largest loop inductance, input voltage, and average clamping voltage.

The TVS diode AK10-380C from the Littelfuse Company is selected with two in series for paralleling each SiC power module. Thus, each TVS diode has a peak pulse current  $I_{cl}$  of 900 A. The standoff voltage is 380 V considering 250 V voltage stress across each TVS diode when the SSPC is open. The breakdown voltage  $V_{br}$  for each TVS diode is between 401 and 443 V. The clamping voltage  $V_{cl}$  for each TVS diode is between 412 and 450 V calculated from (3) using  $V_{cl,max} = 520$  V and  $I_{cl,max} = 10$  kA from the datasheet. For two TVS diodes in series, the maximum overall clamping voltage is 900 V when  $I_{cl} = 900$  A, which gives a 33% voltage margin of the 1200 V voltage rating of the power module

$$V_{cl} = \frac{V_{cl,max} - V_{br}}{I_{cl,max}} I_{cl} + V_{br}. \quad (3)$$

The energy rating of the TVS diode is checked by comparing the required pulsewidth length and the maximum withstand time with the same peak pulse power. Moreover, with the overall inductance in the system, the maximum required absorption energy for the TVS diode can be considered. The overall line inductance includes the cable inductance given in Table II and the equivalent series inductance of the battery in Fig. 1. Based on [30], the series inductance of a 1 kV 200 Ah LiNiCoMnO<sub>2</sub> battery is estimated to be 3.18  $\mu$ H. Thus, the overall line inductance is 8.18  $\mu$ H. The maximum required pulsewidth length is calculated with the minimum clamping voltage. With a peak current of 900 A and a minimum clamping voltage of 824 V, the peak pulse power is 742 kW. The required pulsewidth is calculated using (4), and the result is 22.7  $\mu$ s

$$\Delta t = \frac{L_{series} I_{peak,tot}}{V_{cl,tot} - V_{bus}}. \quad (4)$$

Note that the energy curve tested for the TVS diode is for the double exponential curve while the current waveform of the TVS diode in SSPCs is more like a sawtooth shape. Thus, the required withstand time of a sawtooth curve is normalized from the exponential curve by a factor of 2.8 giving the same energy dissipation [29]. For the double exponential curve, the withstand time corresponds to the period for current reducing to half of the peak value while for the sawtooth curve, the withstand time corresponds to the period for current reducing to zero. As shown in Fig. 9, the withstand pulsewidth for a peak pulse power of 742 kW is 330  $\mu$ s, which is around 14.5 times the required time, meaning the energy absorption requirement can be met with a large margin. This energy margin can allow the SSPC to operate in another system with 14.5 times of the line inductance or 14.5 times of the peak current if the paralleled switch can successfully turn off.

### B. Analysis of Voltage Stress During Turn-Off

The SSPC cell, including the power module and TVS diode shown in Fig. 2, is tested. It is found that the voltage stress is higher than expected. An example testing waveform is shown in Fig. 10. The energy absorption unit is constructed by one AK10-380C series with one AK10-240C with a lower clamping voltage than selected TVS diodes, two AK10-380C

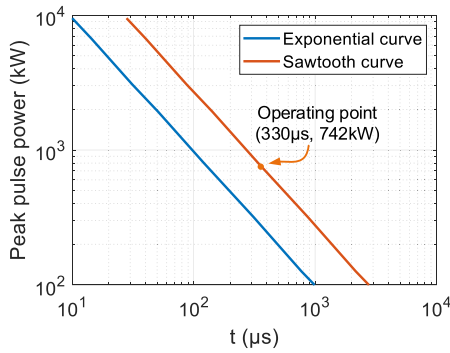


Fig. 9. Peak pulse power rating curve of a TVS diode AK10-380C.

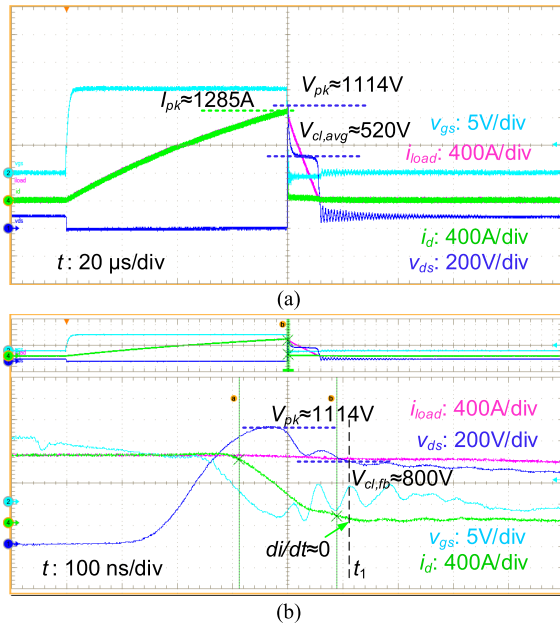


Fig. 10. Turn-off voltage spike of the switching cell. (a) Tested waveform. (b) Zoomed in test waveform.

in series, in the design. The peak voltage across the drain to the source of the device is 1114 V when the turn-off current is 1285 A, and the average clamping voltage is around 520 V. When the selected TVS diodes in the design with higher breakdown voltage are used, the peak voltage would exceed the device voltage rating of 1200 V.

For the low-power SSPCs, the turn-off voltage stress is constructed by a nearly constant clamping voltage and  $Ldi/dt$  voltage caused by the commutation. However, in the zoomed-in waveform of Fig. 10, the clamping voltage ( $V_{cl,fb} = 800$  V) across the TVS diode is still much higher than the average clamping voltage of 550 V even after the  $di/dt$  of the commutation current drops to zero at the time instant  $t_1$ . This is due to the foldback characteristic of high-power TVS diodes, which features as the clamping voltage drops at the beginning of the clamping period. The overall voltage stress can be decomposed into three parts as listed in Table III in this case. The voltage caused by the foldback characteristic can take around 25.1% of the overall voltage stress. The peak-to-average clamping ratio is 2.14.

TABLE III  
VOLTAGE BREAKDOWN OF THE TESTED SSPC CELL

Items	Voltage level (V)	Percentage
Average clamping voltage	520	46.7%
Voltage caused by $Ldi/dt$	314	28.2%
Voltage caused by foldback characteristic	280	25.1%
Overall voltage/V	1114	100%

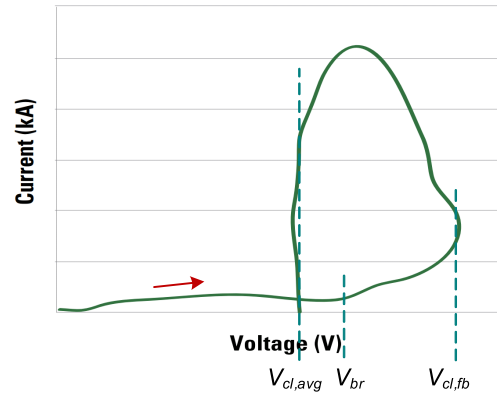


Fig. 11. Surge response caused by foldback of high power TVS diode [32].

### C. Foldback Characteristic

The foldback characteristic of high-power TVS diodes reduces the clamping voltage to a lower voltage level to limit the power dissipation and prevent thermal runaway. An example surge curve caused by the foldback characteristic is shown in Fig. 11. The voltage across the TVS diode at the beginning of the breakdown is higher than the average of the clamping voltage. Such characteristic is specific for high power TVS diode to achieve a small die size while accommodating high pulse currents. The largest conventional TVS diode without the foldback characteristic from Littelfuse Company is 30KPA series, which can only achieve 300 A peak current for 20  $\mu$ s exponential curve [31]. Products from other companies, e.g., Bourns, also follow a similar trend. Therefore, such characteristics can hardly be avoided when using high-power TVS diodes to develop high-power SSPCs.

### D. Solution to Reduce Overvoltage

To reduce the overvoltage of the switch, the part that can be minimized is the one caused by  $Ldi/dt$ . In this article, a solution is conceived from [33] of using dedicated overvoltage clamping MOVs to parallel with energy absorption MOVs to reduce the overvoltage induced by the large inductance. Similar solution and design methodology are used here to separately select a dedicated overvoltage clamping TVS diode to parallel with the energy absorption TVS diode as shown in Fig. 12. The overvoltage TVS clamping diode is selected as ATV50C401JB (two in series) with a breakdown voltage of 894 V. These TVS diodes feature smaller packages and are placed closer to the switch to reduce the commutation voltage. Moreover, they do not have the foldback characteristic.

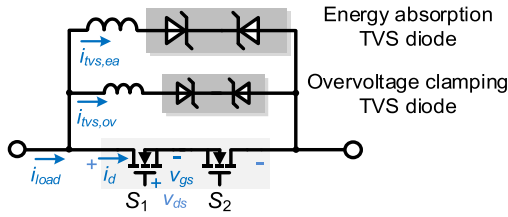


Fig. 12. Modified SSPC topology with overvoltage clamping TVS diodes.

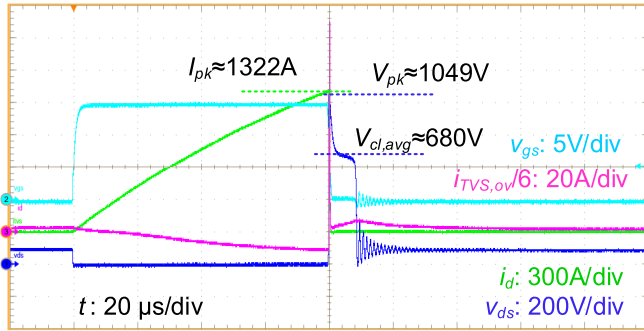


Fig. 13. Turn-off waveform of the SSPC cell with overvoltage clamping TVS diodes.

With the paralleled TVS diodes in Fig. 12 used, tested waveforms are shown in Fig. 13. This test is with two AK10-380 in series as the energy absorption TVS diodes and six paralleled and two series ATV50C401JB TVS diode arrays as the overvoltage clamping TVS diodes. The average clamping voltage is around 680 V. Note that this average clamping voltage is much smaller than the expected value in the design stage because of the foldback characteristic. The peak voltage is 1049 V when the turn-off current is 1322 A using the same gate resistance of 5.5  $\Omega$  for the device to turn off. The peak-to-average clamping ratio is reduced from 2.14 without the overvoltage TVS diodes to 1.54 with the overvoltage TVS diodes. Note that the pink curve of the overvoltage TVS diode current is for one of the six paralleled TVS diodes. The negative current values before the TVS diode breakdown are measured because the Rogowski coil used is influenced by nearby conductors.

The average clamping voltage is lower than the minimum value of 824 V in the design. This means that a TVS diode with underestimated energy requirement could be selected if the foldback characteristic is not considered in the design stage. Using the updated average clamping voltage, the required pulsewidth is calculated as 40.9  $\mu$ s using (4), which is 80.2% longer than the expected pulsewidth of 22.7  $\mu$ s in the design. Since enough margin is given in the design, the energy absorption requirement, in this case, can still be satisfied.

As a summary, the foldback characteristic brings drawbacks including:

- 1) Higher clamping voltage at the beginning of breakdown would overlap with the commutation  $Ldi/dt$  voltage to increase the device voltage stress.
- 2) Lower average clamping voltage during the clamping period results in a longer interruption time and larger energy absorption requirement.

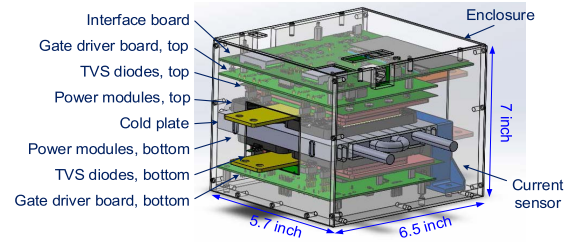


Fig. 14. 3-D model of the mechanical design of SSPC.

## V. HARDWARE AND SOFTWARE DEVELOPMENT OF SSPC

The hardware and software development and some other functions are discussed in this section.

### A. Hardware Development

For the implementation of protection, short circuit protection with the instantaneous trip is implemented by DeSat protection circuit. The  $i^2t$  or overload protection is implemented with the sensed current using a hall sensor HAT-600S with a  $\pm 1800$  A sensing rating. The voltage sensing is implemented with the resistor divider. The temperature sensing is by resistance temperature detector (RTD) inside the module with isolated amplifiers for the central controller, a TMS320F28379D controlCARD, of the SSPC. The controller area network (CAN) serial communication is applied using an SN65HVD235 CAN bus transceiver IC on the SSPC side.

Mechanical design is implemented for an integrated prototype considering the insulation requirement. The bus bar is designed to parallel power modules and connect the input and output. The current density is controlled as a minimum value of 5 A/mm<sup>2</sup>. Ceramic coating of the bus bar is applied with the material of DK15-0907 from Solepox Company for insulation purposes. The coating thickness is 0.15–0.3 mm with a dielectric strength of 15 kV/mm, which can provide an insulation voltage larger than 2.25 kV. In addition, the enclosure is designed using FR4 material for insulation consideration. The 3-D model of the mechanical design is shown in Fig. 14.

### B. Software Development

Software development can be divided into two parts. One is for the distributed controller of the SSPC, and the other is for the central controller of the PC. The SSPC controller is implemented with C language for the DSP. The PC central controller is developed with C# language. Communication is also conducted between the two controllers through the CAN bus. The overall control architecture is shown in Fig. 15. The SSPC controller will sample the voltage, current, and temperature information and send it to the central controller. Besides, protection can be tripped based on the sampled conditions and the fault information is feedback to the central controller. Moreover, it can close, open, and reset the SSPC based on commands from the central controller.

A user interface (UI) is developed for the central controller and the main page is shown in Fig. 16. Switches control options are provided, and each fault condition can be indicated

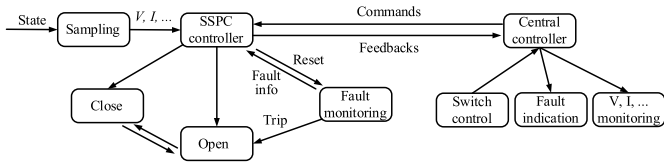


Fig. 15. Control architecture of the SSPC.

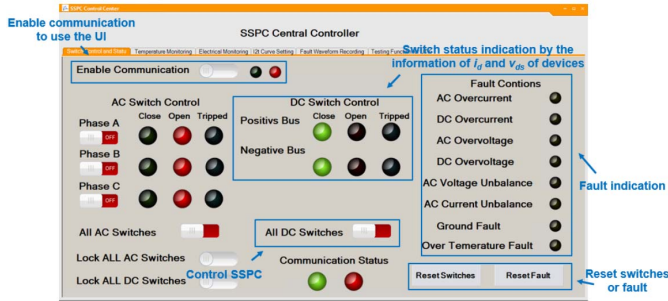


Fig. 16. UI of the SSPC.

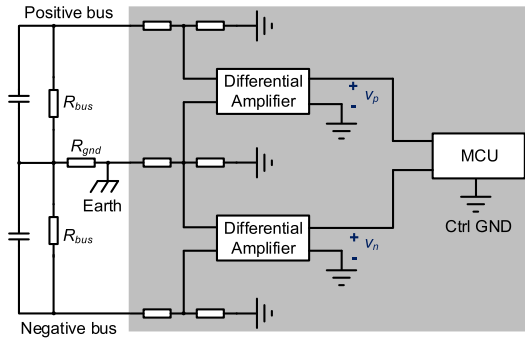


Fig. 17. Sensing circuit of the ground fault indicator.

once triggered. With the UI, users can remotely control and know the working conditions of the SSPC. On other pages of the UI, temperature and current monitoring can also be visualized.

### C. Soft-Start Function and Ground Fault Indicator

The soft-start function is implemented in the SSPC to help reduce the inrush current during the turn-on of the switches. In [12], the detailed design is presented. A low-power auxiliary switch is turned on first to charge the load capacitance to reduce the drain–source voltage across the main switches. The main switch can be turned on with the drain–source voltage lower than 10 V. This minimizes the inrush current and reduces possible nuisance trips caused by it.

The ground fault detector is mainly used to indicate the fault. It will not trip the SSPC to open, even when the fault occurs. The ground fault detector is implemented by checking the voltage differences between positive and negative buses to the earth with a sensing circuit shown in Fig. 17. The system is grounded with a 1 M $\Omega$  grounding resistance at the midpoint of the 1 kV bus. Differential amplifiers are used to sample the voltage between positive or negative buses to the ground to determine whether one of the buses is shorted to the ground.

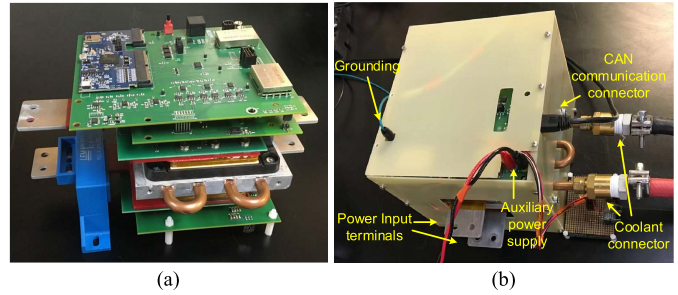


Fig. 18. Prototype of the developed SSPC. (a) Without enclosure. (b) With enclosure.

TABLE IV  
MAIN COMPONENTS OF THE DEVELOPED SSPC

Power module	HT-3220 $\times$ 4 (1.2 kV 642 A@ $T_c=25^\circ\text{C}$ )
Energy absorption TVS diodes	AK10-380C $\times$ 8 ( $V_{br}=401$ V)
Voltage clamping TVS diodes	ATV50C401JB $\times$ 48 ( $V_{br}=447$ V)
Cold plate	Wakefield-vette-120960
Current sensor	HAT 600S
Controller	TMS320F28379D
CAN receiver IC	SN65HVD235
Gate drive IC	IXDD609 $\times$ 2 + SQJ500AEP $\times$ 2

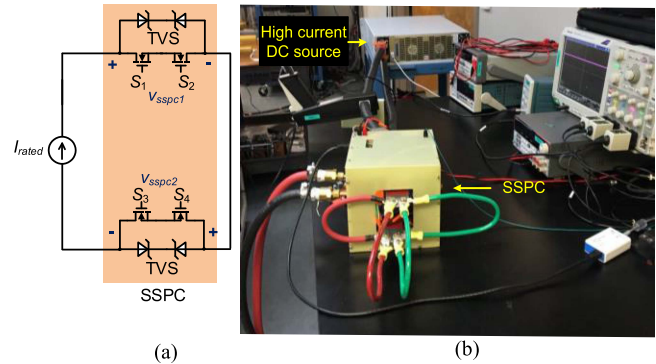


Fig. 19. Steady-state test circuit and setup. (a) Test circuit. (b) Test setup.

The ground fault is indicated once the difference between two sensed voltages is larger than a defined threshold.

## VI. TEST CIRCUITS, TEST SETUPS, AND EXPERIMENTAL RESULTS

The high-power test is also challenging due to the limited facilities in the laboratory. Test circuits and setups are introduced, and experiments are conducted to verify the design and functionality of the developed SSPC.

### A. Developed SSPC Prototype

The hardware is implemented with the enclosure. The prototypes with and without enclosure are shown in Fig. 18. The main components used are summarized in Table IV.

### B. Steady-State Test

The steady-state test circuit is shown in Fig. 19. To avoid the high-power load required for the test, the output of the SSPC is short-circuited. The current through the SSPC is



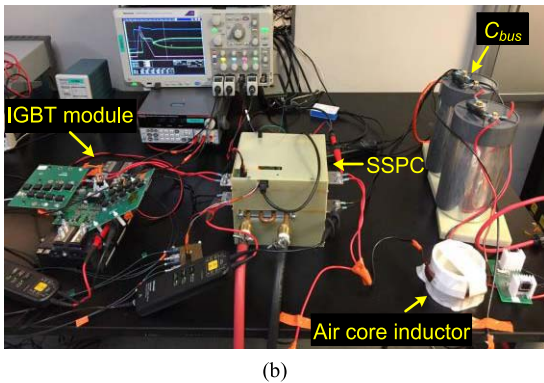
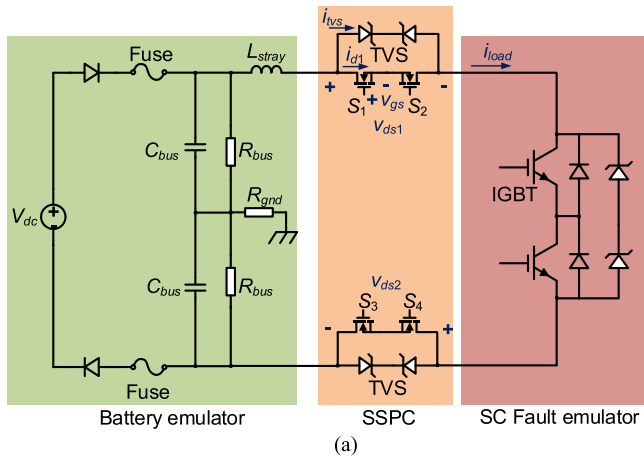


Fig. 20. Short circuit protection test circuit and setup. (a) Test circuit. (b) Test setup.

controlled by a low-voltage high-current dc source operating at current limiting mode. The conduction loss of the SSPC is the same as operating with a 500 kW load with the same current of 500 A.

With the voltage drops  $V_{sspc1}$  and  $V_{sspc2}$  of the positive and negative buses tested as 2.605 and 1.936 V, respectively, the overall loss is 2280.9 W, and the efficiency is 99.51%. Among the total loss, the power module loss is 2188 W, and the bus bar loss is 82.5 W. The difference between the voltage drops of the two modules is caused by the discrepancy of the switches.

### C. Short Circuit Protection Test

Fig. 20 shows the short circuit protection test circuit and test platform. Two high-capacity capacitors are used to emulate the battery to generate a short circuit current. The voltage across the capacitors is 1 kV so that both high voltage and current stress under the worst operating conditions can be generated for SSPC switches. The line inductance is emulated with an air-core inductor. During the test, the SSPC is closed with a controlled coolant temperature to emulate the normal operation. Then, a short circuit event is triggered by a high-power half-bridge insulated-gate bipolar transistor (IGBT) module CM2500DY-24S (1.2 kV 2.5 kA rated). Fig. 21 shows the short circuit protection waveform at 75 °C. The SSPC protects at a current level of around 1760 A with a preset instantaneous current trip current of 1800 A.

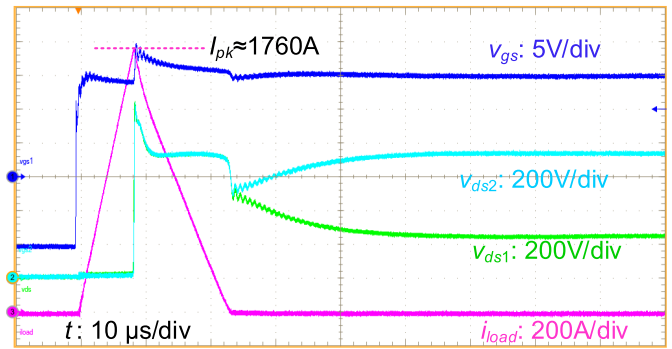


Fig. 21. Waveforms of short circuit protection with 1750 A total current.

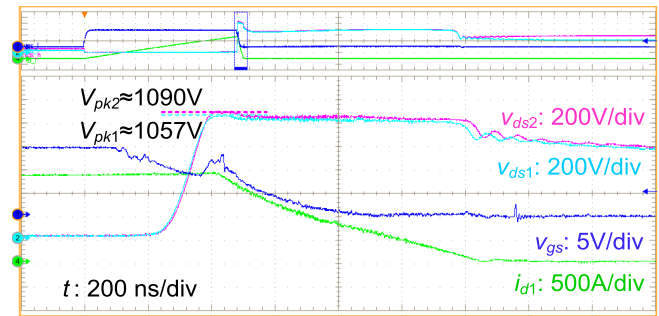


Fig. 22. Test of series switches with paralleled TVS diodes.

To illustrate the voltage sharing performance of the series-connected switches, a test waveform during the turn-off transient is shown in Fig. 22. During the transient, a negligible delay can be observed between two measured drain-to-source voltages. The peak voltages are 1090 and 1057 V, respectively with less than 4% difference.

### D. $I^2t$ Functional Test

$I^2t$  capability cannot be fully tested due to the limitation of available high current power sources in the laboratory. Therefore, only a functional test is implemented. The test circuit and platform are similar to the one used for the steady-state test. The current source can generate a current higher than the rated one for SSPC to detect and protect. The temperature of the SSPC is controlled as 75 °C to emulate the rated condition. Then the current source works to generate a high current as of the overcurrent. A protection waveform is shown in Fig. 23. The flag signal  $v_{flg}$  is set when the SSPC controller begins to accumulate the  $i^2t$  value. In this case, a 550 A overcurrent, meaning 1050 A current corresponding to the protection curve, is generated. With an expectation protection time of 88  $\mu$ s in the protection curve of Fig. 6, the SSPC triggers at 91  $\mu$ s. Note that the TVS diode in this test is changed to LTKAK10-76C with a lower clamping voltage to prevent the overvoltage of the low output voltage dc source.

### E. Soft-Start Test and Ground Fault Test

The soft-start test waveform has been given in [12]. The ground fault indicator is tested with a grounding hook to short

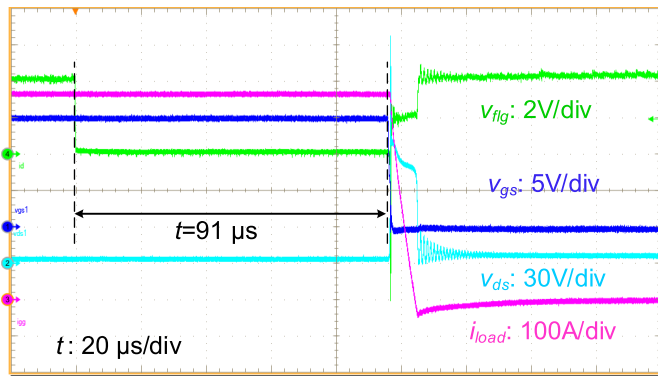


Fig. 23. Waveforms of  $i^2t$  protection.

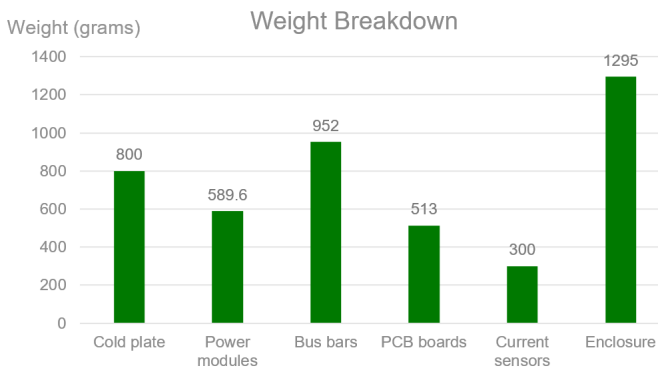


Fig. 24. Weight breakdown of the developed SSPC.

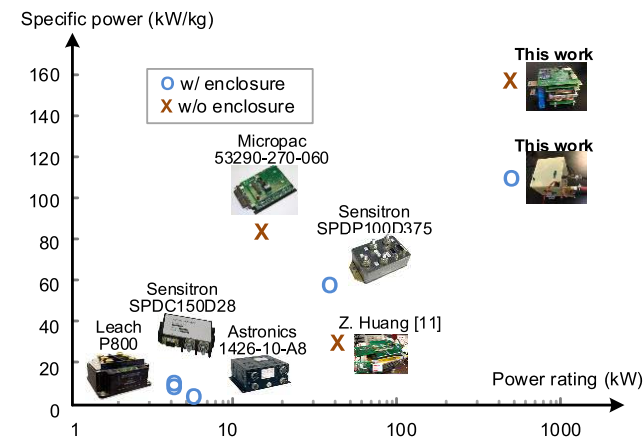


Fig. 25. Power rating and specific power comparison.

circuit the positive or negative bus to the ground. The SSPC functions to detect and indicate the fault.

*F. Weight Breakdown and Power Density Comparison*

The weight breakdown of the developed SSPC is shown in Fig. 24. The main parts of the weight are mechanical-related parts, including enclosure and bus bars. The total weight with and without enclosure is 4.45 and 3.16 kg, respectively, corresponding to specific powers of 112.4 and 158.2 kW/kg.

Fig. 25 shows the specific power and power rating comparison between the developed SSPC and other reported SSPCs with provided weight. Since the enclosure could be one of the main weight contributors, to have a fair comparison, the

weights for cases with or without enclosure are labeled in different shapes. The developed SSPC in this work shows a much larger power rating and specific power density than the state-of-the-art SSPCs. Moreover, other SSPCs in Fig. 25 are all unidirectional while the one developed in this article is bidirectional.

VII. CONCLUSION

This article presents the design and development of a 1 kV 500 A bidirectional dc SSPC for future electrified aircraft applications. The electrical design of the SSPC is presented in detail with the selection of SiC power modules and TVS diodes. The challenges of paralleling and series switches to construct high-power devices for high-power SSPCs are first identified. Paralleling multiple dies in an SSPC with small inner gate resistance for each die can cause the instability issue during the high current turn-off. This instability issue due to the immaturity of the high-power SiC power module limits the protection curve to a relatively small region, which can be overcome during the commercialization and maturation of the power module. The series of switches can benefit from paralleled TVS diodes in SSPC applications.

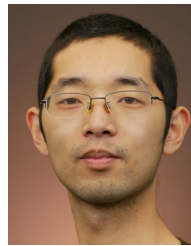
In addition, the high peak-to-average clamping ratio caused by  $Ldi/dt$  of the turn-off current commutation and foldback characteristics of high power TVS diodes is addressed. The part of overvoltage caused by  $Ldi/dt$  is minimized by paralleling lower power TVS diodes with smaller packages.

Finally, the testing setups for the high-power SSPC are presented, and all key functions are tested for the SSPC. The developed SSPC achieved an efficiency of 99.51% and a specific power of 112.4 kW/kg. The power rating and specific power are both much higher compared with state-of-the-art SSPCs thanks to the high-performance SiC power module, advanced thermal management system, limited switch voltage stress with overvoltage clamping, and compact mechanical design.

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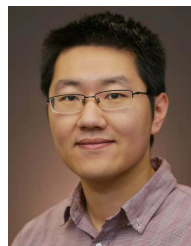
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**Zhou Dong** (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014 and 2017, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with The University of Tennessee, Knoxville, TN, USA.

His research interests include wide bandgap semiconductor device applications, electric power system protection, and design automation in power electronics.



**Ren Ren** (Member, IEEE) received the B.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2012, and the Ph.D. degree in electrical engineering from The University of Tennessee, Knoxville, TN, USA, in 2020.

He is currently a Senior Architecture/Application Engineer with Monolithic Power System, Inc., San Jose, CA, USA, with a focus on the voltage regulator module (VRM) solution for CPUs, GPUs, and application-specified integrated circuits (ASICs).

His research interests include high-frequency converter design using wide bandgap devices, design optimization and automation in power electronics, soft-switching resonant converter, and high-frequency digital control in power electronics.



**Fei (Fred) Wang** (Fellow, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1982, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, USA, in 1985 and 1990, respectively.

He was a Research Scientist with the Electric Power Laboratory, University of Southern California, from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, USA, as an Application Engineer, in 1992. From 1994 to 2000, he was a Senior Product Development Engineer with GE Industrial Systems, Salem, VA, USA. From 2000 to 2001, he was the Manager of the Electronic and Photonic Systems Technology Laboratory, GE Global Research Center, Schenectady, NY and Shanghai, China. In 2001, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, as a Research Associate Professor and became an Associate Professor, in 2004. From 2003 to 2009, he was with the CPES, Virginia Tech, as the Technical Director. Since 2009, he has been with The University of Tennessee, Knoxville, TN, USA, and the Oak Ridge National Laboratory, Oak Ridge, TN, USA, as a Professor and the Condra Chair of Excellence in power electronics, respectively. He is a Founding Member and the Technical Director of the Multi-University NSF/DOE Engineering Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee. His research interests include power electronics and power systems.

Dr. Wang is a fellow of the U.S. National Academy of Inventors.