Design and Transient Analysis of a 650 V/150 A GaN Power Modules With Integrated Bias Power and Gate-Drive Circuit

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Abstract— This article focuses on the design of a 650 V/150 A gallium nitride (GaN) power module. Direct bonded copper (DBC) is employed for the thermal pad insulation and the printed circuit board (PCB) is adopted for the flux cancellation, isolated bias power supply, and gate-drive-circuit integration. The packaged module exhibits high current capability ($>$150 A), high compactness ($45 \times 33 \times 9.6$ mm^3), and excellent thermal resistance (0.43 °C/W). The insulated drain–source and integrated isolated gate-drive circuit also facilitate the assembly of GaN devices, particularly in high-power applications. Double pulse test (DPT) at 450 V/150 A shows $\sim$50 V voltage spike only, which makes the proposed module well suited for high-power applications.

Index Terms— Direct bonded copper (DBC), gallium nitride (GaN) high electron mobility transistors (HEMTs) package, half-bridge module, integrated gate driver, isolated power supply, transient analysis.

I. INTRODUCTION

GALLIUM nitride (GaN) high electron mobility transistors (HEMTs) have been under development for decades in the power electronics domain. It enables numerous new topologies and control algorithms [1], [2], [3], thanks to its superior performance, such as ultrafast switching speed thereby ultralow switching loss. However, compared to its Si counterpart, the major roadblocks to applying GaN devices more widely include the high cost, fragile gates, exotic packaging, and difficult thermal design limited by its small footprint [4], [5], [6], [7], [8].

To improve the thermal performance of GaN devices, multiple approaches have been made from different aspects. Studies to improve the device material and physical structure lead to better thermal conductivity from the heat source to the die substrate [9], [10]. However, supreme material such as the diamond or GaN-on-GaN structure usually yields a much
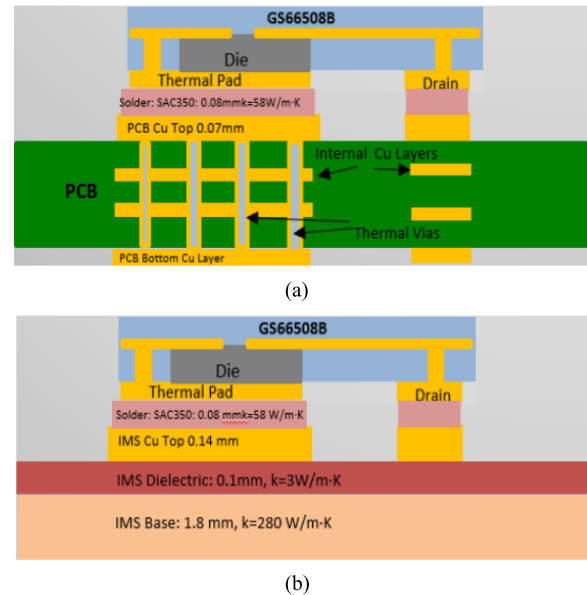
Fig. 1. (a) Bottom-cooled devices using thermal vias. (b) Bottom-cooled devices using IMS.

higher cost than GaN-on-Si design on the market nowadays. It only makes the commercialization of GaN devices even more difficult. Paralleling more dies into a single package mitigates the current unbalance [11], [12], and the thermal dissipation area is also significantly increased, but customers have to pay for the bulky size and much higher cost.

In addition to improving the thermal conductivity of the GaN die itself, it is more practical and effective to improve the overall package, i.e., the thermal impedance from the die to the case. This is particularly true since the thermal impedance of the die itself is much lower than the die-to-case thermal impedance. For example, presently both top-cool and bottom-cool packages have been developed for GaN devices. Even though the top-cool GaN device package, e.g., GaN Systems' GS66508T, exhibits low junction-to-case thermal impedance (0.5 °C/W), its thermal pad is connected to the source internally. For the sake of the electrical insulation, an extra insulated thermal interface material (TIM) is then inserted between its pad and the heatsink, yielding the overall junction to heatsink thermal impedance $>$2 °C/W [13], [14]. This in return results in a higher junction temperature, which further increases the drain-to-source resistance (R_{DSon}). The bottom cooled device can rely on the thermal vias [15], copper slugs, or insulated metal substrates (IMS) to create a thermal path to the heatsink, as shown in Fig. 1. However, note that

both the IMS and copper slugs add the system cost, GaN devices also have to be tightly soldered on top of IMS or copper slugs, which obstructs the switch replacement when damages happen.

Last but not least, both IMS and copper slugs yield poorer flux canceling compared to multilayer PCBs, given the IMS essentially is one single-layer PCB while copper slugs under the switch occupy the room for laying out traces of power supply or gate-drive circuits. The third approach is using hybrid switches (GaN+Si) to offset the high cost of GaN [16]. While finding it effective to reduce the usage of GaN with enhanced thermal capability, it does introduce more pulsewidth modulation (PWM) signals and extra gate drivers through using extra Si devices. Plus, the hybrid switch solutions usually suffer from higher parasitic inductances, which limits the module's switching speed.

Double-side cooling (DSC) is also reported in the previous literature [17], [18], [19], [20], [21]. It doubles the thermal dissipation area and yields higher thermal performance. Still, the major concern is the complex structure which makes the fabrication more costly. Note that the DSC structure does not apply to all packages of GaN devices.

Direct bonded copper (DBC) is a commonly used technology to package conventional Si power modules. GaN power modules based on DBC are also developed to compete with Si counterparts [11], [22]. The DBC exhibits good thermal performance. However, most DBC-based packages require bond wires as well, which introduces excessive parasitic inductance. Packages using hybrid DBC and PCB inherit good thermal performance from DBC and high flexibility from PCB [23], [24], [25], but the integration level is usually low. The PCB is mainly utilized for decoupling capacitors only. More potential of PCB still remains to be explored.

Integration of the gate driver with dies is another recent trend for packaging technologies, which reduces the power loop and gate-drive loop parasitics inside the power module to alleviate the electrical stress, maximize the switching speed, and minimize the negative impact from external circuits. Such integrated designs are reported in the previous research [26], [27], [28]. However, most designs ignored the isolated power supply and gate-drive circuits. Therefore, when using such modules, customers have to lay out an extra isolation layer between the power module and the given power supply, such as a 12 V onboard battery in electric vehicles (EVs). This in return introduces extra parasitics and offsets the switching performance of the devices, particularly for the GaN HEMTs which are sensitive to the loop inductance.

In summary, all present package solutions face cost challenges, not to mention some existing GaN packages only focus on one single die and lose the effective flux cancellation, resulting in high voltage spikes in the switching-off process. After thoroughly comparing the pros and cons of various packaging approaches as shown in Table I, to maximize both the thermal and switching performance of GaN devices, a flip-chip high-current (>150 A) GaN phase-leg package with low inductance, sufficient electrical insulation, low thermal resistance, and integrated gate driver is proposed as Fig. 2(b) by using GaN Systems' 650 V/150 A dies (GS-065-150-1-D)

TABLE I

COMPARISON OF VARIOUS PACKAGE STRUCTURES

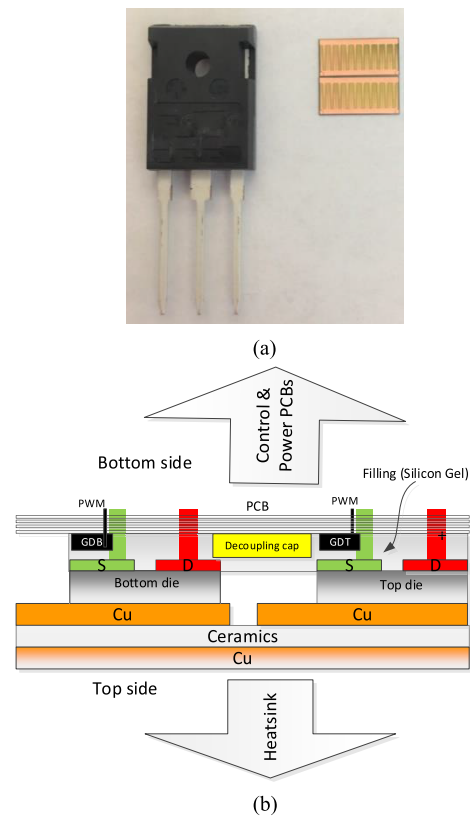| Packages	Thermal impedance	Cost	Fabrication	Parasitics
Double side cooling	Low	High	Complex	High
IMS	Middle	Middle	Middle	High
Thermal Vias	High	Low	Easy	Middle
DBC only	Lowest	Low	Easy	High
Proposed hybrid	Low	Middle	Easy	Low

(a)

(b)

Fig. 2.   (a) Si TO-247 package versus two 650 V/150 A GaN dies. (b) Proposed integrated GaN half-bridge module.

to form a half-bridge. Both DBC and multilayer printed circuit board (PCB) are adopted here. Here, DBC is used to dissipate the heat while the multilayer PCB is adopted for circuit integration (gate drivers, isolated power supply, dies and decoupling capacitors, etc.) and flux cancellation.

It is worth noting that flux cancellation is an important consideration in adopting the PCB in the module. The flux cancellation is an important method to minimize the parasitic inductance induced by the interconnection conductors between components. When the current is carried by these conductors, the flux will be induced around the connector. The longer the path, the higher the energy stored in the induced flux. In addition to shortening the routing length, which effectively reduces the parasitic inductance, putting two conductors that carry opposite direction currents also helps to cancel the flux
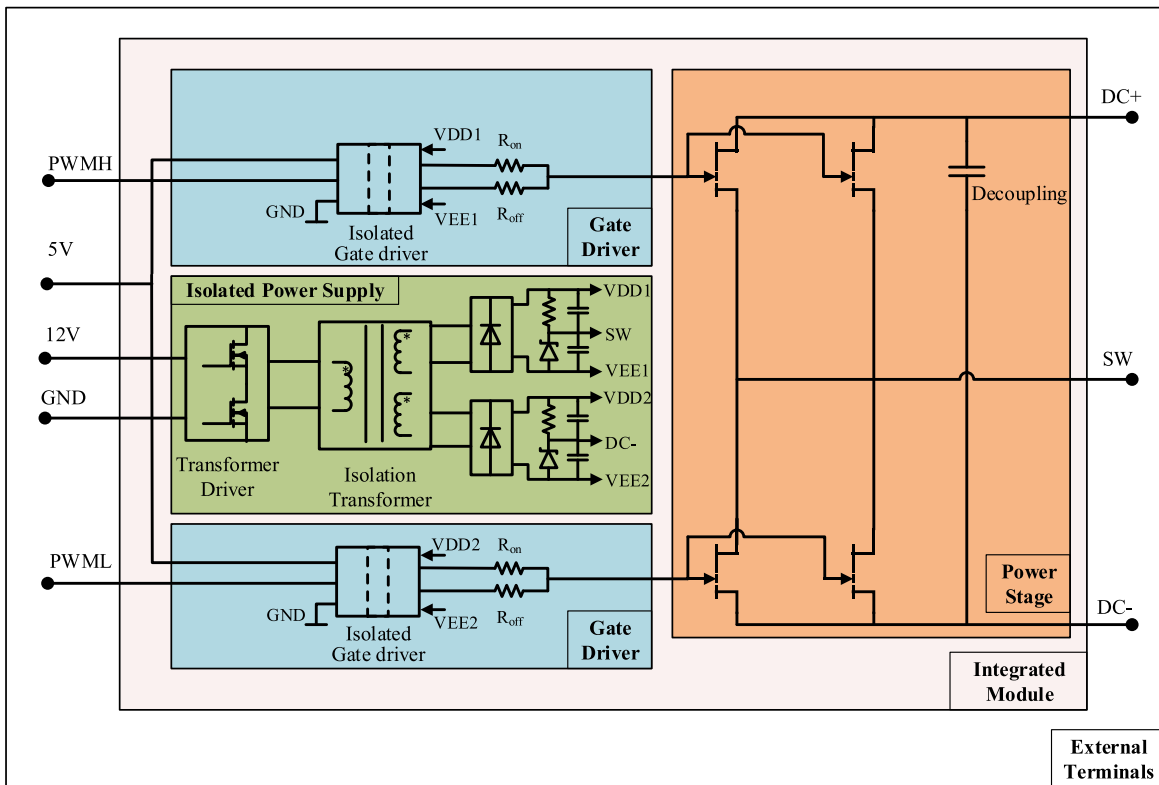
Fig. 3.   Electrical structure of the proposed integrated GaN power module.

around the conductor thus effectively reducing the overall parasitic inductance of the loop.

Due to the single-layer structure of DBC, it is difficult to put two large connectors close enough to cancel the flux, thus we proposed to use PCB+DBC hybrid structure. With the PCB, the connectors can be split into multiple layers of the PCB and the distance can be close enough to cancel the flux thus effectively reducing the parasitic inductance.

When using such power modules, users only need to provide two PWM signals from the microcontroller, and an external power supply, e.g., 12 V, which greatly facilitates the system assembly.

In this article, Section II will detail the electrical integration design, focusing on the gate-drive circuit and power supply integration. The impact of the parasitics of both gate-drive loop and power loop is quantified. Section III will discuss the thermal design, i.e., using DBC to dissipate the heat. Section IV presents the experimental results. Section V is the conclusion and future work.

II. Electrical Integration and Transient Analysis

A. Electrical Integration

To minimize the cost and make the proposed power module compact and ready to use, this article attempts to integrate most of the auxiliary circuits, such as the isolated power supply and the gate driver circuit into the power module. The high-level electrical schematics of the proposed integrated half-bridge module are shown in Fig. 3.

Here, multiple layers are shown. The outer layer involves the external terminals of the designed power module, which include two PWM signals, and non-isolated power supplies of 5 and 12 V. The 5 V power supply is used to power the primary side of the isolated gate driver, a 2.2~5.5 V wide input voltage range is acceptable. The 12 V power supply is used for the gate drive secondary side to generate the +6/−3 V gate-driving voltages. The power requirement of gate drivers is low and the output voltage of the isolated power could stay stable even though it is unregulated. Such power supplies are commonly used and readily available. For instance, the 12 V power supply can directly come from the low-voltage lead-acid battery inside EVs.

Inside the power module, the power stage parallels two GaN Systems' 650 V/150 A dies (GS-065-150-1-D) to enhance the power capability and thermal dissipation areas. Four such dies together are then configured as a half-bridge with decoupling capacitors equipped. Therefore, such a power module is rated as 650 V/300 A, though in actual practice, we might lower the current flowing through. Two isolated gate-drive circuits are then included inside the power module for both the high-side and low-side switches to provide full isolation between the power stage and the control stage, for the sake of the safety requirement and common-mode noise rejection.

Different from other preexisting power modules, the proposed power module also integrates an isolated power supply, as shown in Fig. 3 marked as the green region. It is composed of the transformer driver and a three-winding transformer, which provides the electrical isolation for both the high-side switches and low-side switches. A voltage splitter utilizing Zener diodes generates a negative voltage (VEE) to reliably turn off the switches, thereby reducing the possibility of false triggering. The detailed structure of the isolated power supply is shown in Fig. 4 and the bill of the materials is given
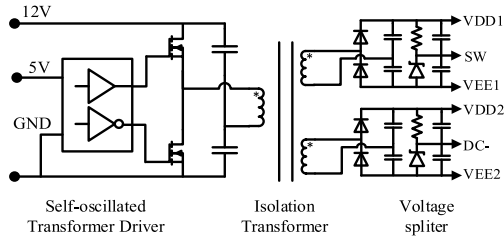
Fig. 4.   Isolated power supply design.

TABLE II
BILL OF MATERIALS, MAIN COMPONENTS

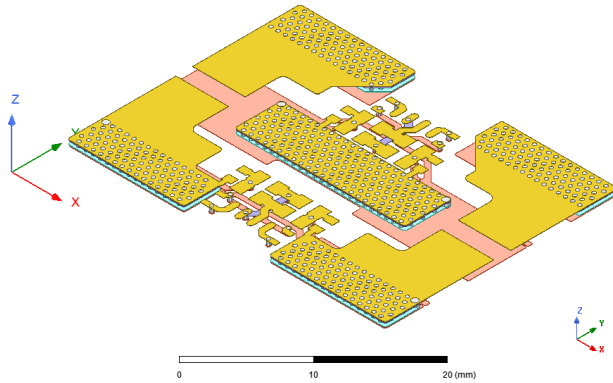| Component	Part Number
Transformer Driver	IR21531STRPBF ×1
Isolated Gate Drive	Si8271AB ×2
Isolated Transformer	760301105 ×1
12V output capacitors	C1608X5R1E106 ×8
12V half bridge	2N7002DW-7-F
Decoupling capacitor	C3225C0G2J223K230AA ×8
GaN bare die	GS-065-150-1-D ×4

Fig. 5.   PCB model imported in ANSYS Q3D.

in Table II. Such a simple structure makes the design more affordable, reliable, and compact.

B. Power-Loop Parasitics and Related Transients

Parasitic inductances and high di/dt of GaN HEMTs yield possible voltage spikes during switching transients. The PCB was adopted to accommodate the decoupling capacitors and facilitate the flux canceling to further minimize the parasitics.

To quantify the parasitics inside the power module, ANSYS Q3D is employed, with the PCB model imported shown in Fig. 5.

The drain-to-source voltage V_{ds} and the gate-drive voltage V_{gs} spikes are key considerations in the power module design. Thus, parasitics of both the gate-drive loop and power loop are extracted from the Q3D model, as summarized in Fig. 6. Given the parasitics of the die itself are already embedded in the SPICE model and the die also has a Kevin connection for
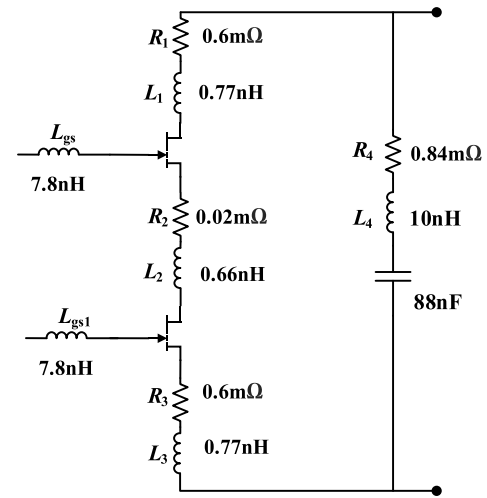

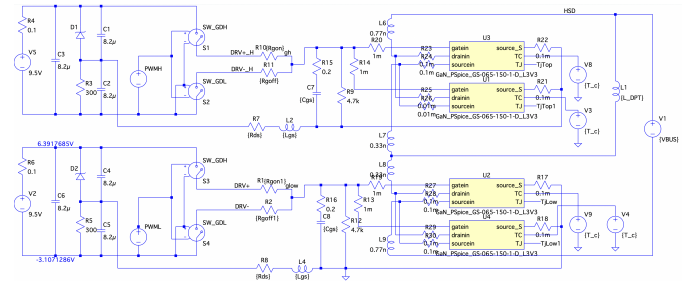Fig. 6.   Parasitics of the proposed power module.

Fig. 7.   Simulation model with parasitics.

the gate, the common-source inductance of the GaN HEMT can be ignored.

To further evaluate the impact of parasitics, an LTspice model with all parasitics above is built in Fig. 7. To simplify the simulation, the gate-drive power supply is replaced by a voltage source with certain internal resistance. The GaN model is provided by GaN Systems.

The V_{ds} spikes are related to power loop inductances, i.e., L_1–L_3 shown in Fig. 6, when GaN HEMTs are switching off. Although such parasitic inductance is already minimized in the PCB layout as shown in Fig. 8, it still cannot be eliminated. Hence, certain voltage spikes still happen, as plotted in Fig. 9. The simulated voltage spike is ∼50 V when the dc bus voltage is 450 V and the switching current is 150 A, which will be verified by experiments later.

C. Gate-Loop Parasitics and Related Transients

The gate-loop traces are designed in a symmetric way for the paralleled HEMTs. The trace lengths for the top GaN 1 and top GaN 2 are measured as 10.08 and 10.15 mm, respectively, which translated to 7.81 and 7.84 nH loop inductance, respectively. The 0.03 nH difference can be safely ignored when compared to the overall 7.8 nH loop inductance. Due to the small die size, the C_{gs} of the GaN HEMTs are trivial (216 pF) as well. Even assuming a 10% mismatch between the R_{on}/R_{off} of the paralleled devices, the falling/raising edges mismatch is less than 0.5 ns. Compared to the >25 ns total rising/falling time, the mismatch can be ignored.
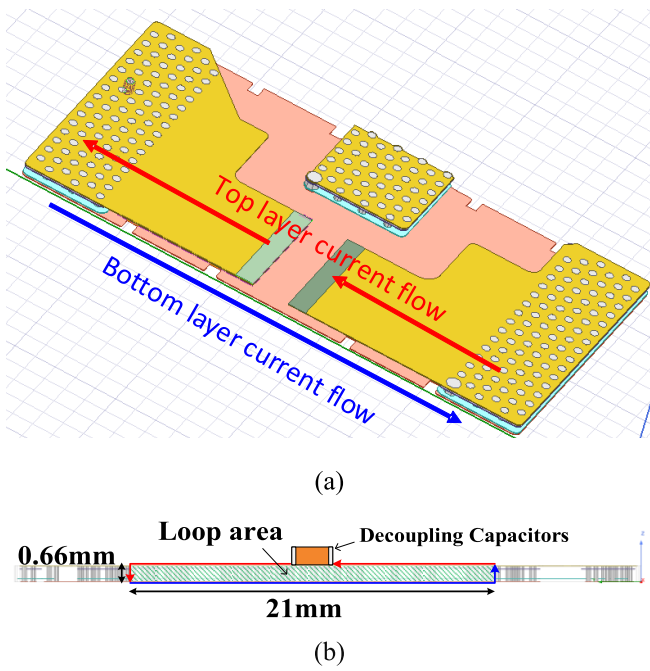
Fig. 10. Simulated V_{gs} undershoot and overshoot spikes.

Fig. 8. PCB layout showing flux canceling loop (a) isometric view and (b) sectional view.
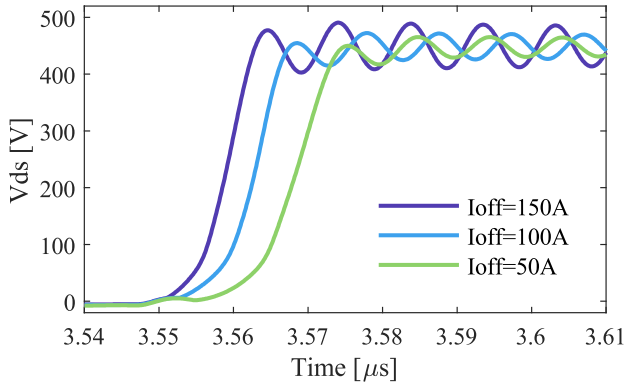
Fig. 9. Simulated waveform showing spikes of V_{ds}.

Fig. 11. Gate-drive loop transients during soft turning-on.
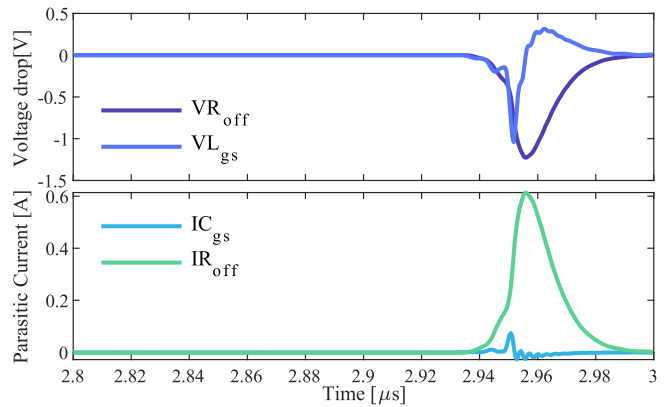
Fig. 12. Key components of gate undershoot voltage spikes.

Though the gate loop is designed in a short and symmetric way, the gate-drive loop still exhibits some parasitic inductances from the PCB layout, as well as the capacitance from the devices themselves. When these parasitics are engaged, both V_{gs} overshoot and undershoot spikes could occur, as simulated in Fig. 10. Due to a much narrower gate-drive voltage margin for GaN HEMTs compared to Si or SiC, V_{gs} spikes are even more critical for the device's safe operation than V_{ds} spikes. For example, the undershoot spike is possible to damage the gate oxide, and the overshoot spike is likely to falsely trigger the switch. To understand the reason for these spikes and guide the gate-drive loop circuit design, a detailed transient analysis with related design criteria will be discussed as follows.

First, a V_{gs} undershoot is possible prior to the turn-on transient, as shown in Fig. 10. The detailed transient process is illustrated in Fig. 11. During the dead time, the low side switch is turned off and the high side switch is not turned on yet. The load current is commutated from the low side switch to the high side one. Note the load current not only
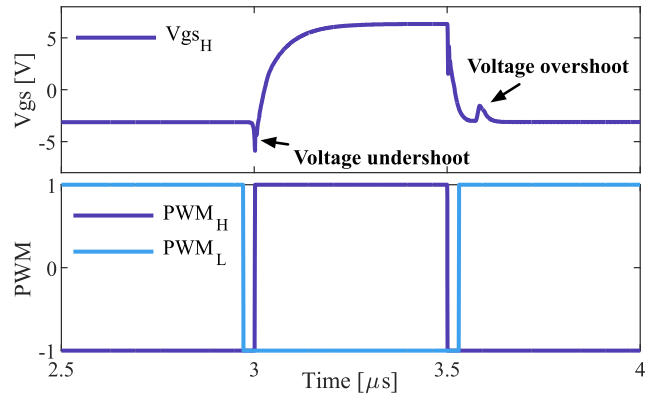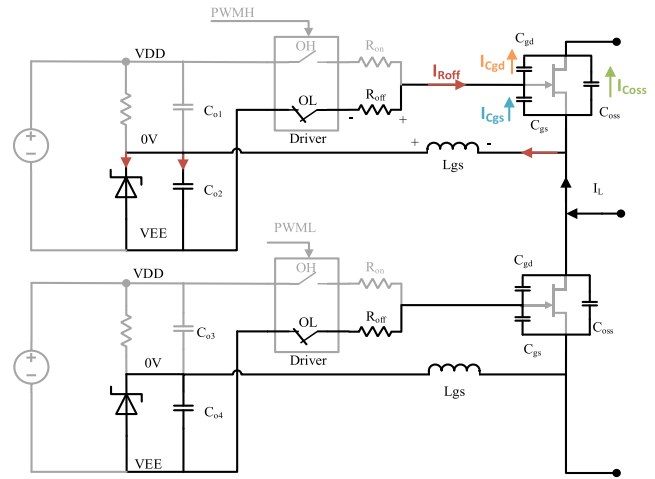
discharges the output capacitance C_{oss} of high side switch for ZVS, but also flows into the gate-drive loop as I_{Roff} and I_{Cgs}, which are noted as parasitic currents and marked with red and blue arrows in Fig. 11, respectively. These two currents then combine and flow through the reverse capacitance C_{gd} as I_{Cgd}. However, since the input capacitance C_{gs} (nF level) is way smaller than the power supply output capacitor C_{o2} (μF level), I_{Cgs} is negligible compared to I_{Roff}, as shown in Fig. 12. Thus, we can assume $I_{Roff} \approx I_{Cdg}$ for simplified analysis.
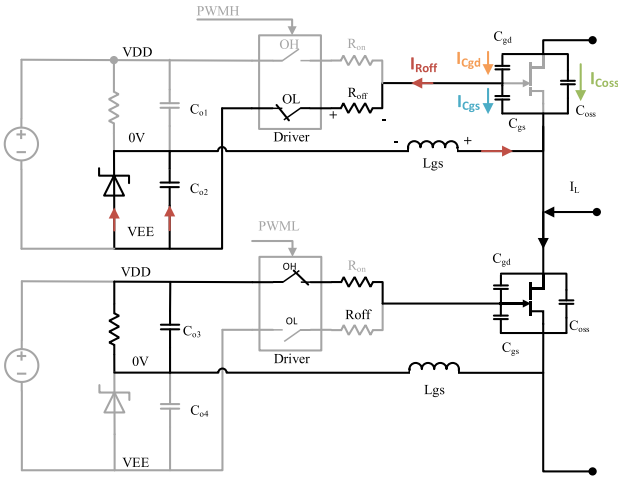
Fig. 13.   Gate-drive-loop transients during hard turning-on.

Fig. 14.   Key waveform during switching off transient.

When $I_{R\text{off}}$ flows through the parasitic current path marked with red arrows in Fig. 11, there will be voltage drops across both R_{off} and L_{gs}. The voltage polarity is shown in Fig. 11 with the plus/minus signs, and the value is simulated in Fig. 12 for a 2 Ω R_{off} and a 7.8 nH L_{gs}. Note that the $I_{R\text{off}}$ is a pulse current, thus it also disturbs the voltage of the power supply output capacitor C_{o2}, which is as follows:

$$V_{C_{O2}} = \frac{1}{C_{o2}} \int_0^t I_{R\text{off}} dt + \text{VEE}. \tag{1}$$

When the selected C_{o2} are large enough, the transient $I_{R\text{off}}$ actually has few impacts on the capacitor voltage and a stable $V_{C_{o2}} \approx \text{VEE}$ is much expected. However, the voltage drop $V_{R\text{off}}$ across R_{off} and $V_{L\text{gs}}$ across L_{gs} greatly depends on the gate-loop circuit design and cannot be ignored. The voltage drops add to the VEE as the gate-to-source voltage V_{gs}. Ultimately, V_{gs} that contains the components contributed by the parasitics is given in the following equation, which implies the existence of V_{gs} undershoot voltage spike:

$$V_{\text{gs}} = -\text{VEE} - I_{R\text{off}} R_{\text{off}} - \frac{dI_{R\text{off}}}{dt} L_{\text{gs}}. \tag{2}$$

Second, Fig. 10 also indicates a possible V_{gs} overshoot spike of the high-side switch when the complementary switch is hard turning on. The detailed transient process is depicted in Fig. 13. Before the spike happens, both the high side-switch and the low-side switch are securely turned off during the dead time, the load current is freewheeling through the high-side switch two-dimensional electron gas (2DEG), and the V_{ds} of the high-side switch is zero. During the hard turning-on transient of the low-side switch, the load current commutates from the high-side switch 2DEG to the low-side channel, which induces a high dv/dt on the V_{ds} of both switches. Due to the existence of parasitic capacitance such as the C_{oss} and C_{gd}, this high dv/dt generates similar transient currents $I_{C\text{oss}}$ $I_{C\text{gd}}$ as discussed, however, in the opposite direction. The corresponding current paths are marked in Fig. 13.

The current $I_{C\text{oss}}$ is supplied to charge the output capacitance of GaN HEMTs to build up V_{ds}, which is always equal to $V_{C\text{gd}} + V_{\text{gs}}$. Even though V_{gs} contains certain voltage spikes, compared with the dc bus voltage the whole V_{gs} can be
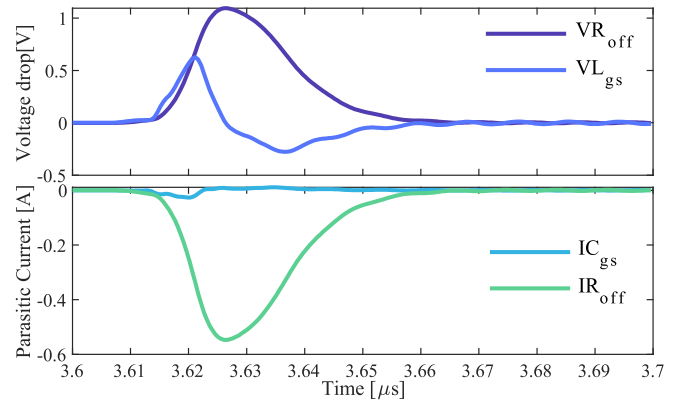
ignored. Thus, we can assume $\Delta V_{\text{gd}} \approx \Delta V_{\text{ds}}$ in the charging process. Furthermore, considering that C_{o2} is much larger than C_{gs}, the $I_{C_{\text{gs}}}$ is also ignorable. The simplified $I_{R_{\text{off}}}$ is then only related to the dv/dt of V_{ds} and can be written as follows:

$$I_{R\text{off}} = \frac{dV_{\text{ds}}}{dt} C_{\text{gd}}. \tag{3}$$

Note that here (dV_{ds}/dt) is mainly determined by the switching speed of the complementary switch. Similar to the voltage undershoot in (2), the absolute value of the V_{gs} overshoot can be written as follows:

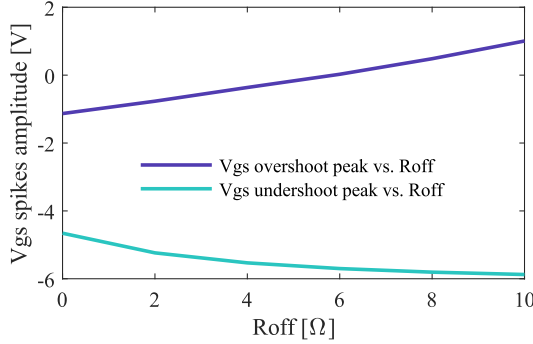$$V_{\text{gs}} = -\text{VEE} + I_{R\text{off}} R_{\text{off}} + \frac{dI_{R\text{off}}}{dt} L_{\text{gs}}. \tag{4}$$

From (4), it is clear that the parasitic current will impair the stable negative VEE and induce a voltage overshoot. One example showing the transient parasitic current and voltage drops during the V_{gs} overshoot is given in Fig. 14, for a 2 Ω R_{off} and a 7.8 nH L_{gs}.

D. Gate-Drive Loop Design Considerations

The gate voltage overshoot and undershoot spikes are both induced by the parasitic gate-loop current, however, the origins of the current are different. The voltage undershoot is caused by the parasitic current that results from the commutation of the load current, which is determined by the turn-off speed of the complementary switch. The voltage overshoot spike, however, is induced by the dv/dt of parasitic C_{gd}, and is highly dependent on the turn-on speed of the complementary switch.

In terms of the parasitics involved, the voltage undershoot is related to the R_{off} of both the device under test (DUT) and the complementary switch. The voltage overshoot spike, on the other hand, is related to R_{off} of the DUT and R_{on} of the complementary switch. It is worth noting that this statement assumes that the parasitic inductance is constant.

Nevertheless, the analysis suggests all the voltage spikes are related to the gate-loop impedance and the turn-on/turn-off speed of the GaN devices, while the major part of the gate-loop impedance is the gate resistance, and the turn-on/turn-off speed is mostly controlled by the external gate driving resistance. Therefore, the selection of gate resistance is the key to optimizing the gate voltage spikes.
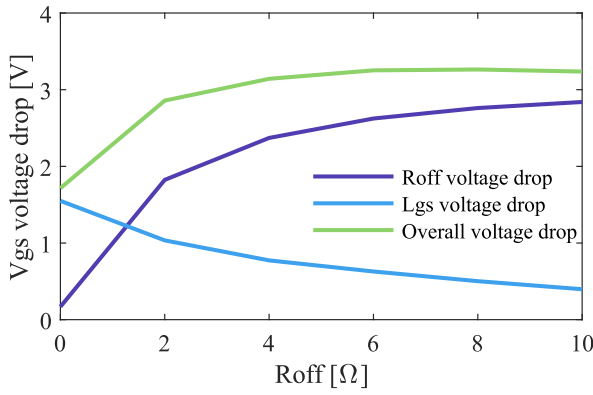
Fig. 15. Voltage drops on gate-loop impedance versus R_{off}.

Fig. 16. V_{gs} spikes amplitude versus R_{off} @$R_{on} = 3$ Ω.

Fig. 17. V_{gs} spikes amplitude versus R_{on} @$R_{off} = 2$ Ω.

Fig. 18. V_{ds} spike versus R_{off}.
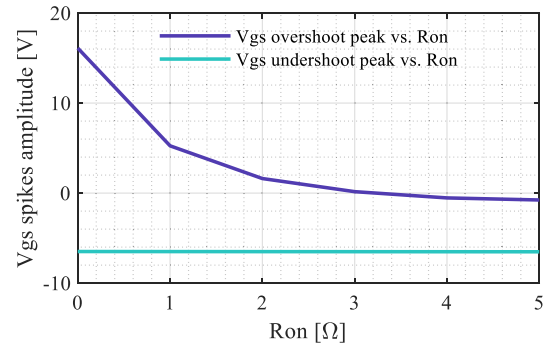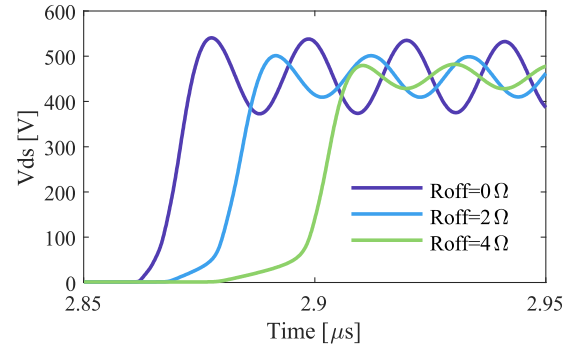

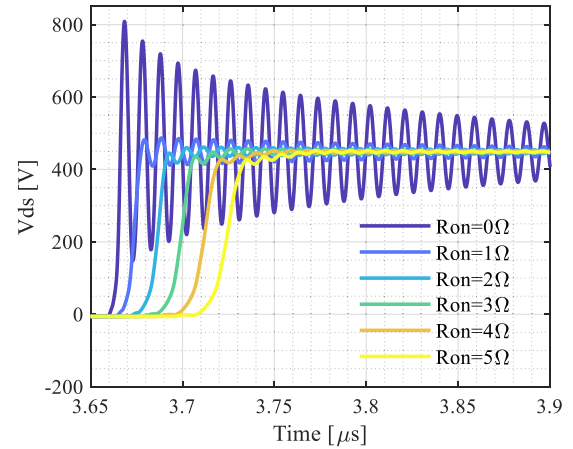Fig. 19. V_{ds} spike versus R_{on}.

A smaller R_{off} leads to a lower voltage drop on the gate resistor itself, but elevates the parasitic current and voltage drop on the parasitic gate-loop inductance. Conversely, a larger R_{off} slows down the switching speed and reduces the parasitic current, but it does not necessarily reduce the voltage drop on R_{off} itself. An example showing how the R_{off}-related voltage drop on the gate resistors and on the parasitic leakage inductances is illustrated in Fig. 15.

Therefore, an optimal gate resistance minimizes the overall voltage drop on the resistor and parasitic inductance. The simulation results, depicted in Figs. 16 and 17, demonstrate how the overall undershoot and overshoot spikes vary with the gate resistance, where a smaller gate resistance generally leads to lower overall spikes due to the already small gate-loop inductance. However, this is only the case when the parasitic loop inductance is not dominant. When the parasitic inductance presents a higher impedance than the gate resistance, the selection of R_{off} can vary.

Furthermore, even in the case where a smaller gate resistance yields lower voltage spikes, it also leads to a faster switching speed, which in turn may result in excessive V_{ds} spikes. The simulation results in Figs. 18 and 19 show the relationship between R_{off}, R_{on} and V_{ds} spikes, respectively. In addition, a 0 Ω gate resistance presents minimal damping to the possible V_{gs} oscillation, which may worsen the V_{gs} spike as shown in Fig. 20.

In addition, Fig. 20 also indicates the gate resistance cannot be too large, otherwise, it will greatly delay the falling edge of V_{gs}. Then the overshoot may happen before V_{gs} drops to VEE, and leads to a significant increment of V_{gs} overshoot.

Concluded from the analysis above, the selection of the gate resistance is crucial in optimizing voltage spikes. The major design considerations are summarized as follows: 1) an optimal gate resistance should balance the voltage drop on the gate resistor and parasitic inductance; 2) the optimal gate resistor may vary with the impedance of the parasitic inductance; and 3) smaller gate resistance may lead to lower voltage spikes, but excessive V_{ds} spikes may occur if the gate resistance is too small.

R_{on} and R_{off}'s selection is the result considering both V_{gs} overshoot/undershoot spike and V_{ds} spikes, together with the consideration of the devices' switching losses. In detail: 1) the V_{gs} undershoot is only related to the R_{off}, while the V_{gs} overshoot is related to both R_{on} and R_{off}. The 3 Ω R_{on} and 2 Ω R_{off} limit the max undershoot with −10 V, and at the same time limit the overshoot under 0 V to avoid mis-triggering and 2) the impact of R_{on} and R_{off} on the V_{ds}
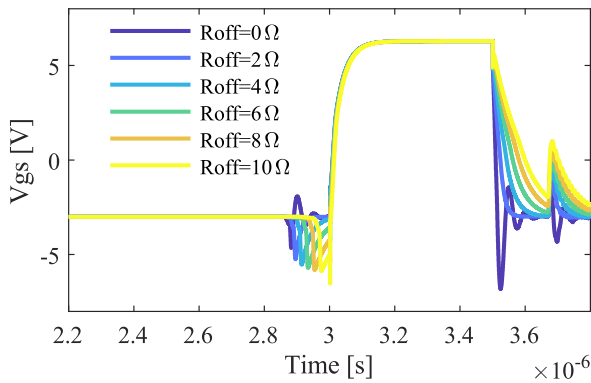
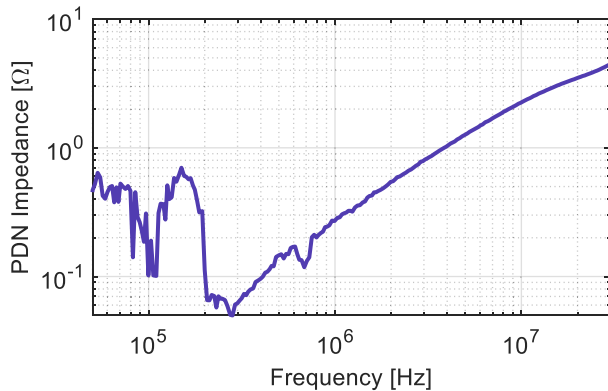Fig. 20. V_{gs} spikes versus R_{off}, dead time $=150$ ns.

Fig. 21. PDN plots with parasitics.

spikes and switching losses: the V_{ds} spikes are related to both R_{on} and R_{off}. The 3 Ω R_{on} and 2 Ω R_{off} present an acceptable spike voltage, at the same time, the relatively low R_{on} and R_{off} also mean relatively low switching losses. With the selected R_{on}, R_{off}, and parasitics, the system PDN plot is given in Fig. 21.

III. PHYSICAL AND THERMAL STRUCTURE DESIGN

A. DBC Design

A thin layer of ceramics is sandwiched between two copper layers, as shown in Fig. 22 to form the DBC. In this way, all G, D, and S terminals of GaN devices are insulated from the heatsink. The bottom layer of the DBC serves exclusively for thermal dissipation, and the use of thermal grease can further enhance the contact between the DBC and the heatsink. Although the additional thermal grease may result in some increment of thermal impedance, it still offers a lower thermal resistance compared to state-of-the-art (SoA) TIMs, which typically exhibit thermal resistance of $\sim$1 °C/W. Thermal simulation results with a power loss of 5 W per die are shown in Fig. 23.

The simulated thermal resistance of each layer is concluded in Table III. Although the thermal resistance of the grease is a major player, it actually fully reveals the advantage of the DBC design. Overall, the simulated substrate-to-heatsink thermal resistance is around 0.4 °C/W.

B. PCB and Assembling

The gate driver and isolated power supply are located on a separated PCB with the decoupling capacitor to form
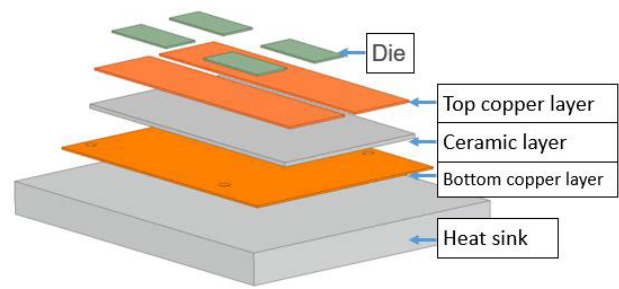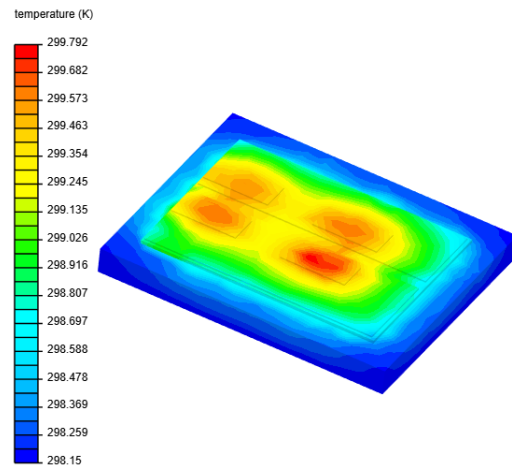

Fig. 22. Physical structure of the DBC design.

Fig. 23. Thermal simulation.

TABLE III
SIMULATED THERMAL IMPEDANCE

Layer	Thermal impedance
Soldering	0.06 °C/W
Top copper	0.04 °C/W
Ceramic (AlN)	0.16 °C/W
Bottom copper & thermal grease	0.12 °C/W

the flux-canceling loop to minimize the potential parasitic inductance. In addition, the gate-drive circuit of the top and bottom switches (GDT and GDB, respectively), including the needed power supply are soldered on this PCB. Only PWM signals for top and bottom switches, i.e., PWM/T and PWM/B are provided by the control system. All connectors of this smart PCB will be directly assembled on this PCB as well. Compared to bottom-cooled devices using the IMS, the proposed package adopts a four-layer PCB to realize the flux cancellation. Compared to discrete switches, soldering dies in one package to form a half-bridge yields much higher compactness. The overall view of the assembled power module is shown in Fig. 24.

IV. EXPERIMENTAL RESULTS

The PCB board with four GaN dies is illustrated in Fig. 25(a) and (b). All the components except four GaN dies are populated on the top layer of the PCB. Fig. 25(c) shows the
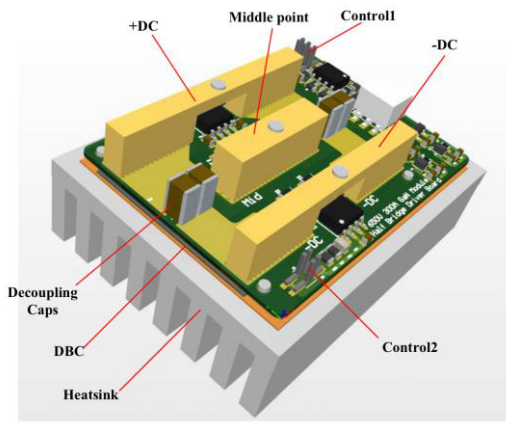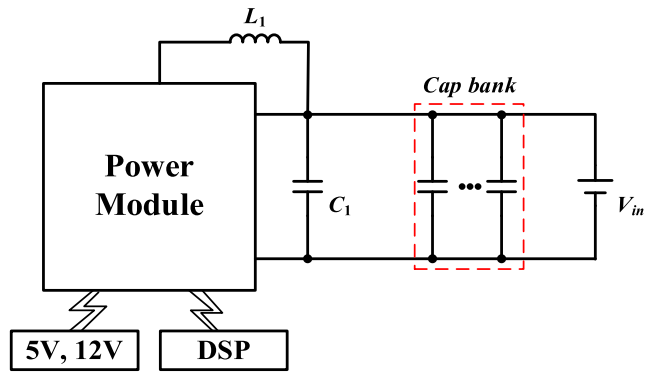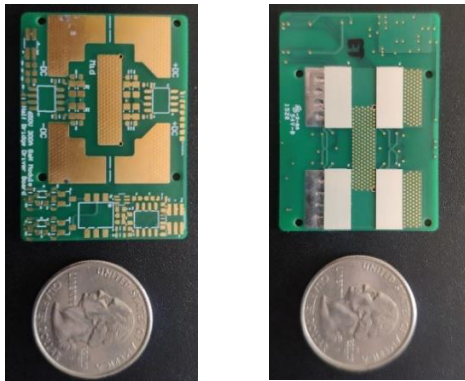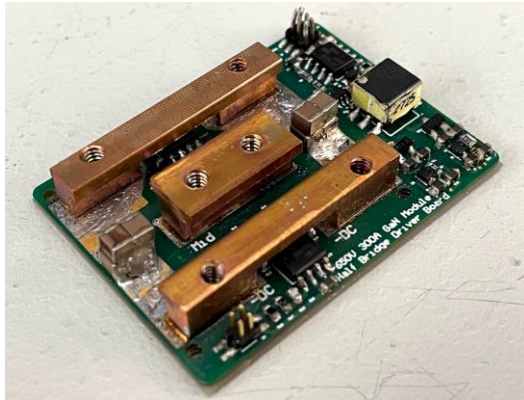
Fig. 24.   Overall module layout.

Fig. 25.   GaN power module: (a) top-layer PCB, (b) bottom-layer PCB, (c) overall power module.

Fig. 26.   DPT setup diagram.

TABLE IV
PARAMETERS OF DPT SETUP

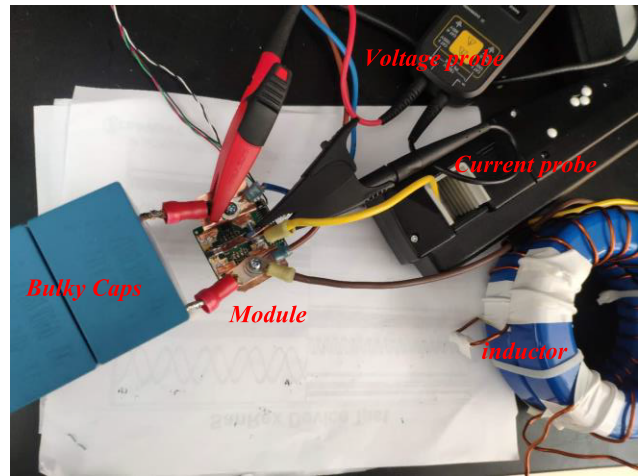| Component	Part Number	Value
L_1	N/A	61μF
C_1	C4BTHBX5200ZANJ	20μF
Cap bank	B32798G2756K	6*75μF

Fig. 27.   DPT test setup.

TABLE V
TESTED THERMAL IMPEDANCE FROM CASE TO HEATSINK

Loss per die/W	Die/°C	Heatsink/°C	ΔT/°C	R_{th}/°C/W
6.9	58.1	55.1	3	0.434
9.4	67.5	63.5	4.0	0.425
12.5	78.6	73.4	5.2	0.416

completed power module, which integrates all the necessary circuits, bus bars, dies, and DBC.

A double pulse test (DPT) was adopted to examine the switching performance of such an integrated power module, as shown in Fig. 26. The external capacitor C_1 is mounted outside the power module, which can help to stabilize the input voltage of the power module. The detailed parameters are provided in Table IV. Besides components in the power loop, the power module only requires external inputs of 5/12 V bias power and PWM signals, demonstrating its simplicity and ease of use.

The DPT test set up is shown in Fig. 27. The DPT result is shown in Fig. 28(a). The drain to source voltage of the bottom switch and the inductor current are measured. According to Fig. 28(b), when switching off ∼150 A, the overshoot voltage under 450 V input voltage is only 54 V, aligned with the simulation results. This improvement is attributed to the integration of decoupling capacitors within the power module, leading to a reduction in the loop inductance.

TABLE VI
COMPARISON OF POWER LOOP INDUCTANCE

Reference	Tested ratings	Power loop Inductance (nH)	Thermal impedance (W/°C)
[24]	400V/60A	0.91	0.38
[25]	400V/70A	3.37	Null
[26]	400V/15A	2.65	2.4
[29]	400V/60A	1.3	3.2
[30]	100V/360A	5	Null
This work	450V/150A	0.77	0.43

which contributes significantly to the thermal impedance as demonstrated in Table III. When assuming a thickness of 0.14 mm for the thermal grease instead of the typical value of 0.1 mm, the calculated thermal impedance would be 0.426 °C/W, which is much closer to the measured value.

V. CONCLUSION

An integrated GaN HEMTs half-bridge power module using 650 V/150 A bare dies is proposed in this article, aiming at the high thermal conductivity, low parasitics, and full integration of the gate drivers and isolated power supplies. The electrical architecture of the power module is designed with a focus on high integration and ease of implementation in real-world circuits. The parasitics of the gate-drive loop and power loop have been thoroughly analyzed to ensure optimal selection of the gate-drive resistance for the safe operation of devices. The adoption of the DBC approach in the thermal design eliminates the need for the TIM layer, resulting in improved thermal performance. Simulation and experimental results have verified that the thermal impedance of the proposed module is as low as 0.4∼0.5 W/°C from the substrate to the heatsink, which represents a significant improvement compared to SoA GaN packages that need TIM. The compact design of the module also results in low voltage spikes, making it an attractive candidate for high-power applications, such as battery chargers or inverters for EVs. The packaged module has been tested at 450 V/150 A and the key specifications compared with the SoA designs are summarized in Table VI.
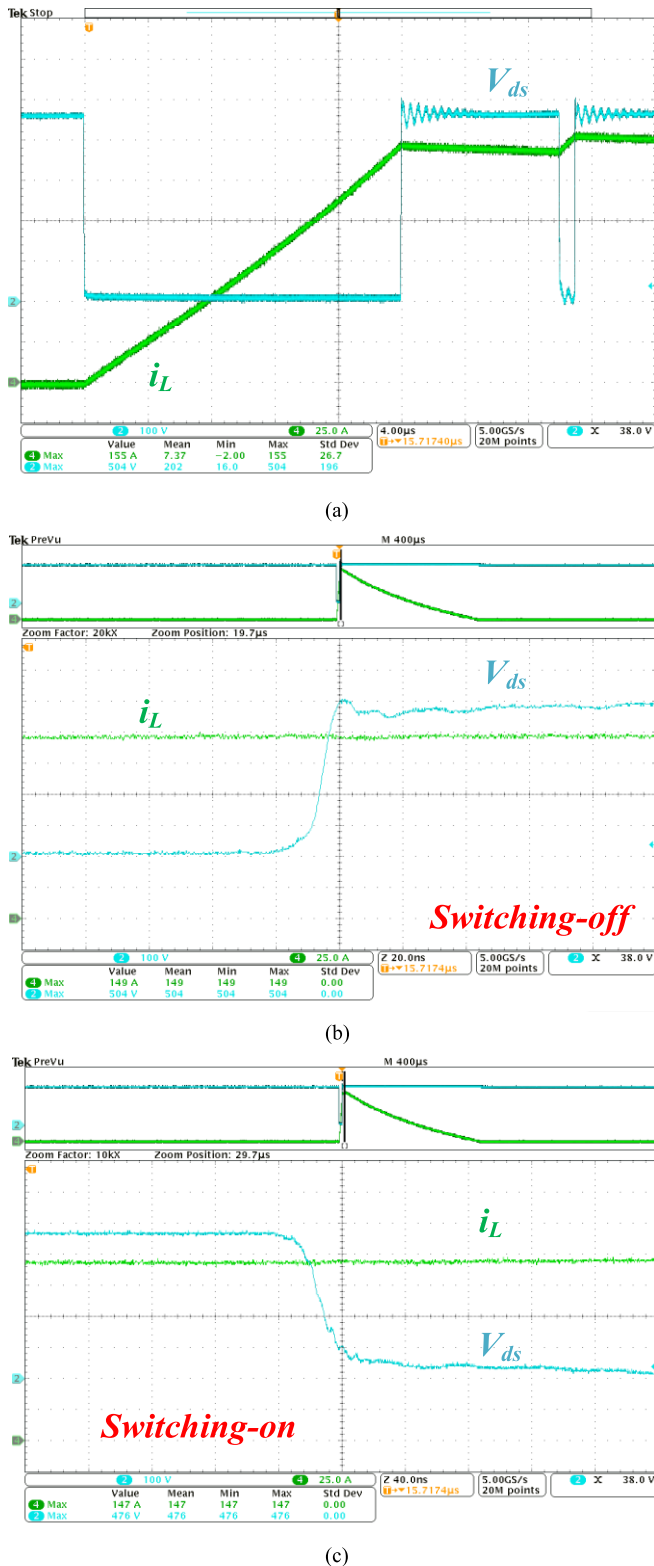
Fig. 28.   (a) DPT result at 450 V/150 A. (b) Turn-off transients. (c) Turn-on transients.

Furthermore, the thermal performance was evaluated by reversely conducting GaN devices. The results presented in Table V indicate that the thermal impedance from the case to the heatsink is approximately 0.43 °C/W, slightly higher than the simulated results of 0.39 °C/W. One possible explanation for this discrepancy is the thickness of the thermal grease,

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