Model and Control of a Current-Fed Dual Active Bridge Based Ultrawide-Voltage-Range Auxiliary Power Module for 400 V/800 V Electric Vehicles

Liyan Zhu, *Member, IEEE*, Hua Bai, *Senior Member, IEEE*, and Alan Brown

***Abstract*—As the counterparts of alternators, the auxiliary power modules (APMs) in electric vehicles (EVs) play an irreplaceable role in bridging the high-voltage (HV) propulsion system with the low-voltage (LV) auxiliary system. With the increasing demands of fast charging, the HV propulsion system is seeing an evolution from the 400 to the 800 V system. Adapting to such trends, the APM faces the challenge of a much wider input voltage range, particularly in EVs with a reconfigurable battery pack. This article proposed a reconfigurable current-fed dual active bridge (CFDAB) based converter. It accepts a record-wide input voltage from 180 to 900 V and an output voltage from 6 to 16 V. The closed-form solutions of switching current are with consideration of coupled inductor current, the key characteristics of CFDAB, and simple control to secure zero-voltage switching and minimize the switching current. Design implementation is also discussed in this article. A 3-kW prototype with a peak efficiency of 97% was built and tested. The experimental results proved the feasibility of using the proposed topology and control for the ultrawide APM applications.**

***Index Terms*—Auxiliary power module (APM), current-fed (CF) dc–dc converter, dual active bridge, electric vehicles (EVs).**

I. Introduction

THE auxiliary power module (APM) is a crucial part of electric vehicles (EVs). It receives the input from the high-voltage (HV) battery to charge the low-voltage (LV) battery and supports LV loads, e.g., the headlights, sensors, and power steering systems. Two significant challenges exist in the APM design. The first is the wide input and output voltage range. For example, the terminal voltage of an HV battery rated at 400 V can vary from 180 to 450 V [1], while an 800 V battery can have a terminal voltage from 500 to 900 V [2]. Furthermore, nowadays the EV powertrain is witnessing an increasing voltage level from 400 to 800 V for two major advantages: First, the faster charging speed. With higher battery voltage, the charging current and conduction losses could be reduced; second, the higher propulsion power. The 800 V battery voltage also implies higher power capability than 400 V and less conduction loss for given power. However, the EV charging stations for the 800 V system are still not widely installed yet. As a compromise, a 400 V/800 V reconfigurable battery pack has been reported to be a potential technology for EV applications recently [3]. Inside the battery pack, multiple strings exist and can be reconfigured in series or in parallel via switch arrays, as shown in Fig. 1. It can be configured as 400 V during charging for better compatibility and can be configured as 800 V during driving to improve the drive capability.

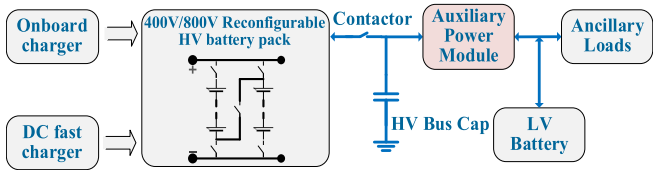

Fig. 1. Structure of EVs with reconfigurable battery packs.

Although the battery is only configured as 400 V during the charging process, it is still necessary for APM to cover the full voltage range for two reasons: First, LV loads still working during the charging process, which may drain the LV battery during the charging process of HV battery; second, the automotive industry is actually using lower capacity 12 V batteries in EVs [4], [5] and is trying to develop EV architecture without LV batteries [6], [7], [8], [9]. Thus, the APM then needs to power the LV system in a much wider input voltage range due to different battery configurations [10], [11], [12], e.g., 180–900 V, as well as a wide output voltage, e.g., 6–16 V [13], [14]. The second challenge is the high output current. Due to the low output voltage, the APM usually suffers from high current stress at the LV side. For instance, a 3.5 kW output at 12 V represents an output current of up to 300 A.

Multiple modified topologies are proposed to widen the range of the voltage gain. Modified *LLC* converters with additional control variables, e.g., the phase-shift control or duty cycles, are investigated in [15], [16], [17], and [18]. Although gaining more control freedoms for a wider operating voltage range, such effort suffers higher switching current or complex control. The partial power regulation concept is also implemented in [19] and [20] to handle the wide voltage range. The converters adopted two

Manuscript received 26 May 2023; revised 1 September 2023 and 26 October 2023; accepted 22 November 2023. Date of publication 29 November 2023; date of current version 26 January 2024. Recommended for publication by Associate Editor M. Shen. *(Corresponding author: Hua Bai.)*

Liyan Zhu and Hua Bai are with the Department of Electrical Engineering and Computer Science, Tickle College of Engineering, University of Tennessee, Knoxville, Knoxville, TN 37996 USA. (e-mail: liyanz@vt.edu; hbai2@utk.edu).

Alan Brown is with the Hella Electronics Center, North America, Northville, MI 48168 USA. (e-mail: alan.brown@hella.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3337712.

Digital Object Identifier 10.1109/TPEL.2023.3337712

stages to deal with power capability and voltage range separately, which need more switches and magnetic components. For the wide-voltage-range and high-power applications, the partial power processing unit will have to deal with a higher portion of overall power, which diminishes its advantage. Other literature proposed modifying the resonant tank or the rectifier stage for a wider voltage range [21], [22], [23], which usually needs more passive components, such as capacitors, inductors, and transformers thereby adding to the cost.

High-power requirements make achieving a wide voltage range even more challenging. The APM designs that are based on the conventional *LLC* [24], [25], [26] or dual active bridge (DAB) [27], [28], [29], [30] struggle to simultaneously support a wide voltage range and deliver high output current. The need to handle heavy loads across a broad voltage range often leads to impractical hardware parameters or high switching currents. To improve the power capability within a wide voltage range, the authors in [31], [32], [33], and [34] presented two-stage designs. One buck stage is used to regulate the voltage, and another dc-transformer (DCX) stage is used to deal with high currents. However, more stages mean more components and lower efficiency. Furthermore, to cover both 400 and 800 V systems, the buck stage will operate at a very low duty cycle, leading to a higher switching current and a larger coupled inductor. Modular design with multiple small power cells is another candidate to handle the wide voltage and high power [35], [36], [37], [38], which, however, usually needs more passive and active devices. The special connection methods between cells also cause the problem of current sharing or voltage matching.

Current-fed (CF) converter, such as current-fed dual active bridge (CFDAB), is another promising topology [39], [40]. It integrates a buck/boost converter and naturally presents a high voltage gain. The zero-voltage switching (ZVS) current and switch-OFF current of the switches in the CF port are determined by both the transformer current and the coupled inductor current, which is different from the regular DAB. However, a comprehensive analytical solution to calculate the ZVS and switch-OFF current has been missing from the previous literature.

Peng et al. [41] analyzed the ZVS conditions of the half-bridge-based voltage-fed (VF) CFDAB. However, the duty cycle of the half-bridge is fixed at 0.5, which simplifies the analysis, but the limited control freedom constrains the voltage range. Watanabe and Itoh [42] analyzed the VF-CFDAB with full-bridge and duty cycle control but proposed discontinuous current-mode (DCM) control to achieve ZVS using the output inductor ripple. While this solution simplifies modeling, it cannot be used for continuous current-mode (CCM) controlled output inductors. How DCM control may lead to excessive output current ripples, which is undesirable for high-current applications, such as APM. A closed-form solution for ZVS/switch-OFF current with the CCM-mode output inductor is more general but is still missing.

The authors in [43] and [44] considered both the transformer current and the CCM inductor current for arbitrary control variables. However, the ZVS boundary was calculated numerically, and a closed-form solution for the ZVS current was not provided. Consequently, the ZVS boundary obtained in the literature is only applicable to specific designs. Guo et al. [45] presented a more comprehensive analytical solution for the ZVS boundary, but the derivation was based on the topology with two independent dc inductors. The coupled inductor is well-suited for the high-current CF port because it cancels the dc components in the output current, thus reducing the output inductor size significantly. However, the discussion of CFDAB with coupled inductors is incomplete. Moreover, using coupled inductors on both input and output is an effective configuration to further extend the voltage range, but its operation and detailed ZVS analysis are still missing. For high-current applications, a more comprehensive closed-form solution for the ZVS and switch-OFF current is still lacking. How to adapt the CFDAB for an ultrawide input and output voltage range and minimize the switching current at the same time is not fully understood yet.

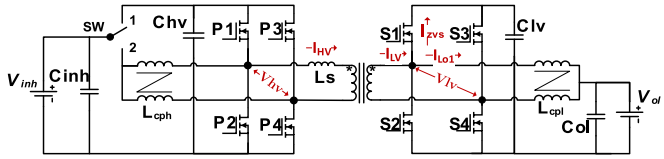

Fig. 2. Proposed reconfigurable CFDAB for the ultrawide voltage range.

This article proposed a CFDAB-based reconfigurable converter, as shown in Fig. 2. Compared with the existing technologies, four major superiorities exhibit the following:

1) ultrawide voltage ranges ($V_{\rm in}$ = 180–900 Vdc, $V_{\rm out}$ = 6–16 Vdc);
2) reduced transformer turn ratio and winding rms current;
3) reduced rms current of the LV high-side switches;
4) low and controllable switch-OFF current.

The rest of this article is organized as follows. Section II details the system specifications, operational principles, and modeling. Section III discusses the optimization and control of the CFDAB. Section IV discusses the design implementations. The experimental results are given in Section V. Finally, Section VI concludes this article.

II. Operation and Modeling of Reconfigurable CFDAB

As illustrated in Fig. 2, a CF port is adopted on the LV side, while the HV port can be configured as either the VF or CF port by the switch SW, which is designed as reconfigurable to extend the voltage range and increase the power capability at the extreme voltage range. The CF port on the LV side helps to reduce the transformer turn ratio and the current stress. Both input/output filters L_{CPL} and L_{CPH} are coupled inductors to shrink the size. $C_{\rm hv}$ and $C_{\rm lv}$ are the clamp capacitors to provide a stable voltage for the full bridges. L_s is the leakage inductance of the transformer. V_{inh} is the HV battery voltage and V_{ol} is the LV-side battery voltage. The voltages applied to the transformer terminals are denoted as $V_{\rm hv}$ and $V_{\rm lv}$, respectively.

Such a phase-shift converter can be modeled as two voltage sources connected by an inductor, as shown in Fig. 3. The power flow between voltage sources is solely determined by the voltage sources and inductance. Despite the configuration, the phase-shift converter is always a current-source converter. Thus, it is

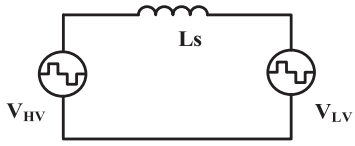

Fig. 3. Simplified phase-shift converter model.

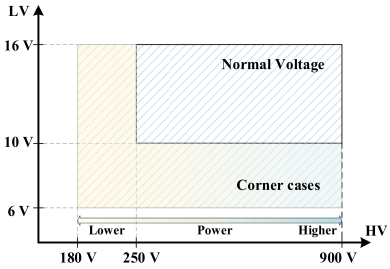

Fig. 4. Operational voltage range of the proposed APM.

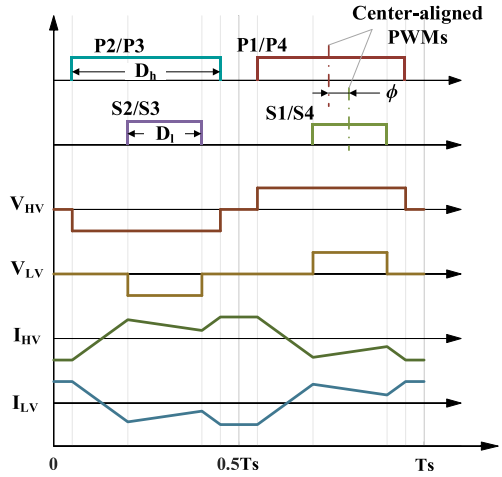

Fig. 5. Variable definition and typical waveforms.

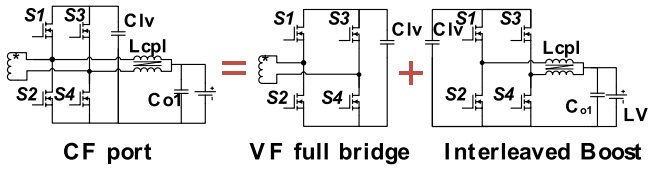

Fig. 6. Decomposition of LV-side CF port.

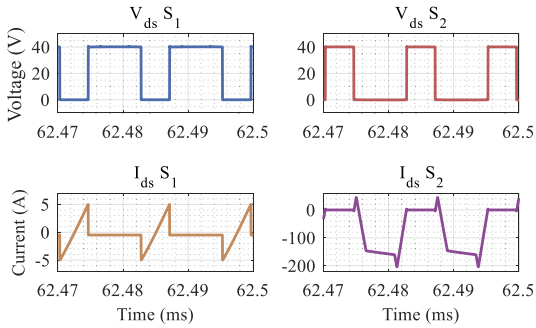

Fig. 7. Typical $\boldsymbol{V_{ds}}$ and $\boldsymbol{I_{ds}}$ of CF port in operation mode 1.

naturally fit for wide-voltage-range applications. However, the conventional DAB, regardless of VF or CF type, suffers the high switch-OFF current when the input/output voltage does not match the transformer turn ratio, also it is hard to secure the ZVS switch-ON at the light load, thereby yielding poor efficiency. To leverage the benefits of phase-shift converters and avoid the drawbacks, this article will focus on minimizing the switch-OFF current and securing the ZVS in the full voltage and power range.

A. Specifications and Operational Principles

Although facing both the 400 and 800 V configurations, depending on the battery state-of-charge (SOC), the peak voltage of a 400 V battery can be close to the minimum voltage of the 800 V system. Hence the APM needs to cover 180–900 V seamlessly. As shown in Fig. 4, the whole voltage range is divided into two regions, the normal voltage range and the corner cases. The normal voltage range, which spans from 250 to 900 V on the HV side and from 10 to 16 V on the LV side, represents the main operational range and is the focus of system optimization efforts. The corner cases refer to the operational range when the input voltage is below 250 V or the output voltage is below 10 V. These extreme voltage levels are less frequently encountered in typical operations. In such cases, the output power and efficiency may be derated to ensure compliance with the voltage range requirements.

The main control variables and typical waveforms of the proposed topology are depicted in Fig. 5, where D_h is the duty cycle of switches $P1/P4$, and D_l is the duty cycle of switches $S1/S4$. T_s is the switching period, and ϕ is the phase shift between the HV-side and LV-side pulsewidth modulations, defined as the time difference divided by $T_s/2$. When $\phi = 0$, the HV-side and LV-side voltages are center aligned with zero active power.

B. Operation of LV-Side CF Port

The LV side is always a CF port despite the HV-side configuration. The operational principles, advantages, and characteristics of the CF port include the following.

1) A CF port on the LV side helps to reduce the transformer turn ratio, facilitating transformer fabrication. It can be decomposed as a VF port plus an interleaved boost converter, as shown in Fig. 6, which steps up the LV battery voltage, thereby effectively reducing the transformer turn ratio.
2) The CF port high-side switches ($S1$ and $S3$) and low-side switches ($S2$ and $S4$) carry different rms currents. In certain operational modes, the high-side switches of CFDAB only circulate a small rms current to hold a stable voltage across the clamp capacitor C_{LV} (C_{HV} for the HV port), while the main load current is carried by low-side switches, as illustrated in Fig. 7. This is particularly beneficial for the LV side, generating less loss or requiring fewer MOSFETs in parallel. Although the current of the high side and low side is unbalanced, the rms value of either side is much

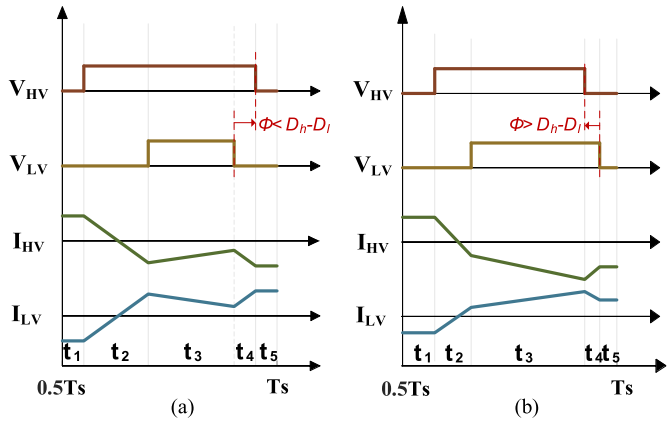

Fig. 8. Basic operational modes. (a) Mode 1. (b) Mode 2.

lower than the conventional design. Both high-side and low-side devices keep the overall loss and temperature rise low, thus will barely harm the system's reliability.

3) The low-side switches carry a much higher load current, but the switching current is still the same as the high-side switches in certain operational modes. This reveals another significant benefit of the CF port, i.e., the switching current can be low regardless of the output power. The detailed switching current and related operational modes will be discussed later.
4) The ZVS current of the CF port consists of transformer current and coupled inductor current. Different from the regular DAB where the switch current follows the transformer current, both the transformer current and coupled inductor ripple current need to be considered to calculate the ZVS current of the CFDAB. As shown in Fig. 2, $I_{\text{ZVS}} = I_{\text{LV}} - I_{cpl}$, which also applies to the HV port when it is configured as a CF port. The part contributed by the inductor ripple is particularly important when small output inductors are equipped.

Note that the "unbalanced" current distribution mentioned in points 3 and 4 actually means reduced current stress on both high-side and low-side switches compared with the conventional DAB converter, with a greater reduction on the high side. Despite the asymmetric distribution of losses, the overall loss for both switches remains within safe limits. Furthermore, the proposed configuration requires fewer devices compared with symmetric current stress distribution, making it a more efficient and cost-effective solution.

C. HV Side Configured as VF Port

When the SW, as shown in Fig. 2, is switched to position 1, the HV port is configured as VF, and the LV side is kept as CF. This configuration will be noted as VF-CFDAB in this article.

A phase-shift converter has multiple operational modes. Each mode has a unique set of equations to describe its behaviors. Two modes, as illustrated in Fig. 8(a) and (b), will be utilized for their special properties and consecutive control variables, which will be detailed in the Section III.

The boundary condition between the two modes is given in (1). When $\phi > D_h - D_l$, the converter enters mode 2

$$D_h = D_l + \phi. \tag{1}$$

In mode1, the output power is

$$P_{\text{VF\_op1}} = \frac{N_t \phi T_s V_{inh} V_{ol}}{L_s}. \tag{2}$$

The HV-side switch-ON and switch-OFF currents in mode 1 are symmetrical, which means that the switching-ON current equals the negative value of the switch-OFF current. The switching-ON current is

$$I_{\text{VF\_op1}_{\text{hv-on}}} = -\frac{T_s\left(D_h V_{inh} - N_t V_{ol}\right)}{2L_s}. \tag{3}$$

Here, N_t is the transformer's high-side to low-side turn ratio. Note that if the coupled inductor is not disconnected in VF-CFDAB, the self-inductance L_{hv} of L_{CPH} still presents and an extra inductive current I_{cph_pk} defined in (4) needs to be considered. This current helps to facilitate ZVS but also contributes to extra switching current. If the switching loss is of concern, a relay should be installed to fully disconnect L_{CPH} in the VF-CFDAB configuration. However, if the control is well designed, as illustrated later, there is no need to utilize I_{cph_pk} to achieve ZVS. Thus, in this article, the impact of I_{cph_pk} is ignored in the VF-CFDAB configuration

$$I_{cph\_pk} = \frac{T_s D_h V_{inh}}{2L_{\text{hv}}}. \tag{4}$$

The LV-side switch-ON and switch-OFF currents in mode 1 are also symmetric. The switch-ON current is

$$I_{\text{VF\_op1}_{\text{lv-on}}} = -\frac{N_t T_s\left(N_t V_{ol} - D_l V_{inh}\right)}{2L_s} - \frac{T_s V_{ol}\left(L_{\text{lv}} - D_l L_{\text{lv}} + D_l M_{\text{lv}}\right)}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)} \tag{5}$$

where L_{lv} is the self-inductance of L_{CPL}, and M_{lv} is the mutual inductance of its two windings. Note that (5) consists of two parts, which correspond to the transformer current and coupled inductor ripple current.

In operational mode 2, the power is given as

$$P_{\text{VF\_op2}} = \frac{N_t T_s V_{inh} V_{ol} D_l\left(2D_h - D_l + 2\phi\right) - N_t T_s V_{inh} V_{ol}\left(D_h - \phi\right)^2}{4 D_l L_s}. \tag{6}$$

The switch-ON current and switch-OFF current are no longer symmetrical, as illustrated in Fig. 9. For the HV port, the switch-ON current is the same as (3). The switch-OFF current is

$$I_{\text{VF\_op2}_{\text{hv-off}}} = \frac{T_s\left(D_h D_l V_{inh} - D_h N_t V_{ol} + N_t \phi V_{ol}\right)}{2 D_l L_s}. \tag{7}$$

The LV-side switching current is also associated with the coupled inductor ripple current, with its switch-ON and switch-OFF

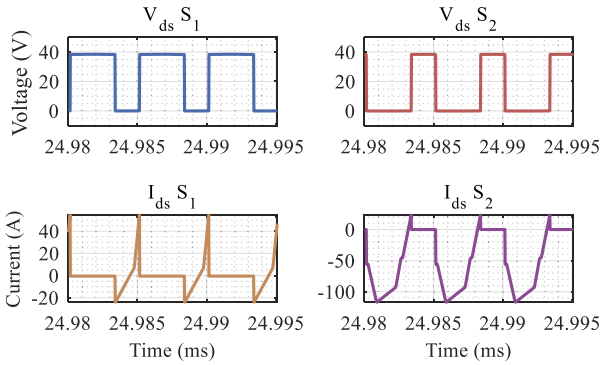

Fig. 9. Typical $\boldsymbol{V_{ds}}$ and $\boldsymbol{I_{ds}}$ of CF port in operation mode 2.

currents given in (8) and (9), respectively

$$I_{\text{VF\_op2}_{\text{lvon}}} = -\frac{T_s V_{ol}\left(L_{\text{lv}} - D_l L_{\text{lv}} + D_l M_{\text{lv}}\right)}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)} - \frac{N_t T_s\left(N_t V_{ol} + \left(\phi - D_l\right) V_{inh}\right)}{2L_s} - \frac{N_t T_s V_{inh}\left(D_h^2 - 2D_h D_l - 2D_h\phi + D_l^2 - 2D_l\phi + \phi^2\right)}{8D_l L_s} \tag{8}$$

$$I_{\text{VF\_op2}_{\text{lvoff}}} = \frac{N_t T_s\left(N_t V_{ol} - D_h V_{inh}\right)}{2L_s} + \frac{T_s V_{ol}\left(L_{\text{lv}} - D_l L_{\text{lv}} + D_l M_{\text{lv}}\right)}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)} - \frac{N_t T_s V_{inh}\left(D_h^2 - 2D_h D_l - 2D_h\phi + D_l^2 - 2D_l\phi + \phi^2\right)}{8D_l L_s}. \tag{9}$$

D. HV-Side Configured as a CF Port

When the switch SW, as shown in Fig. 1, is switched to position 2, the HV port is configured as CF mode, which will be noted as CF-CFDAB configuration in this article. It integrates an interleaved boost stage on the HV side. This configuration will mainly be used for the corner cases when the input voltage is extremely low but the output voltage is relatively high. Similar to the VF-CFDAB, two same operational modes, as defined in Fig. 8, will be discussed for CF-CFDAB.

The modes' boundary of the CF-CFDAB is the same as the VF-CFADB given in (1). The output power of the CF-CFDAB in mode 1 is

$$P_{\text{CF\_op1}} = \frac{N_t \phi T_s V_{inh} V_{ol}}{D_h L_s}. \tag{10}$$

The power has a similar form as VF-CFDAB. The main difference is the involvement of D_h. In the CF-CFDAB, the voltage of C_{HV} is boosted to V_{inh}/D_h. Attention is needed for the voltage constraint when setting D_h.

The CF-CFDAB configuration is more complex due to the introduction of an additional coupled inductor. α, β, γ, and δ given in (11)–(14) are used to shorten the equations, where L_{hv} is the self inductance of L_{CPH} and M_{hv} is the mutual inductance between L_{CPH} windings

$$\alpha = \frac{T_s V_{inh}\left(L_{\text{hv}} - D_h L_{\text{hv}} + D_h M_{\text{hv}}\right)}{2\left(L_{\text{hv}}^2 - M_{\text{hv}}^2\right)} \tag{11}$$

$$\beta = \frac{T_s V_{ol}\left(L_{\text{lv}} - D_l L_{\text{lv}} + D_l M_{\text{lv}}\right)}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)} \tag{12}$$

$$\gamma = \frac{N_t T_s\left(D_h^2 - 2D_h D_l - 2D_h\phi + D_l^2 - 2D_l\phi + \phi^2\right)}{8D_h D_l L_s} \tag{13}$$

$$\delta = \frac{T_s\left(V_{inh} - N_t V_{ol}\right)}{2L_s}. \tag{14}$$

The switch-ON and switch-OFF currents are still symmetrical in mode 1 despite the configuration. The HV port switch-ON current is

$$I_{\text{CF\_op1}_{\text{hvon}}} = -\alpha - \delta - \frac{N_t \phi T_s V_{ol}}{2D_h L_s}. \tag{15}$$

The LV port switch-ON current is

$$I_{\text{CF\_op1}_{\text{lvon}}} = \frac{D_l N_t T_s V_{inh}}{2D_h L_s} - \frac{N_t^2 T_s V_{ol}}{2L_s} - \beta. \tag{16}$$

In operational mode 2 of CF-CFDAB, the output power is

$$P_{\text{CF\_op2}} = -2\gamma V_{inh} V_{ol}. \tag{17}$$

The switch-ON and switch-OFF currents are then no longer symmetrical. The HV-side switch-ON current is

$$I_{\text{CF\_op2}_{\text{hvon}}} = \gamma V_{ol} - \alpha - \delta. \tag{18}$$

The HV switch-OFF current is

$$I_{\text{CF\_op2}_{\text{hvoff}}} = \alpha + \gamma V_{ol} + \frac{T_s\left(D_l V_{inh} - D_h N_t V_{ol} + N_t \phi V_{ol}\right)}{2D_l L_s}. \tag{19}$$

The LV-side switch-ON current is

$$I_{\text{CF\_op2}_{\text{lvon}}} = -\left(\beta + \gamma V_{inh} + \frac{N_t T_s\left(\phi V_{inh} - D_l V_{inh} + N_t D_h V_{ol}\right)}{2D_h L_s}\right). \tag{20}$$

The LV switch-OFF current is

$$I_{\text{CF\_op2}_{\text{lvoff}}} = \beta - \gamma V_{inh} - \delta N_t. \tag{21}$$

The equations in this section offer the complete description of the power, ZVS current, and switch-OFF current in the major operational modes and two different system configurations with the coupled inductor current considered. These closed-form solutions serve as valuable tools for the control design and optimization in Section III.

III. Control of Proposed Reconfigurable CFDAB

This section will discuss the key characteristics of the converter, particularly the optimization of duty cycles to secure ZVS and minimize the switch-OFF current.

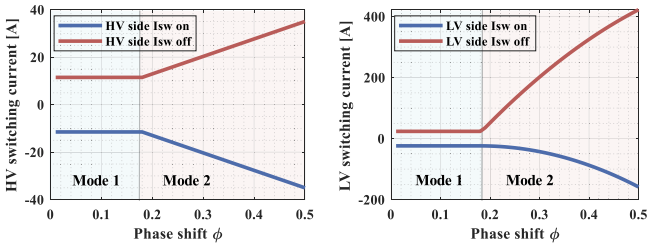

Fig. 10. Switching current versus phase shift in different operation modes, VF-CFDAB.

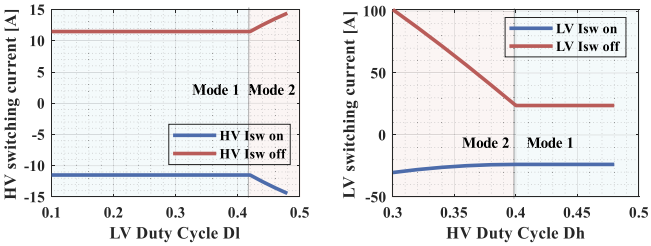

Fig. 11. Switching current versus duty cycle in different operation modes, VF-CFDAB.

TABLE I
ROLES OF CONTROL VARIABLES

Related Control Variables		VF-CFDAB configuration		CF-CFDAB configuration	
		Mode 1	Mode 2	Mode 1	Mode 2
Output Power		ϕ	D_h, D_l, ϕ	D_h, ϕ	D_h, D_l, ϕ
HV side	Isw_on	D_h	D_h	D_h, ϕ	D_h, D_l, ϕ
	Isw_off	D_h	D_h, D_l, ϕ	D_h, ϕ	D_h, D_l, ϕ
LV side	Isw_on	D_l	D_h, D_l, ϕ	D_h, D_l	D_h, D_l, ϕ
	Isw_off	D_l	D_h, D_l, ϕ	D_h, D_l	D_h, D_l, ϕ

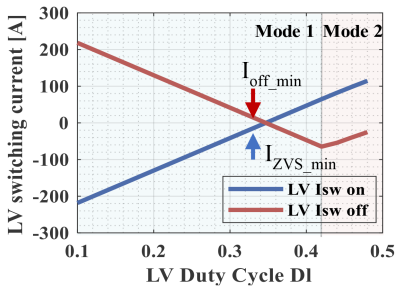

Fig. 12. LV-side switching current versus the duty cycle at 500 V/14 V.

A. Key CFDAB Characteristics

Several important characteristics of CFDAB are revealed by the closed-form equations, as derived in Section II.

1) The output power of the VF-CFDAB configuration in operational mode 1 is not related to any duty cycle, but only the voltages and the phase shift when the transformer is settled, as suggested in (2).
2) The switch-ON and switch-OFF currents of both the HV and LV ports in the VF-CFDAB configuration are not related to phase shift in operational mode 1, which means that the switching currents are decoupled with the output power, as suggested in (3) and (5). Fig. 10 also shows an example of 500 V input and 14 V output. Clearly, the switching current remains constant in mode 1 for both the HV and LV ports.
3) The HV-side switching current is only related to D_h, and the LV-side switching current is only related to D_l for VF-CFDAB configuration in operation mode 1, as suggested in (3) and (5). An example is shown in Fig. 11, where the HV-side switching current is not related to the LV-side duty cycles. The same applies to the LV side. It means that the switching current of one port can be independently controlled by the corresponding duty cycle without being affected by the other port.
4) The switch-OFF current increases rapidly after entering operation mode 2 for HV and LV ports in both VF and CF configurations. Thus, from the switching losses point of view, mode 1 is preferred.

How control variables D_h, D_l, and ϕ are linked to the output power and the switching current is summarized in Table I.

B. Duty Cycles Optimization for VF-CFDAB

The special characteristics of the CFDAB topology suggest a possible decoupled switching current and power control, where the switching current is more related to duty cycles. Thus, this article adopts duty cycles as the main control variables for optimization. The goal is to secure full-range ZVS and minimize the switch-OFF current.

For the LV port of VF-CFDAB, the switching current decreases with D_l in mode 1, as one example shown in Fig. 12.

There is a duty cycle where both the switch-ON and switch-OFF currents are zero, which, however, is not feasible to achieve ZVS, particularly when the LV-side MOSFETs have relatively large output capacitance. To minimize the switching current and at the same time secure ZVS, the target switch-ON current is calculated as

$$I_{\mathrm{lv_{zvs}}} = \frac{2Q_{\mathrm{lv}}}{T_{db}} \tag{22}$$

where T_{db} is the deadtime and Q_{lv} is the charge stored in the output capacitance of LV-side MOSFETs. Together with (5), the boundary LV-side duty cycle is

$$D_{l_{\mathrm{LVzvs}}} = \frac{\frac{T_s V_{ol} N t^2}{2L_s} - \frac{2Q_{\mathrm{lv}}}{T_{db}} + \frac{L_{\mathrm{lv}} T_s V_{ol}}{2L_{\mathrm{lv}}^2 - 2M_{\mathrm{lv}}^2}}{\frac{N t T_s V_{inh}}{2L_s} + \frac{T_s V_{ol}(L_{\mathrm{lv}} - M_{\mathrm{lv}})}{2L_{\mathrm{lv}}^2 - 2M_{\mathrm{lv}}^2}}. \tag{23}$$

Because, in mode 1, the LV switch-ON current and switch-OFF currents are symmetrical; when the minimal ZVS current is secured, the minimal switch-OFF current is also guaranteed.

Different from the LV side, the HV port switching current increases with duty cycles, as shown in Fig. 13.

When reducing D_h, the switch-OFF current keeps decreasing despite the operational modes. Hence, a smaller D_h is preferred to minimize the switch-OFF current. However, the switch-ON current has a peak value at the boundary of mode 1 and mode 2. To secure ZVS, D_h needs to secure a minimal ZVS current similar to (3). Together with (22), the boundary D_h to achieve

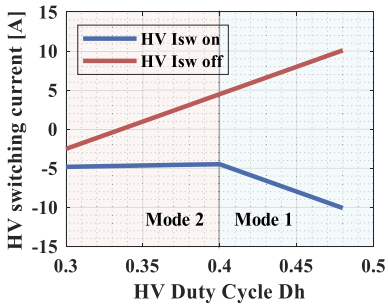

Fig. 13. HV-side switching current versus the duty cycle at 500 V/14 V.

HV-side ZVS is

$$D_{h_{\mathrm{HVzvs}}} \leq \frac{4L_s Q_{\mathrm{hv}} + N_t T_s T_{db} V_{ol}}{T_s T_{db} V_{inh}} \tag{24}$$

where Q_{hv} is the charge stored in the HV-side MOSFETs output capacitance. Note that D_h in (24) has a wide range. While ZVS is always secured, smaller D_h yields smaller switch-OFF current stress. However, if D_h is too small, the converter will enter operational mode 2, and the LV-side switch-OFF current will surge. Thus, D_h needs to be large enough to stay in mode 1

$$D_h \geq D_{l_{\mathrm{LVzvs}}} + \phi. \tag{25}$$

Therefore, the optimal solution for the HV-side duty cycle will be $D_h = D_{l_{\mathrm{LVzvs}}} + \phi$. D_h will then vary with $D_{l_{\mathrm{LVzvs}}}$, which simplifies the control significantly. The corresponding HV-side switch-OFF current is no longer minimal. However, this does not impact the overall efficiency much, given the switch-OFF current does not increase rapidly and the HV switching loss is not dominant. The HV-side switch-ON current at the boundary of operational modes is then

$$I_{\mathrm{hv_{zvsmin}}} = \frac{T_s\left(N_t V_{ol} - V_{inh}\left(D_l + \phi\right)\right)}{2L_s}. \tag{26}$$

To make sure, there is a solution of (24)

$$I_{\mathrm{hv_{zvsmin}}} \geq \frac{2Q_{\mathrm{hv}}}{T_{db}}. \tag{27}$$

Thus, the additional limitation of D_l is

$$D_l \geq \frac{2L_s\left(\frac{2Q_{\mathrm{hv}}}{T_{db}} + \frac{T_s(N_t V_{ol} - \phi V_{inh})}{2L_s}\right)}{T_s V_{inh}}. \tag{28}$$

In summary, the limitations of D_h and D_l are given as follows.

1) The LV-side duty cycle secures ZVS and minimal switch-OFF current simultaneously.
2) The HV-side ZVS current at the boundary of modes must be enough to discharge C_{oss}.
3) The smaller D_h the better, as long as larger than $D_l + \phi$.
4) $D_h = D_l + \phi$ links D_h and D_l. Thus, D_l also needs to ensure that the HV-side ZVS current is high enough at the boundary of operational modes.

In addition, the duty cycles of the CF port cannot be too small in case the clamp capacitor sees overvoltage.

A more comprehensive representation of the ZVS boundaries is given in Fig. 14, showcasing the relationship for a specific case with a 500 V input and 14 V output at a fixed phase shift of 0.1. It is important to note that, for each voltage combination, a specific figure can be generated to demonstrate the relationship between the ZVS current and duty cycles.

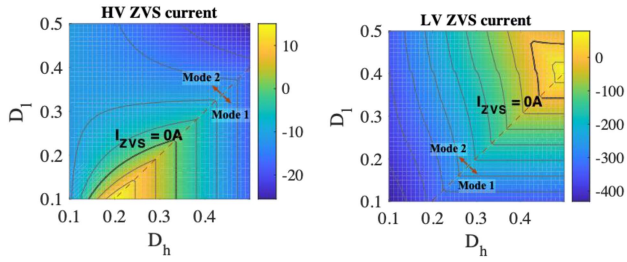

Fig. 14. ZVS current versus duty cycles for 500 V/14 V.

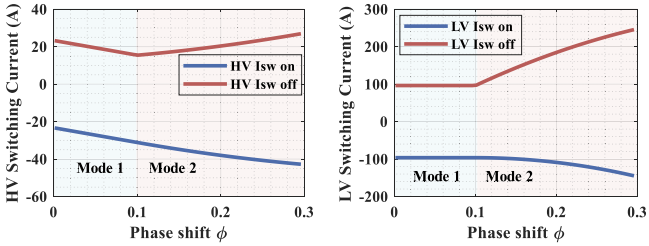

Fig. 15. Impact of the ϕ on switching current, fixed $\boldsymbol{D_h}$ and $\boldsymbol{D_l}$, CF configuration.

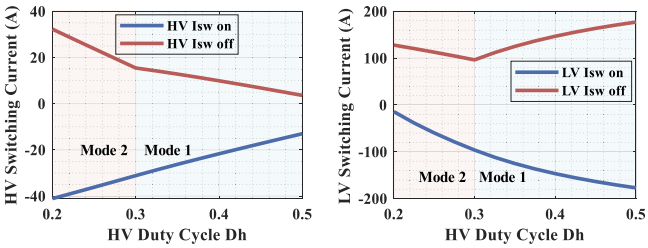

Fig. 16. Impact of $\boldsymbol{D_h}$ on switching current, fixed $\boldsymbol{D_l}$, CF-CFDAB.

C. Duty Cycles Optimization for CF-CFDAB

The optimization of the CF-CFDAB has the same target as the VF-CFDAB. However, as shown in Table I, more control variables are involved in the CF configuration. The phase shift or the output power is no longer decoupled with the switching currents. It impacts the switching current for both mode 1 and mode 2, as illustrated in Fig. 15.

However, the switch-ON current keeps decreasing with ϕ increasing throughout modes 1 and 2. It means as long as the ZVS can be secured at $\phi = 0$, the full-range ZVS can be realized. As for the switch-OFF current, the LV side keeps minimal current stress in mode 1, and the HV side has minimal switch-OFF current at the boundary of the operation modes. It means that the optimized switching loss is still happening at $D_h = D_l + \phi$, the same as the VF-CFDAB configuration, as validated in Fig. 16, where a higher D_h helps to reduce the HV-side switch-OFF current but increases the LV-side switch-ON current rapidly.

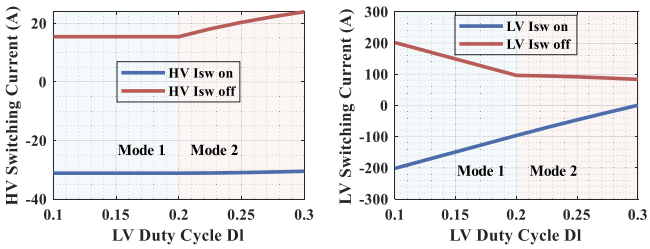

Fig. 17. Impact of D_l on switching current, fixed D_h, CF configuration.

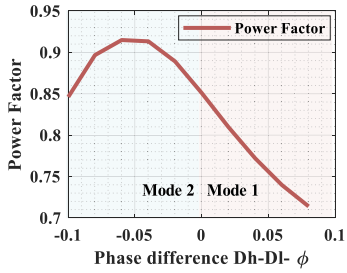

Fig. 18. Transformer power factor versus the phase difference.

Considering the overall switching losses, keeping D_h at the boundary of operational modes is still preferred.

Overall, keeping $D_h = D_l \ + \phi$ not only minimizes the switching losses but also simplifies the setting of the ZVS boundary. According to (15), the switch-ON current of the HV port at $\phi = 0$ is

$$I_{\text{hvon}_{\phi=0}} = -\frac{T_s\left(V_{inh} - N_t V_{ol}\right)}{2L_s} - \frac{T_s V_{inh}\left(L_{\text{hv}} - D_h L_{\text{hv}} + D_h M_{\text{hv}}\right)}{2\left(L_{\text{hv}}^2 - M_{\text{hv}}^2\right)}. \tag{29}$$

To secure the HV-side ZVS, (22) must hold true for $I_{\text{lvon}_{\phi=0}}$. Also when $\phi = 0$, $D_h = D_l$. Thus, the boundary condition for the HV-side ZVS is

$$D_{l_{\text{HVzvs}}} \le \frac{2\left(L_{\text{hv}}^2 - M_{\text{hv}}^2\right)\left(\frac{T_s(V_h - N_t V_{ol})}{2*Lkh} - \frac{2Q_{\text{hv}}}{Tdb} + \frac{L_{\text{hv}} T_s V_{inh}}{2\left(L_{\text{hv}}^2 - M_{\text{hv}}^2\right)}\right)}{T_s V_{inh}\left(L_{\text{hv}} - M_{\text{hv}}\right)}. \tag{30}$$

This represents the worst case for ZVS. The LV-side switch-ON and switch-OFF currents are solely controlled by D_l. As shown in Fig. 17, a large D_l is preferred to reduce the LV-side switch-OFF current, but it also decreases the ZVS current. Thus, the maximum useable D_l also needs to secure the LV-side ZVS.

The switch-ON current in operational modes 1 and 2 is consistent when $D_h = D_l$ and $\phi = 0$

$$I_{\text{lvon}_{\phi=0}} = \frac{N_t T_s V_{inh}}{2L_s} - \frac{T_s V_{ol}\left(L_{\text{lv}} - D_l L_{\text{lv}} + D_l M_{\text{lv}}\right)}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)} - \frac{N_t^2 T_s V_{ol}}{2L_s}. \tag{31}$$

Thus, the boundary of ZVS is

$$D_{l_{\text{lvzvs}}} \le -\frac{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)\left(\frac{2Q_{\text{lv}}}{T_{db}} + \frac{N t T_s V_{inh}}{2L_s} - \frac{N t^2 T_s V_{ol}}{2L_s} - \frac{L_{\text{lv}} T_s V_{ol}}{2\left(L_{\text{lv}}^2 - M_{\text{lv}}^2\right)}\right)}{T_s V_{ol}\left(L_{\text{lv}} - M_{\text{lv}}\right)}. \tag{32}$$

Finally, D_l will be selected as

$$D_{l_{\text{opt}}} = \max\left(D_{l_{\text{HVzvs}}},\ D_{l_{\text{LVzvs}}},\ \frac{V_{ol}}{V_{\text{clv}_{\max}}}\right) \tag{33}$$

where $V_{\text{clv}_{\max}}$ is the maximum allowed voltage on the LV-side clamp capacitor.

Due to the high-current nature of the APM application, the conduction loss is another major player. Using $D_h = D_l \ + \phi$ also helps to reduce the circulating current of the transformer, thus the conduction losses. Fig. 18 shows an example of how the power factor of the transformer changes with the phase difference. To illustrate the relationship between control variables, the horizontal axis is set as $D_h - D_l - \phi$. The figure shows that the power factor increases when the difference between D_h and $D_l + \phi$ decreases. Although the peak power factor happens when $D_h < D_l + \phi$, it is actually in the mode 2, which means that the switch-OFF current is high. Thus, $D_h = D_l \ + \phi$ is also the optimal point to maximize the power factor without increasing the switch-OFF current.

IV. Design Implementation

A. Turn Ratio and Boundary of the VF/CF Configuration

The selection of the transformer turn ratio N_t is mainly determined by the ZVS consideration. As aforementioned, the key operational range is the normal voltage zone, as shown in Fig. 4, of which the VF configuration in mode 1 will be the main operation mode. Thus, the target N_t is designed to facilitate the natural ZVS in this key operational range. In the range, the LV-side ZVS current is given in (5). Ignoring the additional ZVS current contributed by the coupled inductor ripple current, the ZVS boundary is

$$N_t > \frac{D_l V_{inh}}{V_{ol}}. \tag{34}$$

Because the LV side is always a CF port, theoretically, D_l could vary from 0–1, although some upper and lower limits are usually installed.

The HV-side ZVS current is given in (3), and the boundary condition of ZVS is

$$N_t < \frac{D_h V_{inh}}{V_{ol}}. \tag{35}$$

Different from the LV side, the maximum D_h is 0.5 in the VF configuration. To make sure ZVS can be achieved by controlling D_h, N_t must be smaller than $\min(\frac{0.5V_{inh}}{V_{ol}})$. In the key operational range, the minimum value is achieved when $V_{inh} = \ 250$ V and $V_{ol} = \ 16$ V. However, $V_{ol} = \ 16$ V is the full SoC of the LV battery. Thus, $V_{ol} = \ 10$ V is selected as a more practical practice. Finally, the turn ratio is selected as $N_t = \ 0.5 \times 250 \div 10 \approx 12$.

With N_t being selected, the VF/CF configuration boundary is also determined. When the ZVS is no longer accomplishable

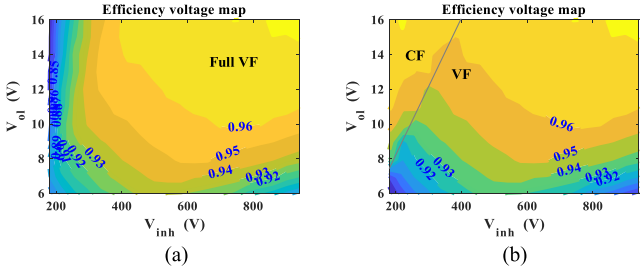

Fig. 19. Efficiency estimation and VF/CF boundary. (a) VF-CFDAB topology. (b) Proposed VF/CF reconfigurable topology.

by controlling duty cycles in the corner cases, the converter will be configured as CF-CFDAB to further extend the ZVS. The boundary voltages are given in (36). The estimated efficiency maps comparing the pure VF-CFDAB topology and proposed reconfigurable topologies are illustrated in Fig. 19. The VF/CF configuration boundary is also marked. Clearly, the reconfigurable design improves the efficiency of corner cases effectively

$$\frac{V_{inh}}{V_{ol}} < \frac{N_t}{\max\left(D_h\right)}. \tag{36}$$

It is worth noting that the selection of the transformer turn ratio also impacts the constrained D_h issues, as mentioned in Fig. 21. With a higher turn ratio, the optimized LV duty cycles will decrease to match the input and output voltage, providing a larger margin for $\phi = \max(D_h) - D_l$, which helps to reduce or eliminate the occurrence of special cases, where D_h is clamped at 0.5. In this design, to obtain the best average efficiency over the full voltage range, the peak efficiency is designed at 500 V input. If different voltages are preferred, the transformer turn ratio needs to be tuned according. For example, if the peak efficiency is preferred at 700 V input, a turn ratio of 17:1 is needed. However, it needs to be noticed that the turn ratio is related to the VF/CF configuration boundary. The higher turn ratio will increase the chance of working with CF-CFDAB configuration when the input voltage is relatively low. For this particular application, there is no need for an online and fast transition. Typically, relays are used for reconfiguration. The transition of APM configuration is done at the same time when the HV battery is reconfiguring. During this short reconfiguration period, critical LV loads are supported by the LV battery, making it permissible to temporarily discontinue the APM before restarting it.

B. Leakage Inductance

A small leakage is preferred for multiple reasons. First, it must be small enough to output rated power when both the input and output voltages are low. Second, for a given power, a low leakage inductance means low phase shift, which means that it can extend the coverage range of the preferred operation mode 1. Third, small leakage helps to reduce the reactive power of the transformer as well as the loss induced by the leakage flux.

The leakage inductance will be determined in the scenario that the HV is at 500 V, which is around the middle point of the full input range, and the LV is at 14 V, which is the nominal voltage.

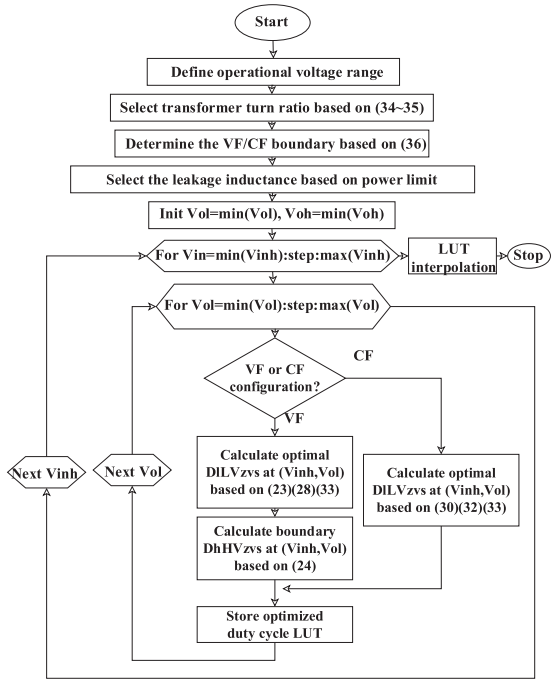

Fig. 20. Design and optimization flowchart.

According to (2) and optimized duty cycles at 500 V/14 V, to output 3 kW at the boundary of operational mode 1, the leakage inductance is around 45 μH.

Leakage inductance is also a factor that relates to the constrained D_h issues, as mentioned in Fig. 21. A smaller leakage inductance allows for higher power delivery within a given margin of ϕ. By minimizing the leakage inductance, the power capacity of the converter can be increased, providing more headroom for D_h without hitting the hard limit.

If considering the leakage inductance during the ZVS design, the general rule found from the ZVS boundary equations is that the smaller the leakage inductance, the higher the possible ZVS current. No matter whether the leakage inductance is high or low, there is always an optimized duty cycle of LV duty cycles, unless the leakage inductance is large enough that there is no solution for the LV duty cycle in 0–1 anymore.

C. Control Implementation

Due to limited computational resources, it is difficult to calculate the optimized duty cycles online. Since the duty is only related to the input and output voltage, it is feasible to do the optimization offline and store results as a lookup table (LUT) for control use. The overall design and optimization steps are summarized as a flowchart in Fig. 20.

In real-time control, the D_l will be selected based on input/output voltages from LUT first. The phase shift will be regulated by a proportional and integral (PI) controller for the target power. The HV-side duty cycle will be set as $D_h = D_l + \phi$ to make sure the converter is operating in mode 1. If the calculated D_h is out of the ZVS boundary or reaches the maximal $D_h = 0.5$, keep D_h at the boundary, and the converter will operate in mode 2.

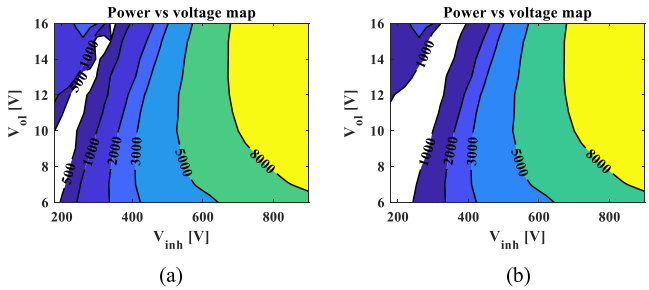

Fig. 21. Max output power versus voltage map with special cases highlighted in white. (a) With 500 W minimal output power limit. (b) With 1000 W minimal output limit.

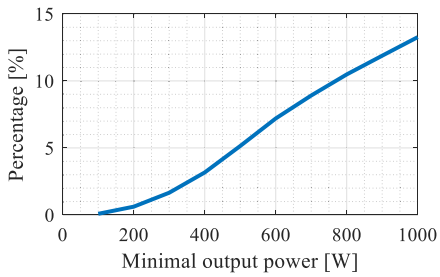

Fig. 22. Cases of constrained D_h in percentage versus required minimal output power.

The occurrence of cases where D_h is kept at 0.5 primarily happens when the optimized D_l is close to 0.5. As aforementioned, operation mode 1 is preferred due to its various benefits. However, the boundary condition of operational mode 1 is $D_h > D_l + \phi$. Therefore, if the optimized D_l is fairly close to 0.5, there is a limited margin for ϕ before the D_h hit the hard limit. Thus, the percentage of these special cases is highly related to the specification, i.e., the required minimal output power for the full voltage range.

Fortunately, hitting the hard limit is not the common case. The theoretical max output power in operational mode 1 is plotted in Fig. 21, with the cases of constrained D_h highlighted in white. With minimal output power requirements of 500 W and 1 kW, the percentage of constrained D_h is 5.2% and 13.4%, respectively. A more comprehensive plot that depicts the percentage versus the power requirement is given in Fig. 22. Note that these special cases mainly occur at extreme voltage levels, which are not common operational ranges of the converter.

V. Experimental Results

A 3-kW prototype is built to test the proposed topology and the control method. The hardware parameters, wide voltage range power capability, efficiency, and loss breakdown are presented in this section.

A. Hardware Implementation

Following the design consideration and optimized design procedure, the parameters of the prototyped hardware are listed in Table II.

TABLE II
Hardware Parameters of the Prototypes

Input voltage range	180 – 900 V
Output voltage range	6 – 16 V
Max output power	3.2 kW
HV-side switches	2×C3M0032120K
LV-side switches	2×IRF100P219
Switching frequency	80 kHz
Leakage inductance	45 μH
Magnetizing inductance	540 μH
Transformer turn ratio N_t	12 : 1
Transformers Core	3C95, E65/32/27
Coupled inductors core	3C95, E43/10/28
HV-coupled inductor self-inductance	50 μH
HV-coupled inductor mutual inductance	35 μH
HV-windings construction	5×52/38×5 turns
LV-coupled inductor self-inductance	10 μH
LV-coupled inductor mutual inductance	8 μH
HV-windings construction	5×34/44/38×4 turns

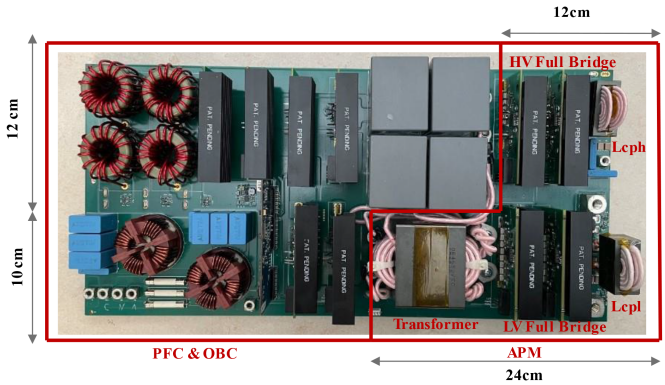

Fig. 23. Hardware prototype.

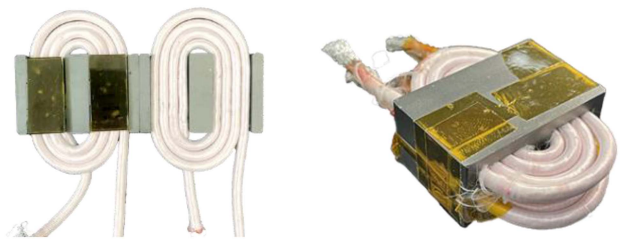

Fig. 24. LV coupled inductors, disassembled and assembled view.

The experimental prototype is shown in Fig. 23. Note that the complete hardware is an integrated charger providing both onboard charger (OBC) and APM functions. For this work, we only utilized the dc–dc part as marked on the right side of the figure. Two coupled inductors for the HV port and LV port are also designed and fabricated with the EE43 cores, as shown in Fig. 24. It is noteworthy that, although the coupled inductor

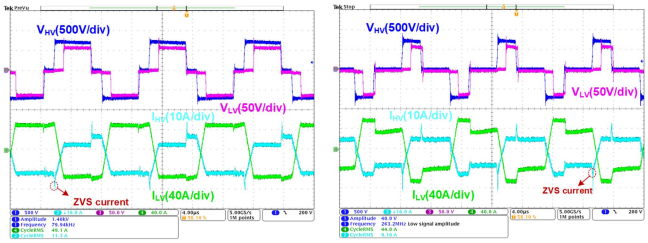

Fig. 25. Key transformer waveforms. (a) At 700 V/16 V, 3.25 kW. (b) At 700 V/6 V, 1.6 kW.

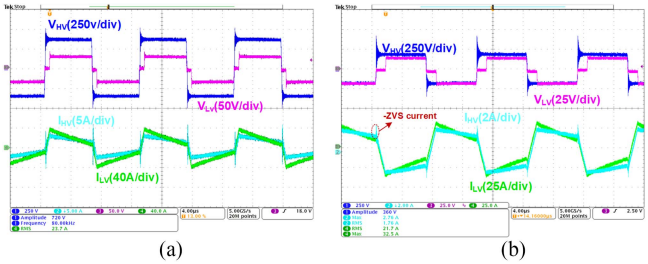

Fig. 26. Key transformer waveforms. (a) At 180 V/16 V, 600 W, CF-CFDAB. (b) At 180 V/6 V, 270 W.

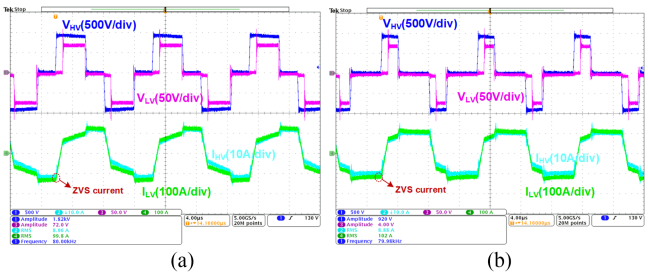

Fig. 27. Key transformer waveforms. (a) At 900 V/16 V, 2.6 kW. (b) At 900 V/6 V, 1.1 kW.

usually has a tolerance of above 5%, the asymmetric inductance only generates the unbalanced ripple current. It will not change the average output current of each output nor induce the dc bias in the transformer.

B. Power Test at Full Voltage Range

The power tests cover the combination of the input voltage of 180 V/350 V/500 V/700 V/900 V and the output voltages of 6 V/14 V/16 V. Each test is down to around 400 W. The tested key transformer currents are given in Figs. 25–27. The maximum power is tested up to 3.25 kW at 700 V input and 16 V output.

The LV-side loads of an APM can kick in and cut off rapidly. This requires a fast closed-loop control of APM to handle the load transients. Fig. 28 gives a test load transient from 10 to 40 A in 300 μs, showing a fast response of 100 A/ms.

The comparison between the proposed control and the conventional voltage matching control that only calculates the duty cycles to match input/output voltage with turn ratio is given in

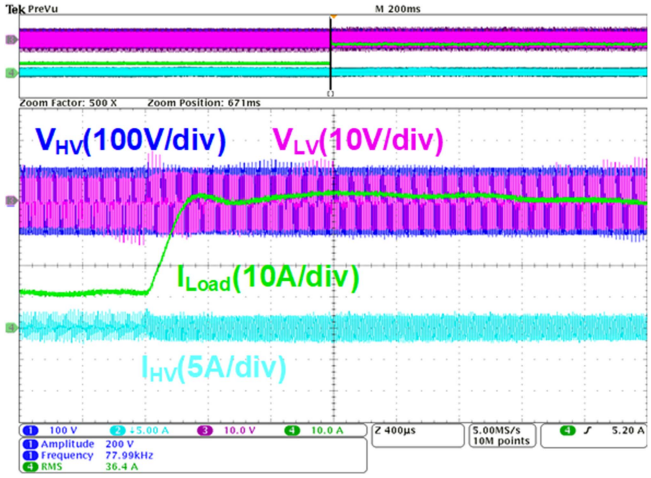

Fig. 28. Load transient test: load current from 10 to 40 A.

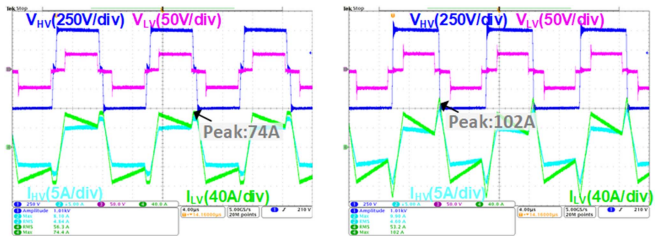

Fig. 29. Peak current comparison at 500 V/14 V, 1.5 kW. (a) Proposed control. (b) Voltage match control.

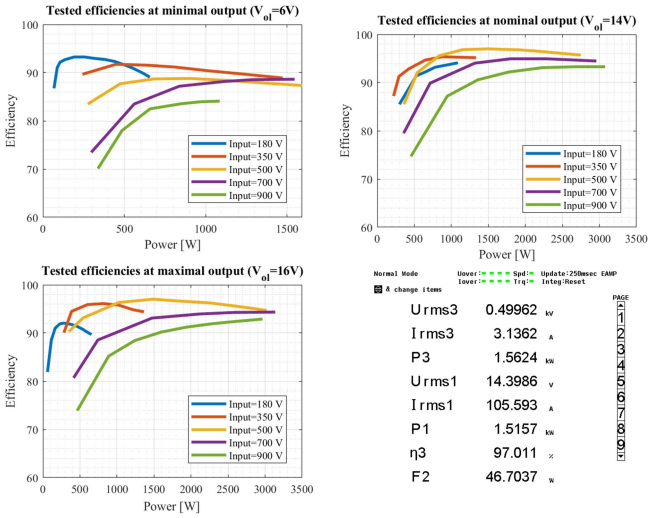

Fig. 30. Efficiency map and peak efficiency screenshot.

Fig. 29. For the same input/output voltages and power level, the proposed control greatly reduced the peak current (74 A compared with 102 A), thereby the switching current.

C. Efficiency and Loss Breakdown

The efficiency is tested under different voltages, as shown in Fig. 30. From the plot, the peak efficiency is above 97% at

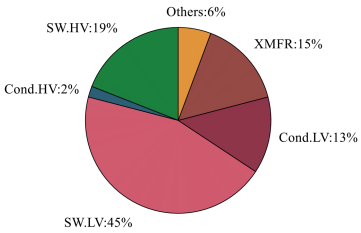

Fig. 31. Losses breakdown at 600 V/16 V/2.2 kW, 103 W total losses.

TABLE III
SPECIFICATIONS AND PERFORMANCE COMPARISON

Products /prototypes	Input voltage	Output voltage	Peak power	Peak efficiency
UTK [31]	250 – 450 V	10 – 16 V	7.0 kW	96%
CAS-EV [46]	240 – 400 V	10 – 15 V	2.7 kW	94%
BorgWarner [47]	220 – 800 V	11 – 13.5 V	1.2 kW	92%
Eaton [48]	225 – 450 V	6 – 16 V	3.0 kW	94%
Bosch [49]	250 – 475 V	10.5 – 15.5 V	3.6 kW	95%
Vitesco [50]	220 – 450 V	8 – 16 V	3.5 kW	Null
Bel Power [51]	400 – 800 V	9 – 16 V	4 kW	93%
NCKU [52]	220 – 450 V	9 – 16 V	2.5 kW	97%
Seoul Tech [53]	460 – 780 V	11.5 – 15.1 V	1.2 kW	93%
Queen's [54]	250 – 430 V	9 – 16 V	1.3 kW	96.5%
NUAA [55]	200 – 450 V	9 – 14.4 V	3 kW	94.7%
This work	180 – 900 V	6 – 16 V	3.25 kW	97%

1.5 kW output. The efficiency curve also indicates the power capability for the corner cases by examining the maximal tested power for each curve. Notice that the maximal power is aligned with real-world requirements and constraints. For example, at a low input voltage, the maximum required power is relatively low. The considerations behind this include: First, the HV battery is already drained and cannot provide high output power when its terminal voltage is close to 180 V; second, no need for high output power at the ultralow input cases since only critical loads are needed to be powered under the corner cases. Thus, there is no need to charge the LV battery at high power. Another case is when the input voltage is high but the output voltage is low. The maximal power is relatively higher at 1.5 kW, given the HV battery has a high charge and can provide enough power, while at the same time, the LV battery is almost drained and needs higher charging power.

Although the 700–14 V is the most used case for 800 V EV, the peak efficiency is designed at 500 V/14 V. The reason is that the converter design needs to consider the safe operation of the devices for the full input voltage range. Optimizing the system for 500 V/14 V, where 500 V is around the middle of the input voltage range, may slightly scarify the peak efficiency during daily driving, but it improves the light-load efficiency, keeps the overall loss low across the full voltage range, and thus extend the operational range for corner case availability, such as the cases when the EVs are unattended for a long time and the HV battery is drained.

The loss breakdown is also included, as shown in Fig. 31. Aligned with what was mentioned earlier in this article, the major losses come from the HV and LV switching losses, which also confirms the necessity of switching current optimization.

VI. CONCLUSION

This article proposed a reconfigurable APM topology to cover an ultrawide range of input and output voltage. This work derived the first closed-form solution for the ZVS and turn-OFF current with the coupled inductor current taken into consideration. The solution also works with arbitrary duty cycles and phase shifts for both VF-CFDAB/CF-CFDAB in different operational modes. The corresponding optimization method is proposed for a simple control to minimize the switching losses and secure a full-range ZVS. The power tests have been done to cover 180–900 V input and 6–16 V output, with a peak efficiency of 97% and a maximal power of 3.25 kW. The tested results prove the wide voltage capability and effectiveness of the control, which makes the proposed converter a promising candidate to power the LV system for the emerging 400 V/800 V EVs. The proposed technology compared with the existing product and literature is summarized in Table III.

REFERENCES

[1] L. Kostal, L. Schmidhauser, L. Kabel, and R. Bosch, "Voltage cases for electric mobility," 2013, Accessed on: Mar. 4, 2020. [Online]. Available: www.zvei.org
[2] C. Jung, "Power up with 800-V systems: The benefits of upgrading voltage power for battery-electric passenger vehicles," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 53–58, Mar. 2017, doi: 10.1109/MELE.2016.2644560.
[3] B. Conlon, M. Anwar, K. Sevel, M. Wang, R. Badawi, and A. Bavili, "Switchable 400V/800V high voltage architecture for ultium battery electric trucks," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6, doi: 10.1109/ECCE50734.2022.9947905.
[4] "Model S owner's manual," Tesla, Accessed on: Aug. 26, 2023. [Online]. Available: https://www.tesla.com/ownersmanual/models/en_us/GUID-E414862C-CFA1-4A0B-9548-BE21C32CAA58.html
[5] "Model X owner's manual," Tesla, Accessed on: Aug. 26, 2023. [Online]. Available: https://www.tesla.com/ownersmanual/modelx/en_us/GUID-E414862C-CFA1-4A0B-9548-BE21C32CAA58.html
[6] J. Shaoqing et al., "Whole vehicle electric architecture without low-voltage energy source and vehicle," CN116278820A, Jun. 2023, Accessed on: Aug. 24, 2023. [Online]. Available: https://patents.google.com/patent/CN116278820A/en?q=(LV+battery+auxiliary+emergency)&oq=LV+battery+auxiliary+emergency
[7] J. L. D. Arroyabe, "Battery controller for an electrically driven vehicle without any low-voltage battery, electrically driven vehicle comprising said controller, and method," US11351866B2, Jun. 2022, Accessed on: Aug. 24, 2023. [Online]. Available: https://patents.google.com/patent/US11351866B2/en?q=(%E6%97%A0%E4%BD%8E%E5%8E%8B%E7%94%B5%E6%B1%A0)
[8] Ö. Spjuth, M. Sonesson, and S. Lorensson, "Battery architecture without low voltage battery," US20220274488A1, Sep. 2022, Accessed on: Aug. 24, 2023. [Online]. Available: https://patents.google.com/patent/US20220274488A1/en?q=(%E6%97%A0%E4%BD%8E%E5%8E%8B%E7%94%B5%E6%B1%A0)
[9] L. Qixin, W. Jian, and X. Dongsheng, "A kind of highly reliable electronl-mobil electric system without low voltage battery," CN204687856U, Oct. 2015, Accessed on: Aug. 24, 2023. [Online]. Available: https://patents.google.com/patent/CN204687856U/en?q=(%E6%97%A0%E4%BD%8E%E5%8E%8B%E7%94%B5%E6%B1%A0)
[10] I. Aghabali, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin, and A. Emadi, "800-V electric vehicle powertrains: Review and analysis of benefits, challenges, and future trends," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 3, pp. 927–948, Sep. 2021, doi: 10.1109/TTE.2020.3044938.
[11] S. Mungekar, A. Dey, and G. Gohil, "High efficiency bidirectional DC-DC converter with matrix transformer for heavy duty hybrid electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 641–648, doi: 10.1109/ECCE44975.2020.9236243.

[12] J. Engelhardt, J. M. Zepter, T. Gabderakhmanova, G. Rohde, and M. Marinelli, "Double-string battery system with reconfigurable cell topology operated as a fast charging station for electric vehicles," *Energies*, vol. 14, no. 9, Jan. 2021, Art. no. 2414, doi: 10.3390/en14092414.
[13] O. García, L. A. Flores, J. A. Oliver, J. A. Cobos, and J. de la Peña, "Bi-directional DC/DC converter for hybrid vehicles," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, 2005, pp. 1881–1886, doi: 10.1109/PESC.2005.1581888.
[14] C. L. Zhu, M. Shen, and M. Obrigkeit, "A high power DC/DC converter designed for single coolant loop hybrid electric vehicle application," *SAE Tech. Papers*, SAE International, Warrendale, PA, USA, 2010, doi: 10.4271/2010-01-1254.
[15] A. Amirahmadi, M. Domb, and E. Persson, "High power density high efficiency wide input voltage range LLC resonant converter utilizing E-mode GaN switches," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 350–354.
[16] R. T. H. Li, M.-F. Vancu, F. Canales, and D. Aggeler, "High performance dc-dc converter for wide voltage range operation," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, 2012, pp. 1151–1158, doi: 10.1109/IPEMC.2012.6258987.
[17] A. Mustafa and S. Mekhilef, "Dual phase LLC resonant converter with variable frequency zero circulating current phase-shift modulation for wide input voltage range applications," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2793–2807, Mar. 2021, doi: 10.1109/TPEL.2020.3015799.
[18] K. K. F. Yuen, Y. P. Chai, and R. T. H. Li, "DC/DC converter with an integration of phase-shift and LLC for wide output voltage range," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6, doi: 10.1109/PEAC.2018.8590481.
[19] Z. Wu, Z. Wang, T. Liu, W. Xu, C. Chen, and Y. Kang, "A high efficiency and high power density partial power regulation topology with wide input range," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2074–2091, Feb. 2023, doi: 10.1109/TPEL.2022.3207526.
[20] H. Wu, C. Wan, K. Sun, and Y. Xing, "A high step-down multiple output converter with wide input voltage range based on quasi two-stage architecture and dual-output LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1793–1796, Apr. 2015, doi: 10.1109/TPEL.2014.2349917.
[21] M. I. Shahzad, S. Iqbal, and S. Taib, "A wide output range HB-2LLC resonant converter with hybrid rectifier for PEV battery charging," *IEEE Trans. Transp. Electrific.*, vol. 3, no. 2, pp. 520–531, Jun. 2017, doi: 10.1109/TTE.2017.2698243.
[22] Q. Cao, Z. Li, B. Xue, and H. Wang, "Fixed frequency phase shift modulated LLC resonant converter adapted to ultra wide output voltage range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 817–822, doi: 10.1109/APEC.2019.8722285.
[23] W. Sun, Y. Xing, H. Wu, and J. Ding, "Modified high-efficiency LLC converters with two split resonant branches for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7867–7879, Sep. 2018, doi: 10.1109/TPEL.2017.2773484.
[24] Y. Jang, M. M. Jovanovic, M. Kumar, J. M. Ruiz, R. Lu, and T. Wei, "Isolated, bi-directional DC-DC converter for fuel cell electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 1674–1681, doi: 10.1109/APEC.2019.8722067.
[25] C. Duan et al., "Design of a 2.5kW 400V→M2V high-efficiency DC/DC converter using a novel synchronous rectification control for electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1082–1086, doi: 10.1109/ECCE.2013.6646824.
[26] Z. Nie, W. D. Williams, C. Duan, W. Guo, and K. H. Bai, "System optimization of a high-power and high-step-down accessory power module for electric vehicles," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1926–1931, doi: 10.1109/APEC.2014.6803569.
[27] F. Beg, "A novel design methodology for a 1.5 KW DC/DC converter in EV and hybrid EV applications," *Int. J. Electr. Comput. Eng.*, vol. 8, pp. 1497–1500, 2014.
[28] P. Xuewei and A. K. Rathore, "Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated dc/dc converters low voltage high current applications," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, 2014, pp. 2566–2571, doi: 10.1109/ISIE.2014.6865024.
[29] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC-DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006, doi: 10.1109/TPEL.2005.869730.
[30] M. R. Ahmed and Y. Li, "A low-cost, high-power-density DC-DC converter for hybrid and electric vehicle applications," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. P.1–P.8, doi: 10.23919/EPE.2019.8914879.
[31] L. Zhu, H. Bai, A. Brown, and M. McAmmond, "Design a 400 V–12 V 6 kW bidirectional auxiliary power module for electric or autonomous vehicles with fast precharge dynamics and zero DC-bias current," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5323–5335, May 2021, doi: 10.1109/TPEL.2020.3028361.
[32] L. Zhu, H. Bai, A. Brown, and M. McAmmond, "Two-stage vs one-stage design for a bidirectional 400V/12V 6kW auxiliary power module in electric vehicles," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2020, pp. 1222–1226, doi: 10.1109/ITEC48692.2020.9161459.
[33] N. Zanatta, T. Caldognetto, D. Biadene, G. Spiazzi, and P. Mattavelli, "Design and implementation of a two-stage resonant converter for wide output range operation," *IEEE Trans. Ind. Appl.*, vol. 58, no. 6, pp. 7457–7468, Nov./Dec. 2022, doi: 10.1109/TIA.2022.3199195.
[34] Z. Lu, G. Xu, W. Xiong, Y. Sun, and M. Su, "A quasi two-stage isolated bidirectional buck-DAB converter for wide input voltage range," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1384–1390, Feb. 2023, doi: 10.1109/TPEL.2022.3208105.
[35] Y. Li, S. Shao, H. Chen, J. Zhang, and K. Sheng, "An IPOS LLC converter with current sharing capability," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1283–1287, doi: 10.1109/ECCE.2019.8913290.
[36] Y. Li, S. Shao, H. Chen, J. Zhang, and K. Sheng, "High-gain high-efficiency IPOS LLC converter with coupled transformer and current sharing capability," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 63–73, Mar. 2020, doi: 10.24295/CPSSTPEA.2020.00006.
[37] J. Sun, X. Tang, Y. Xing, B. Chen, H. Wu, and K. Sun, "Current sharing control of interleaved LLC resonant converter with hybrid rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2223–2227, doi: 10.1109/APEC.2019.8721810.
[38] J. Afsharian, D. Xu, N. Zhu, B. Gong, and Z. Yang, "A modular stacked transformer structure for LLC resonant converters and analysis of current sharing behavior in parallel PCB windings," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 1–8, doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8797177.
[39] D. Sha, J. Zhang, and K. Liu, "Leakage inductor current peak optimization for dual-transformer current-fed dual active bridge DC-DC converter with wide input and output voltage range," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6012–6024, Jun. 2020, doi: 10.1109/TPEL.2019.2952650.
[40] H. S. Gohari, S. Abbasian, N. A. Mardakheh, K. Abbaszadeh, and F. Blaabjerg, "Coupled inductor-based current-fed ultra-high step-up DC-DC converter featuring low input current ripple," *IEEE Trans. Circuits Syst. II, Express Briefs*, to be published, doi: 10.1109/TCSII.2022.3206231.
[41] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004, doi: 10.1109/TPEL.2003.820550.
[42] H. Watanabe and J.-I. Itoh, "Development of current-fed DAB converter applying triangular current mode for wide voltage applications," *IEEJ J. Ind. Appl.*, vol. 12, pp. 726–734, 2023, doi: 10.1541/ieejjia.22008043.
[43] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC-DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015, doi: 10.1109/TIE.2015.2432093.
[44] D. Sha, X. Wang, K. Liu, and C. Chen, "A current-fed dual-active-bridge DC-DC converter using extended duty cycle control and magnetic-integrated inductors with optimized voltage mismatching control," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 462–473, Jan. 2019, doi: 10.1109/TPEL.2018.2825991.
[45] Z. Guo, K. Sun, T.-F. Wu, and C. Li, "An improved modulation scheme of current-fed bidirectional DC–DC converters for loss reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4441–4457, May 2018, doi: 10.1109/TPEL.2017.2719722.
[46] K. Tashiro, Y. Okagawa, K. Zhang, Y. Yamada, S. Tachizaki, and S. Takahashi, "Downsizing of in-vehicle DC/DC converters with GaN devices," *Automotive*, 2020, Art. no. 6.
[47] BorgWarner, "Gen5 high voltage DC/DC," Auburn Hills, MI, USA, 2022.
[48] Eaton, "DC–DC-converter-data-sheet-brochure-emob0008-en-us," Accessed on: Oct. 18, 2022. [Online]. Available: https://www.eaton.com/content/dam/eaton/products/emobility/power-electronics/dc-dc-converters/eaton-dcdc-converter-data-sheet-brochure-emob0008-en-us.pdf
[49] Bosch, "High-voltage DC/DC converter generation 3evo," Accessed on: Oct. 18, 2022. [Online]. Available: https://www.bosch-mobility-solutions.com/en/solutions/power-electronics/high-voltage-dc-dc-converter-generation-3evo/

[50] Vitesco Technologies, "High voltage DC/DC converter—4th generation," Accessed on: Oct. 19, 2022. [Online]. Available: https://www.vitesco-technologies.com/en-us/products/high-voltage-dc-dc-converter-4th-generation
[51] Bel Fuse, "700DNC40-12 - 4000W, 12V, DC-DC HEV down converter," Accessed on: Oct. 19, 2022. [Online]. Available: https://www.belfuse.com/product-detail/power-solutions-custom-value-added-solutions-emobility-700dnc40-down-converter?navCategory=eMobilityDcdcConverters
[52] C.-Y. Chen, T.-J. Liang, K.-F. Liao, K.-H. Chen, and Y.-H. Yeoh, "Design and implementation of two-stage boost and full-bridge resonant converter for wide-range APMs," in *Proc. IEEE Int. Future Energy Electron. Conf.*, 2021, pp. 1–6, doi: 10.1109/IFEEC53238.2021.9662017.
[53] H. P. Kieu, D. Lee, S. Choi, and S. Kim, "A 700kHz 800V/14V GaN-based DC-DC converter with optimized integrated transformer for electrical vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5549–5553, doi: 10.1109/ECCE47101.2021.9595023.
[54] Y. Chen, W. Liu, A. Yurek, X. Zhou, B. Sheng, and Y.-F. Liu, "Design and optimization of a high power density low voltage DC-DC converter for electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 1244–1251, doi: 10.1109/ECCE44975.2020.9235889.
[55] X. Xu, Y. Zhang, L. Zhu, H. Yu, Y. Zhang, and H. Wu, "A high step-down DC-DC converter with matrix-transformer and wide voltage gain for vehicle power supply applications," in *Proc. 22nd Int. Conf. Elect. Mach. Syst.*, 2019, pp. 1–6, doi: 10.1109/ICEMS.2019.8922407.

Liyan Zhu (Member, IEEE) received the B.S. degree from the Kunming University of Science and Technology, Kunming, China, in 2017, and the Ph.D. degree from the University of Tennessee, Knoxville, TN, USA, in 2022, both in electrical engineering.

He is currently a Research Scientist with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. His research interests include WBG-based dc/dc converters, magnetic components, auxiliary power modules, and integrated chargers for electric vehicles.

Hua Bai (Senior Member, IEEE) received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2002 and 2007, respectively.

In 2010, he joined Kettering University (former General Motor Institute) as an Assistant Professor and has been an Associate Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN, USA, since 2018. His research interests include power electronics (particularly wide-bandgap devices) with motor drives, electric vehicle battery chargers, auxiliary power modules, and battery energy storage systems. He is the author of 2 books, 140 IEEE papers, and holds more than 20 industrial patents. He is an Associate Editor for the *SAE International Journal of Electrified Vehicles* and IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION.

Alan Brown received the B.Sc. degree in electrical engineering from Michigan State University, East Lansing, MI, USA, in 1992.

He is currently a Senior Power Electronics Engineer with HELLA Electronics Center, Northville, MI USA. His responsibilities include the development of high-power dc/dc converters, ac/dc onboard chargers, and fuel-saving technologies for micro and mild hybrids.