Improved Double Pulse Test for Accurate Dynamic Characterization of Medium Voltage SiC Devices

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***Abstract*—This article presents an improved double pulse test (DPT) for accurate dynamic characterization of the medium voltage (MV) silicon carbide device. The difference between low voltage (LV) and MV DPT setup grounding is first introduced, which results in different measurement considerations. Then, parasitic capacitances in the DPT and their impact on the DPT are discussed considering different grounding points and device connections. Approaches are proposed to minimize the impact of parasitic capacitances on DPT results. In addition, the impact of switching V-I timing alignment on the testing results is discussed, compared to that in the LV DPT; a V-I alignment approach is introduced for the MV DPT. A 10 kV/20 A SiC MOSFET-based DPT is taken as an example of the improved DPT, and test results show that it can minimize the impact from parasitic and improve the accuracy of the device switching loss estimation.**

***Index Terms*—Double pulse test (DPT), medium voltage (MV), parasitic capacitance, silicon carbide (SiC), switching V-I timing alignment.**

I. Introduction

THE double pulse test (DPT) is a widely used approach to characterize the dynamic performance of power devices, and its methodology and considerations are already fully discussed for low voltage (LV) conditions, including for conventional Si devices [1], [2] and wide band-gap devices [3], [4], [5], [6], [7]. With the development of medium voltage (MV) silicon carbide (SiC) devices, the dynamic characterization of these MV devices is critical for device performance estimation and converter design. Note that in this article, LV refers to < 1 kV dc bus voltage and MV refers to >1 kV, although the examples for MV condition used refer to dc bus voltages around 6 to 7 kV.

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There have been some MV SiC device characterization work using the MV DPT setup, including 3.3 kV SiC MOSFET [8], [9], 10 kV SiC MOSFET [9], [10], [11], [12], 15 kV SiC MOSFET [13], [14], and 15 kV SiC IGBT [15]. MV DPT setup has some differences from the LV DPT setup. However, these are rarely discussed in the literature.

First, the grounding configuration of the MV DPT setup is different from that of the LV DPT setup. The negative polarity of the MV dc power supply is commonly grounded together with its chassis for insulation and safety considerations. Using passive voltage probes for measurement introduces another grounding point through the oscilloscope [9], [10], [11], [12]. The multiple grounds introduce voltage potential differences among them, and thus noise occurs in the measurements, which has been discussed in [16]. Therefore, multiple grounds need to be avoided in the MV DPT setup, which requires probe selection considerations.

Second, the impact of parasitic capacitance on the MV DPT is critical because of the high voltage. The impact of parasitic capacitance on the device or converter loss has been discussed in both the MV and LV applications. In [17], the impact of load inductor parasitic capacitance on the switching performance of the 10 kV/20 A SiC MOSFET is discussed. It shows that a larger load inductor parasitic capacitance results in a higher turn-ON energy loss and a lower turn-OFF energy loss. For example, the energy of a 27 pF capacitance at 6.25 kV is 0.53 mJ, and it results in an $\sim$11% increase of the turn-ON energy loss (@10 A load current). In [18], it is found that the estimated converter loss does not match with the experiment results unless taking the loss induced by the printed circuit board (PCB) parasitic capacitance into consideration. In [19], the impact of parasitic capacitance, introduced by the PCB and the load inductor, on the DPT of a LV GaN device is discussed, and the extra loss introduced by the parasitic capacitance is derived to be the total energy stored in the parasitic capacitance. However, these works do not give a clear approach to minimize the impact of parasitic capacitance on DPT results.

Third, compared to the LV DPT, the switching V-I timing alignment of the MV DPT, considering the propagation delay difference between the voltage and current probes, is more difficult. The widely used approach in the LV DPT is to align the initial drain-source voltage dip point with the source current increasing point based on the principle of voltage drop on the stray inductance because of *di/dt* [3]. However, for MV DPT, compared to the whole dc-link voltage, the voltage drop on the

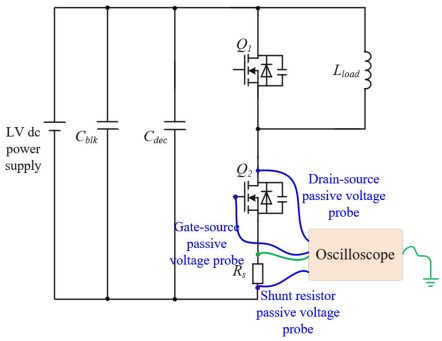


Fig. 1. Schematic of the typical LV DPT circuit.

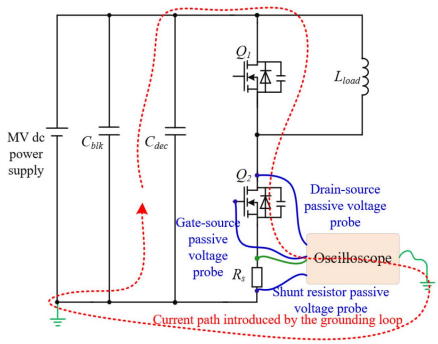


Fig. 2. Schematic of MV DPT setup with grounding loop.

stray inductance is small and the drain-source voltage dip point is difficult to identify. Therefore, another switching V-I timing alignment approach for MV DPT is needed.

Based on the abovementioned review and discussion, the focus and contributions of this article are as follows:

1) identifying the differences between the LV DPT and the MV DPT in terms of the setup, grounding, parasitic capacitance, measurement, and data analysis;
2) discussion of the parasitic capacitances in the DPT setup and their impact on the DPT results;
3) DPT setup improvement for parasitic capacitance reduction and more accurate DPT results;
4) improved data analysis approach to minimize the impact of parasitic capacitances on the MV switching loss calculation.

The rest of this article is organized as follows. The grounding configuration difference between the MV DPT and the LV DPT and its impact on the measurement are discussed in Section II. The impact of parasitic capacitances on the DPT and approaches to minimize the impact and improve the test accuracy are introduced in Section III. In Section IV, a switching V-I timing alignment approach for the MV DPT is proposed. In Section V, the DPT setup and test results of the 10 kV/20 A SiC MOSFET are presented as an example for experimental verification. Some discussions are given in Section VI. Finally, Section VII concludes this article.

A. Grounding Difference and Measurement Considerations

A. Grounding Configuration Difference

The schematic of the typical LV DPT circuit is shown in Fig. 1. The shunt resistor R_s is used to detect the DUT (Q_2) source current, and passive voltage probes are preferred to measure the DUT drain-source voltage, gate-source voltage, as well as shunt resistor voltage because of their high bandwidth. Since passive probes are nonisolated and are grounded internally through the oscilloscope, the DPT setup is grounded through the oscilloscope. In addition, the dc output terminals of the LV dc power supply are mostly not grounded. Therefore, the LV DPT setup only has one grounding point through the oscilloscope.

Compared to the LV DPT setup, the MV DPT setup has a different grounding point. The negative dc terminal of the MV dc power supply is grounded internally, together with its chassis. Then, if passive voltage probes are used for the DUT voltage and current measurement, grounding through the oscilloscope will be introduced, as shown in Fig. 2. The grounding of the oscilloscope provides another path for the switching current, as indicated in the dashed red line. As a result, the device source current "leaks" through the oscilloscope grounding path and returns to the dc-link capacitor through the MV power supply grounding wire, which results in the current measurement error. Besides, the current flowing through the oscilloscope grounding path affects the measurement accuracy of the oscilloscope [3]. Since the DPT switching transient current is mainly provided by the decoupling capacitor C_{dec}, putting C_{dec} as close as possible to the DUT source terminal minimizes the stray inductance of the switching current returning path so that the current flowing through the grounding loop can also be reduced. However, the grounding loop is highly susceptible to noise coupling, which causes a voltage drop on the grounding loop and affects the measurements of the oscilloscope.

In [3], to alleviate the issues caused by the CM loop in the LV DPT setup, which has a similar condition as this grounding loop, two methods are introduced: one is applying CM chokes on the dc power supply side, and the other is isolating the oscilloscope, i.e., not grounding the oscilloscope. In the MV DPT setup, however, neither of the approaches is preferred. First, developing a CM choke for MV application is not easy due to the insulation consideration. Second, not grounding the oscilloscope could lead to safety hazards, since high voltage potential may exist on some parts that could be touched by people, such as the chassis and the communication terminal. In fact, ungrounded oscilloscopes should also not be used for LV setup.

B. Measurement Considerations

Using isolated current and voltage measurements can eliminate the grounding loop. Then, the MV DPT setup is only grounded through the MV dc power supply, as shown in Fig. 3.

The main concerns for using differential probes are the relatively low bandwidth and large measurement loops, which couple with noise.

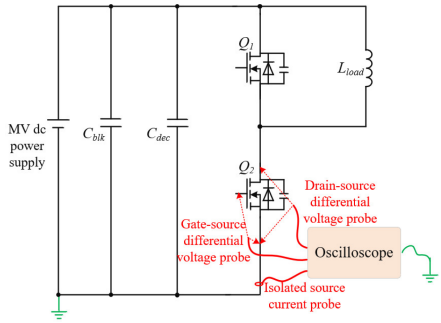


Fig. 3. Schematic of MV DPT setup without the grounding loop.

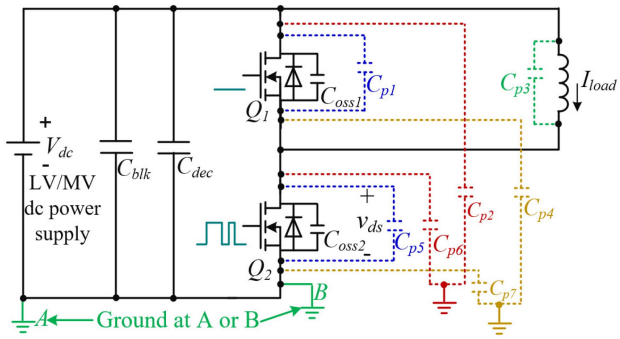


Fig. 4. Parasitic capacitances in the DPT setup.

The signal equivalent frequency, which is determined based on the rise/fall time, determines the bandwidth requirement for the probe [3]. Compared to LV SiC MOSFET, the MV SiC MOSFET has a similar or even higher *dv/dt*. However, the high dc-link voltage in the MV DPT results in a larger v_{ds} rise/fall time and, thus, a lower probe bandwidth requirement. For example, for 10 kV SiC MOSFET with a dc-link voltage of 7.0 kV and a *dv/dt* of 250 V/ns, which is the maximum switching speed shown in the literature [20], the rise/fall time is 28 ns. Then, the minimum bandwidth requirement for the v_{ds} probe is 62.5 MHz based on the calculation in [3]. Therefore, a MV differential probe, such as CIC DP20-10K, which has a bandwidth of 120 MHz, can be used for the v_{ds} measurement. For the measurement loop concern, the MV passive probe also has a large measurement loop compared to that of the LV passive probe due to the insulation requirements (clearance and creepage). Therefore, the difference between the MV differential probe and the passive probe is smaller than that in the LV condition. Minimizing the measurement loop while still maintaining the insulation requirement and placing the measurement loop away from the noise area (mostly the switching node area) can help with minimizing the coupled noise. For example, CIC DP20-10K has two 406 mm long probe leads, and the distance between them on the probe is around 90 mm. To measure a 7 kV voltage, the two probe leads can be put at 7 mm away considering the clearance distance in the air (IEC 61800-5-1). Because the creepage distance at the probe lead terminal must be 90 mm, by putting the two probe leads as close as possible, the measurement loop area can be reduced from 365 cm^2 to 89 cm^2. Moreover, since the measured voltage is high, the impact of the coupled noise is negligible, which can be observed from the later DPT waveform.

The DUT current rise/fall time depends on the load current and the *di/dt*, which are not directly dependent on the voltage level. Therefore, the MV DPT, like the LV DPT, may also require a high bandwidth current measurement, depending on the DUT characteristics and the switching speed. Considering the device package and setup layout, different isolated current probes can be used. The coaxial shunt provides the highest bandwidth, and optical-based isolated voltage probes with high bandwidth, such as the Tektronix TIVP1, which has a bandwidth of 1 GHz, can be used to avoid the grounding through the oscilloscope. If the required bandwidth is not too high, a split-core current probe, such as the Tektronix TCP0030A with 120 MHz bandwidth, can be considered if the setup allows this type of connection. If the required bandwidth is lower than 50 MHz, the Rogowski coil, such as CWTMini50HF, can be adopted because it is easy to use. However, besides the low bandwidth, the Rogowski coil is also easy to couple with noise, so minimizing the measurement loop is preferred.

MV SiC devices have relatively large gate-source capacitance C_{gs}. For example, the C_{gs} of the Wolfspeed 10 kV/20 A discrete SiC MOSFET and the 10 kV/100 A power module are 4.7 nF [11] and 40 nF [10], respectively. Based on the recommended gate resistance values, which are 15 Ω and 2 Ω, respectively, the rise time of gate-source voltage v_{gs}, can be estimated, and the required bandwidths are 11 MHz and 10 MHz, respectively. Therefore, the LV differential probe, such as Tektronix TMDP0200, which has a bandwidth of 200 MHz, can meet the bandwidth requirement. However, compared to the v_{ds} measurement, the v_{gs} measurement is more sensitive to the noise since the signal voltage is low. Thus, minimizing the measurement loop, such as twisting the two probe terminals (since no insulation concern), is recommended. Alternatively, the optically isolated voltage probe is a better choice because of its small measurement loop and high noise immunity capability.

The bandwidth requirements, probes and examples, pros and cons of the MV DPT measurement approaches for DUT v_{ds}, i_{ds}, and v_{gs} are summarized in Table I.

III. Impact Analysis of Parasitic Capacitances and Approaches to Minimize

The parasitic capacitance exists between any two insulated conductive parts in the DPT setup. During switching transients, parasitic capacitances connected to the switching node are charged or discharged, and the charging or discharging current flows through the DPT circuit, affecting the DPT and the measurement results.

A. Parasitic Capacitances in the DPT Setup

The major parasitic capacitances in the DPT setup for the device with a noninsulated baseplate, i.e., the device baseplate is internally connected to its drain terminal, are shown in Fig. 4. The discussion for the device with an insulated baseplate will be provided later. C_{p1} and C_{p5} are the capacitances between the upper or the lower device's baseplate and their PCB source

TABLE I
SUMMARY OF MV DPT MEASUREMENT APPROACHES

Signal	Bandwidth requirement	Probes and examples	Pros	Cons
DUT voltage, v_{ds}	Moderate (≥60 MHz)	MV differential voltage probes, e.g., CIC DP20-10K, 120 MHz	Galvanic isolation	Long probe leads and large measurement loop
DUT current, i_{ds}	Depends on devices	Coaxial shunt + optical-based isolated voltage probes, e.g., TIVP1, 1 GHz	High bandwidth and galvanic isolation	Expensive and special connection for shunt
		Split core current probes, e.g., TCP0030A, 120 MHz	Moderate bandwidth and cheap	Special connection for the probe
		Rogowski coils, e.g., CWTMini50HF, 50 MHz	Cheap and easy for connection	Low bandwidth and noise sensitive
DUT Gate, v_{gs}	Low (≥11 MHz)	LV differential voltage probes, e.g., TMDP0200, 200 MHz	Galvanic isolation	Long probe leads and large measurement loop
		Optical-based isolated voltage probes, e.g., TIVP1, 1 GHz	High bandwidth, galvanic isolation, and small measurement loop	Expensive

polygon, respectively; $C_{\rm p2}$ and $C_{\rm p6}$ are the capacitances between the upper or the lower device's baseplate and the hotplate, respectively; $C_{\rm p3}$ is the equivalent parallel capacitance (EPC) of the load inductor; $C_{\rm p4}$ and $C_{\rm p7}$ are the isolation capacitances of the gate drive power supply (GDPS) for the upper and lower device, respectively. Since $C_{\rm p2}$ and $C_{\rm p7}$ are not connected to the switching node, their voltages are constant and their impact on the DPT can be neglected.

The capacitance of the GDPS depends on the GDPS isolated transformer design, and the typical value is in the range of 1–5 pF for both LV and MV applications [21], [22], [23]. The capacitance between the PCB and the device baseplate depends on the PCB layout and mechanical relationship. The parasitic capacitance introduced by the hotplate depends on the device baseplate area, the hotplate baseplate area, the distance between the device and the hotplate, as well as the insulation material between the device and the hotplate.

Once the load inductor is built, the inductor EPC can be determined based on the measured resonant frequency and inductance with an impedance analyzer [24]. However, the calculated EPC value is a lumped value to meet the impedance performance of the inductor in the frequency domain. It is not accurate for use in the fast transient, like the SiC switching transients. Therefore, the distributed model is needed. Treating each winding turn as one unit, each turn has its resistance, leakage inductance, and mutual inductance with other turns [25]. The parasitic capacitance exists between any two turns and between each turn and the core. When a voltage change is applied on the inductor terminals, because of the inductance and resistance, the capacitance closing to the two terminals will see the voltage change first, which results in charging/discharging current flowing through them. Then, the voltage change spreads to the second turn, third turn, and so on, getting other parasitic capacitances into the charging/discharging loop. Therefore, the equivalent capacitance of the inductor during the fast-switching transient is different from the calculated lumped EPC.

B. Impact on the MV DPT

During the turn-ON transient of the DUT, the switching node voltage drops from $V_{\rm dc}$ to 0. During this period C_{oss1}, C_{p1}, and C_{p3} are charged, while C_{oss2}, C_{p4}, C_{p5}, and C_{p6} are discharged.

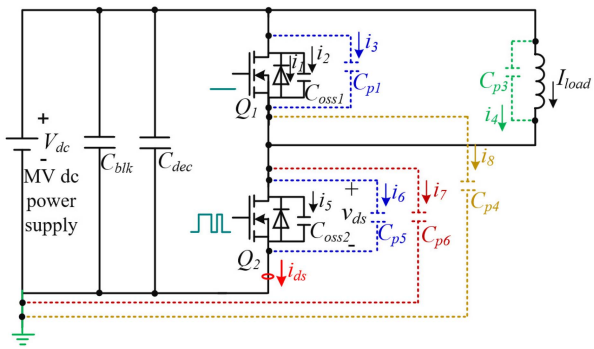


Fig. 5. Currents of parasitic capacitances in the MV DPT setup.

Conversely, during the turn-OFF transient, the switching node voltage increases from near 0 to $V_{\rm dc}$. In this period, C_{oss1}, C_{p1}, and C_{p3} are discharged, and C_{oss2}, C_{p4}, C_{p5}, and C_{p6} are charged. The charging and discharging currents are shown in Fig. 5: i_1 is the reverse recovery current of the upper device's body diode, which is neglectable in the SiC MOSFET; i_2, i_3, i_4, i_5, i_6, i_7, i_8 are the current of C_{oss1}, C_{p1}, C_{p3}, C_{oss2}, C_{p5}, C_{p6}, C_{p4}, respectively, and their positive directions are all defined as their charging directions.

During the turn-ON transient, since i_5 and i_6 flow through the DUT channel but do not go through the current probe for DUT source current measurement, the measured DUT source current during the turn-ON transient is

$$i_{ds\_\rm on} = I_{\rm load} + i_1 + i_2 + i_3 + i_4 - i_7 - i_8. \tag{1}$$

Assuming no parasitic capacitance exists, then the ideal measured DUT source current during the turn-ON transient should be

$$i_{ds\_\rm on\_ideal} = I_{\rm load} + i_1 + i_2. \tag{2}$$

Therefore, the extra current induced by parasitic capacitances during the turn-ON transient is

$$i_{ds\_\rm on\_ext} = i_3 + i_4 - i_7 - i_8. \tag{3}$$

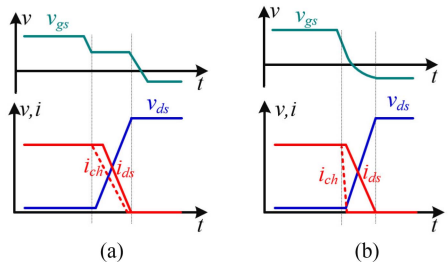


Fig. 6. Typical turn-OFF current and voltage waveforms with (a) large gate resistance and (b) small gate resistance (ZVS).

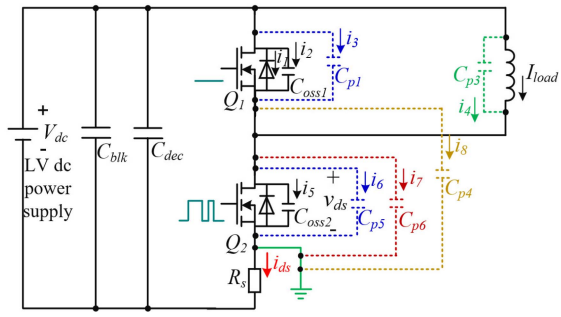


Fig. 7. Currents of parasitic capacitances in the LV DPT setup.

From (3), since i_3 and i_4 are positive while i_7 and i_8 are negative during the DUT turn-ON transient, these parasitic capacitances result in a larger measured DUT source current, and thus a larger turn-ON energy loss.

During the turn-OFF transient, the charging and discharging currents are provided by the load inductor current, which is treated as constant during the short switching transient. Thus, the measured DUT source current during the turn-OFF transient is

$$i_{ds\_off} = I_{\text{load}} + i_2 + i_3 + i_4 - i_7 - i_8. \tag{4}$$

Assuming there is no parasitic capacitance, Then, the measured DUT source current during the turn-OFF transient is

$$i_{ds\_off\_ideal} = I_{\text{load}} + i_2. \tag{5}$$

Nevertheless, the impact of parasitic capacitance on the turn-OFF transient depends on the turn-OFF speed of the device channel. When the turn-OFF gate resistance is large so that the turn-OFF speed of the channel is slow, the overlap between the device channel current i_{ch}, and v_{ds} results in switching loss, as shown in Fig. 6(a). In this case, the extra current induced by the parasitic capacitance during the turn-OFF transient is

$$i_{ds\_off\_ext} = i_3 + i_4 - i_7 - i_8. \tag{6}$$

During the turn-OFF transient, i_3 and i_4 are negative, and i_7 and i_8 are positive. Therefore, these parasitic capacitances result in a smaller measured DUT channel current during the turn-OFF transient, and smaller calculated turn-OFF energy loss.

However, when the turn-OFF gate resistance is small, the device channel is quickly turned off before v_{ds} starts to increase, as shown in Fig. 6(b). There is no overlap between i_{ch} and v_{ds}, and zero voltage switching (ZVS) is achieved. After the device channel is turned OFF, the device performs as a nonlinear capacitor, i.e., C_{oss2}, and v_{ds} increase as C_{oss2} is charged by i_{ds}. In this case, the turn-OFF energy loss is

$$E_{\text{off}} = \int_0^{t_{vr}} v_{ds} i_{ds} dt = \int_0^{t_{vr}} v_{ds} C_{oss2}(v_{ds})\, dv_{ds} \tag{7}$$

where t_{vr} is the rise time of v_{ds} during the turn-OFF transient. Therefore, the calculated turn-OFF loss is not related to i_{ds}, so the current flowing through the parasitic capacitance does not affect the energy loss result.

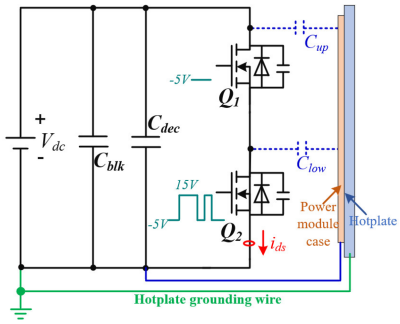


Fig. 8. DPT connection of devices with insulated baseplates.

C. Impact on the LV DPT

Because of the different grounding points, the impact of parasitic capacitances on the LV DPT is different. As shown in Fig. 7, since the setup is grounded at the DUT source terminal through the oscilloscope, and the current measurement, which could be a shunt resistor, is between the grounding point and the negative dc terminal, the measured current during turn-ON transient is

$$i_{ds\_on} = I_{\text{load}} + i_1 + i_2 + i_3 + i_4 \tag{8}$$

and the measured current during the turn-OFF transient is

$$i_{ds\_off} = I_{\text{load}} + i_2 + i_3 + i_4. \tag{9}$$

Comparing (8) and (1), (9) and (4), respectively, the impact of C_{p1} and C_{p3} still exists, which is the same as that in the MV DPT case. However, the impact of C_{p4} and C_{p6} is eliminated.

D. Devices With Insulated Baseplates

For devices with insulated baseplates, such as power modules, the configuration of parasitic capacitance introduced by the hotplate is different from the case with noninsulated baseplates. Take a half-bridge module as an example, as shown in Fig. 8. C_{up} and C_{low} are the capacitances between the module baseplate and the upper and lower device, respectively. These two capacitances are the module's intrinsic capacitances and do not need to be excluded from the DPT since they also exist in the real converter. To avoid the impact from the hotplate and its grounding path, the power module baseplate can be connected to a constant

voltage point, such as the dc-link negative bus, positive bus, or middle point. This method bypasses the hotplate grounding loop and minimizes the charging/discharging loop inductance and resistance, and thus resonance can be avoided.

E. Discussion of Switching Loss Introduced by Parasitic Capacitance

In some literature, such as [18], [19], the extra loss introduced by the parasitic capacitance is concluded to be

$$E_{ext} = \frac{1}{2} C_p V_{\rm dc}^2 \tag{10}$$

where C_p is the parasitic capacitance. Because of the inductance and resistance in the parasitic capacitance charging/discharging loop, during the device turn-ON process, the capacitance's voltage does not directly change from $V_{\rm dc}$ to 0; instead, there is a resonance between the parasitic capacitance and loop inductance, with damping provided by the resistance. If the resonance ends within the switching transient, (10) can be used to estimate the extra energy loss introduced by the parasitic capacitance. However, if the resonance does not end in the switching transient, using (10) to estimate the extra energy loss introduced by the parasitic capacitance results in an overestimated parasitic capacitance-related loss.

F. Approaches to Reduce the Impact of Parasitic Capacitances

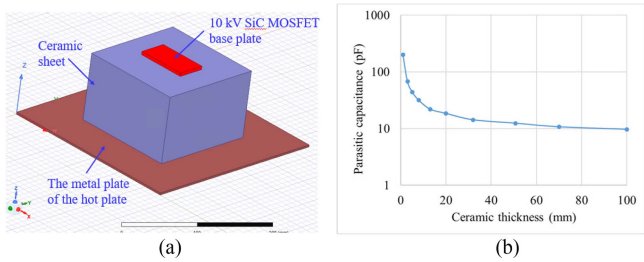
The straightforward approach is to minimize the parasitic capacitance. For PCB-related parasitic capacitances, they can be minimized through PCB layout improvement. The GDPS parasitic capacitance can also be minimized through a better GDPS isolated transformer design. For the load inductor, several inductors can be connected in series to reduce the total parasitic capacitance. Also, for each inductor, it is preferred to have only one layer of winding to minimize the interwinding capacitance [3]. The capacitance between two parallel electric conductive plates can be calculated as

$$C = \frac{\varepsilon A}{d} \tag{11}$$

where ε, A, and d are the permittivity of the material, effective area, and distance between the two polarities of the capacitance, respectively. According (11), the hotplate-related parasitic capacitance can be reduced through one or more options as follows:

1) using a smaller hotplate, which can reduce the effective area between the hotplate and the DUT;
2) using an insulation sheet with smaller permittivity;
3) using a thick insulation sheet, which increases the distance between the DUT and the hotplate.

Commonly, the device baseplate area is smaller than the hotplate baseplate area, which makes the capacitance estimation different from the ideal case of two parallel equal-area conductive sheets. Besides, the insulation material may not fill the whole space between the device and the hotplate, and thus, the capacitance is the paralleling of an insulation material-based capacitance and an air-based capacitance. There is a nonlinear relationship between the parasitic capacitance and the insulation sheet thickness. This can be obtained through finite element-based simulation, such as Ansys Maxwell. As shown in Fig. 9(a), the parasitic capacitance between the 10 kV/300 mΩ SiC MOSFET baseplate and the hotplate is simulated with Maxwell. Fig. 9(b) shows the parasitic capacitance with different hotplate thickness. The parasitic capacitance decreases slowly as the ceramic thickness increases.



(a) (b)

Fig. 9. Hot plate parasitic capacitance analysis: (a) simulation model and (b) relationship between simulated parasitic capacitance and the ceramic sheet thickness.

However, parasitic capacitances cannot be totally eliminated. To further reduce the impact of parasitic capacitances, their currents can be measured and subtracted from the measured DUT source current.

Take the MV device DPT setup with the noninsulated baseplate, as shown in Fig. 5, as an example. Based on (1)–(3), during the turn-ON transient, the ideal DUT source current subtracting the contribution of parasitic capacitances is

$$i_{ds\_\text{on\_ideal}} = i_{ds\_\text{on}} - i_3 - i_4 + i_7 + i_8. \tag{12}$$

Similarly, Based on the previous analysis, during the turn-OFF transient, the ideal DUT source current subtracting the contribution of parasitic capacitances is

$$i_{ds\_\text{off\_ideal}} = \begin{cases} i_{ds\_\text{off}} - i_3 - i_4 + i_7 + i_8 \; Not\; ZVS \\ i_{ds\_\text{off}} \; ZVS \end{cases}. \tag{13}$$

Then, the switching energy can be calculated as

$$\begin{cases} E_{\text{on}} = \int_t^{t+t_{\text{on}}} v_{ds} i_{ds\_\text{on\_ideal}}\, dt \\ E_{\text{off}} = \int_t^{t+t_{\text{off}}} v_{ds} i_{ds\_\text{on\_ideal}}\, dt \end{cases} \tag{14}$$

where t_{ON} and t_{OFF} are the turn-ON and turn-OFF switching transient period, respectively.

The current flowing through the PCB-related parasitic capacitance is difficult to measure. When the capacitance is small, it can be neglected. However, when the capacitance is not negligible, it can be estimated with (10) since the loop is small and, thus, small loop inductance and resistance. The currents of the capacitance introduced by the hotplate and GDPS can be easily measured with current probes by either clamping the grounding wire or clamping the whole power cord. The current flowing through the inductor parasitic capacitance needs to be calculated based on the measured inductor current and the ideal inductor current, which can be estimated as

$$i_{4\_\text{ideal}} = I_0 + \int_t^{t+t_{sw}} \frac{V_{\rm dc} - v_{ds}(t)}{L} dt \tag{15}$$

where I_0 is the inductor current at the moment v_{ds} starts to change; t_{sw} is the switching period; L is the inductance.

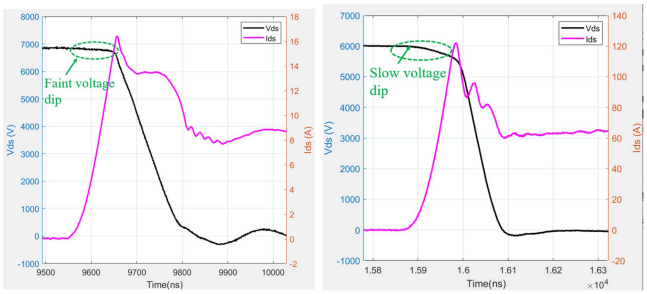


Fig. 10. Voltage dip on the drain-source voltage during the turn-ON transient of (a) 10 kV/20 A SiC MOSFET and (b) 10 kV/120 A SiC module.

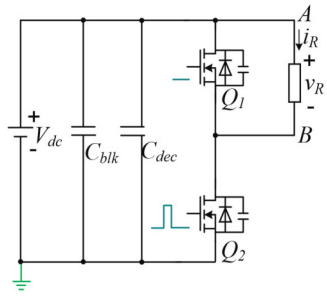


Fig. 11. Probe delay difference test circuit.

IV. Switching V-I Timing Alignment

A. V-I Misalignment in the MV DPT

The V-I misalignment leads to error in the switching energy loss calculation. Compared to the LV DPT [3], the MV DPT has less sensitivity of V-I misalignment. Because the higher dc-link voltage results in a longer switching time, and thus, the same V-I misalignment leads to less error in percentage. However, it is still necessary to do the V-I alignment in the MV DPT. First, it increases the accuracy of the switching energy loss calculation. Second, to subtract the parasitic capacitance current from the measured DUT source current, the V-I alignment is also important, otherwise, the error could be accumulated. Third, if the difference in delay between the current probes and the MV voltage probe is large, a large error could still be introduced.

In the MV DPT, however, the switching waveform-based V-I alignment method does not work because the voltage drop caused by *di/dt* is very small compared to the high dc-link voltage. The turn-ON transient waveforms of a 10 kV/20 A SiC MOSFET are shown in Fig. 10(a). Due to the small voltage drop on the stray inductance, it is difficult to identify the voltage dip point and the V-I alignment cannot be accurately conducted. Even for the 10 kV/120 A SiC module, the v_{ds} drops slowly at the beginning of the current increase, as shown in Fig. 10(b), which makes it difficult to accurately align the voltage and current waveforms. Even with the mathematical method, i.e., calculating the derivative of the current waveform and matching it with the voltage, the V-I switching timing alignment with the waveforms is difficult to conduct.

B. Resistor-Based V-I Alignment Method

Using the voltage probe to measure the voltage of a resistor and the current probe to measure its current, the measured voltage and current waveform should have the same shape and the ratio of the value equals the resistance value. Based on this, a power resistor-based test method is used to measure the probe delay difference. As shown in Fig. 11, the load inductor in the MV DPT setup is replaced with a power resistor. The voltage probe is used to measure the resistor voltage, and current probes used in the MV DPT are all used to measure the resistor current. It is preferred to put the current probes at terminal A, rather than terminal B, to minimize the interference of the *dv/dt* to the probe measurement through the parasitic capacitance of probes.

It is critical to minimize the parasitic capacitance and stray inductance of the resistor so that its voltage and current are in phase. Therefore, noninductive resistors with plastic cases are preferred because of their small inductance and capacitance. Also, multiple resistors may be used in series/parallel, to meet the power rating and voltage insulation requirement. Different from the DPT control, only a single pulse for device Q_2 is needed in the test, and the pulse duration should at least cover the whole device switching transient. Also, the resistor transient power rating should be sufficient for the pulse duration.

If the stray inductance is not easy to be neglected, it can also be compensated with mathematical calculations. The resistor voltage and current meet the relationship of

$$v_R = Ri_R + L_s \frac{di_R}{dt} \tag{16}$$

where v_R is the resistor voltage; R is the resistance; i_R is the "real" current; L_s is the stray inductance. Knowing v_R, R, and L_s, the "real" current can be solved and then used as the reference for the current waveforms measured with current probes.

V. 10 kV/ 20 A SiC MOSFET-Based DPT Example

A. DPT Setup and Improvement

The 10 kV/20 A SiC MOSFET used in this article has the same package as the one discussed in [11], and its baseplate is the drain terminal. The DPT setup picture, before any improvement, is shown in Fig. 12. To conduct the dynamic characterization at different junction temperatures, the *WENESCO H0909AA* hotplate is used to regulate the temperature. A fiber optic temperature sensor is applied to the DUT baseplate to monitor its junction temperature, given that the temperature change of the DUT during the DPT test is very small and the case temperature is close to the junction temperature. For better drain terminal connection and mechanical support, the device is first mounted on a copper sheet, whose surface area is slightly larger than the device's baseplate area, and then they are attached to the hotplate through a 3 mm thick ceramic sheet for electrical insulation. The upper device Q_1 is floated from the hotplate since it does not need to be heated. Two MV GDPS are used to supply the two gate driver circuits, respectively. A MV inductor with a single layer winding is built with MV wires to minimize the parasitic

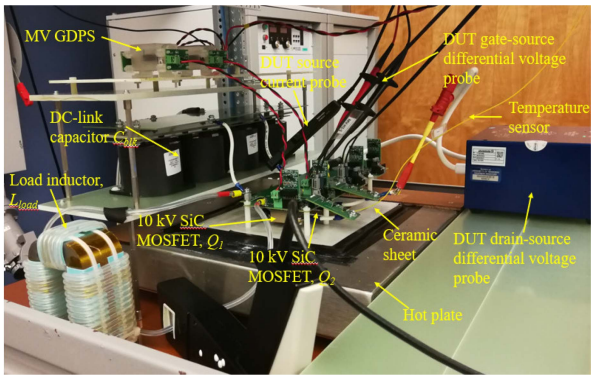


Fig. 12. Picture of the first version of the MV DPT setup.

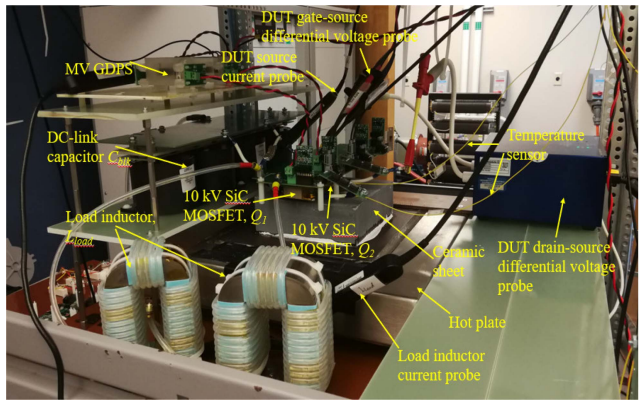


Fig. 14. Picture of the improved MV DPT setup.

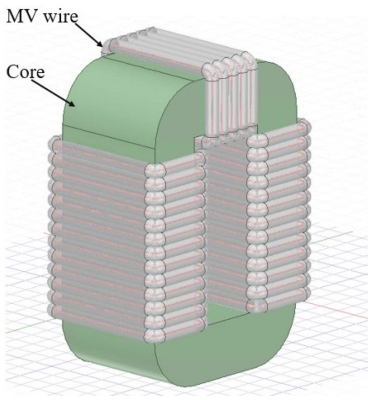


Fig. 13. Ansys/Maxwell3D DPT inductor model for parasitic capacitance simulation.

capacitance and maintain the insulation capability. Tektronix TCP0030A current probe is used to measure the DUT source current, and Tektronix LV differential probe TMDP0200 and CIC MV differential probe DP20-10K differential voltage probe are used to measure the gate-source and drain-source voltages, respectively. Tektronix MSO58 oscilloscope is used to obtain the measuring waveform and data. Spellman ST-20 MV dc power supply is utilized to supply the dc-link. Moreover, the MV dc power supply, hotplate, and oscilloscope are all internally grounded through their power cords, and the negative terminal of the GDPS's primary power rail is also grounded.

The capacitance between the PCB and device's baseplate, i.e., C_{p1} and C_{p5}, estimated through Ansys Maxwell, is 0.74 pF. GDPS-related capacitances, C_{p4} and C_{p7}, measured with the impedance analyzer E4990A, are 0.93 pF. The capacitance between the hotplate and the upper and lower devices, i.e., C_{p2} and C_{p6}, are 7.0 pF and 40.0 pF, respectively, which are also measured with the same impedance analyzer. The inductor EPC calculated based on the resonant frequency and the inductance, which are both measured with the same impedance analyzer, is 2.7 pF. However, a detailed DPT inductor model is developed in Ansys/Maxwell3D for parasitic capacitance simulation with each turn is a unit, as shown in Fig. 13. The core and the MV wire are modeled with the same size and material. Based on the simulation results, the capacitances between the core and the first and last turn are 5.13 pF and 5.17 pF, respectively, and capacitances between the core and middle turns vary between 3.6 pF and 4.2 pF, which means the transient parasitic capacitance introduced by the inductor could be higher than the calculated EPC value. Since the inductor and hotplate-related capacitances are larger than others, they are the focus of minimization in the following discussion.

To reduce the inductor-related capacitance, another MV inductor with only one layer of winding is developed and connected in series with the first one. To reduce the hotplate-related capacitance, a thicker ceramic sheet is adopted. Based on the simulation with Ansys Maxwell, a ceramic sheet with a thickness of 50.8 mm is selected considering the product availability, thermal resistance between the hotplate and the device, as well as the hotplate power capability. With this thick ceramic sheet, the parasitic capacitance between the DUT and the hotplate is reduced from 40 to 11 pF.

The improved DPT setup for the 10 kV/20 A SiC MOSFET is shown in Fig. 14. Moreover, to obtain currents flowing through the inductor and hotplate parasitic capacitances, the load inductor current and the hotplate grounding current are measured with Tektronix TCP0030A and TCP0150A current probes, respectively.

B. Probe Delay Difference Test

The dc-link voltage is set at 6 kV, and the pulse width is determined at 1 μs, which is around five times the switching transient period. Ten *Vishay* 100 Ω/150 W noninductive resistors (*LTO150F100R0JTE3*) are connected in series to be a 1 kΩ/ 1.5 kW resistance branch. The resistor current is around 6 A after the device is turned ON, and the transient power loss is 36 kW. For a 1 μs pulse current, each resistor can withstand 10 kW loss, so the resistor branch has a capability of 100 kW, which is higher than the real loss.

The parasitic is evaluated with the Keysight impedance analyzer *E4990A*. The measured inductance of the resistor branch is around 600 nH, and the impedance is 988.0 Ω at 1.5 MHz and 987.7 Ω at 15 MHz. The dv/dt of the 10 kV SiC MOSFET is around 50 V/ns, and with 6 kV dc-link voltage, the rise time is about

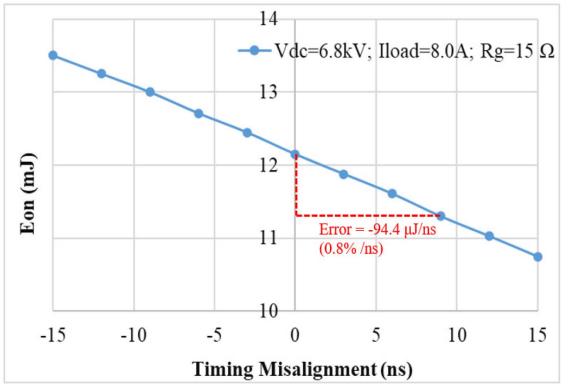


Fig. 15. Sensitivity of V-I misalignment for the 10 kV/20 A SiC MOSFET.

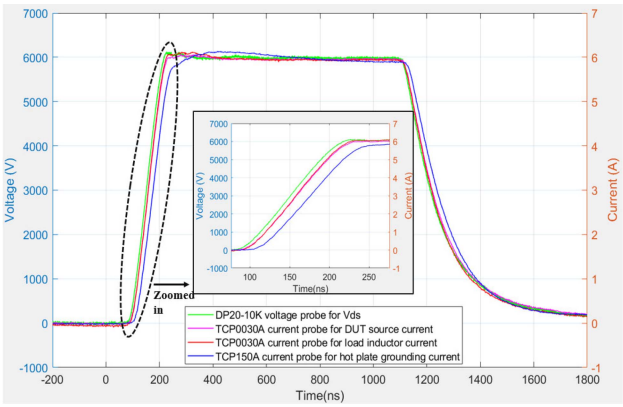


Fig. 16. Voltage and current waveforms of the probe delay test.

120 ns, so the equivalent frequency is 2.92 MHz. At this frequency, the phase delay caused by the inductance (600 nH) is only around 0.636°, and the corresponding time delay is 0.605 ns, compared to the current probe delay, this delay is small (<10%). Also, the sensitivity of the switching timing misalignment is shown in Fig. 15, based on the DPT test waveforms of the 10 kV/20 A SiC MOSFET. 1 ns of timing discrepancy results in 0.8% of switching loss error. Therefore, 0.605 ns only leads to 0.484% of switching loss error, so it is not considered.

The measured resistor voltage and current waveforms are shown in Fig. 16, and their shapes are similar, but they do not align with each other due to different delays. By shifting the current waveform to match the voltage waveform, the delay difference between the voltage probe and the current probe can be achieved. Compared to the voltage probe, the delay difference of the current probe used for the DUT source current, the load inductor current, and the hotplate grounding current is -7 ns, -7 ns, and -25 ns, respectively. The negative number means the measured current waveform needs to be shifted to the left by that time value to align with the voltage waveform.

C. DPT Test Results

The DPT test waveform at 6.8 kV dc-link voltage and 23 °C junction temperature is shown in Fig. 17. During the switching

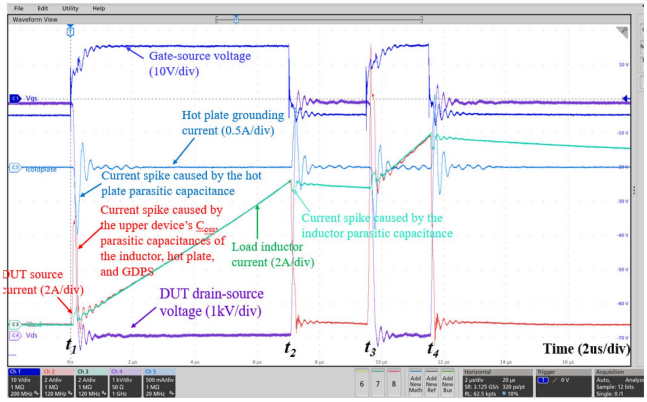


Fig. 17. DPT waveform at 6.8 kV dc-link voltage and 23 °C junction temperature.

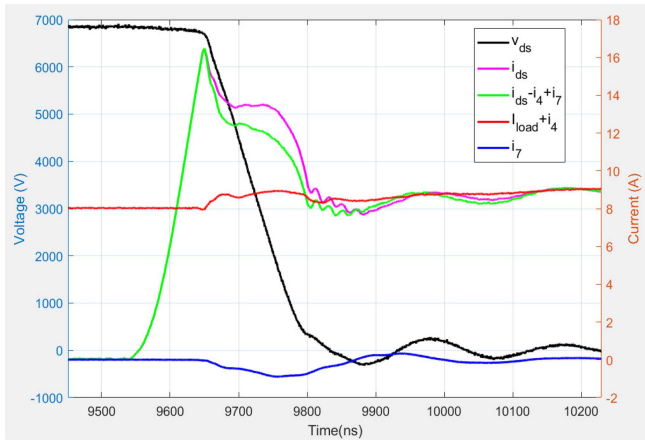


Fig. 18. "Real" ids deducting the currents from the load inductor and hotplate parasitic capacitances.

transients, the DUT source current, the load inductor current, and the hotplate grounding current all have current spikes. The hotplate grounding current spike is negative during the turn-ON transient and positive during the turn-OFF transient, corresponding to the discharging and charging of the hotplate parasitic capacitance. Similarly, the load inductor current spike also has a different polarity at the turn-ON and turn-OFF transients because of the charging and discharging of its parasitic capacitance. During the turn-ON transient, the DUT source current spike is mainly caused by the charging/discharging current of C_{oss1}, C_{p1}, C_{p3}, C_{p4}, and C_{p6}. Therefore, the waveform verifies the existence of parasitic capacitances and their charging and discharging currents.

To show the impact of the parasitic capacitance currents on the DUT current, the load inductor parasitic capacitance current, i_4, and the hotplate parasitic capacitance, i_7 are deducted from the measured DUT current considering the probe de-skew. As shown in Fig. 18, the parasitic capacitances leads to a larger measured i_{ds}, and the real i_{ds} becomes smaller after deducting i_4 and i_7, which matches with the discussion in Section III.

A comparison of the measured hotplate parasitic capacitance (grounding) current between the thin (3 mm) and thick

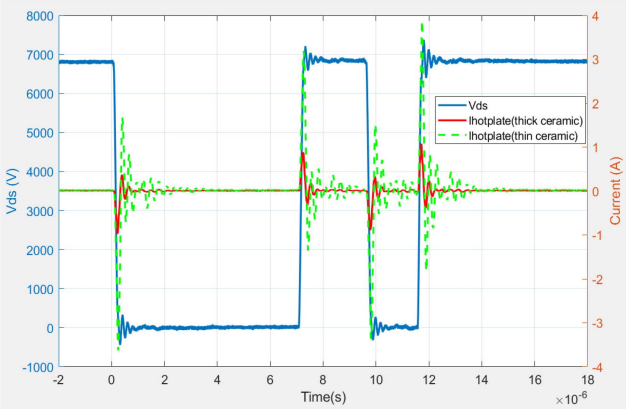


Fig. 19. Comparison of hotplate parasitic capacitance current between the thick and thin ceramic sheet setup.

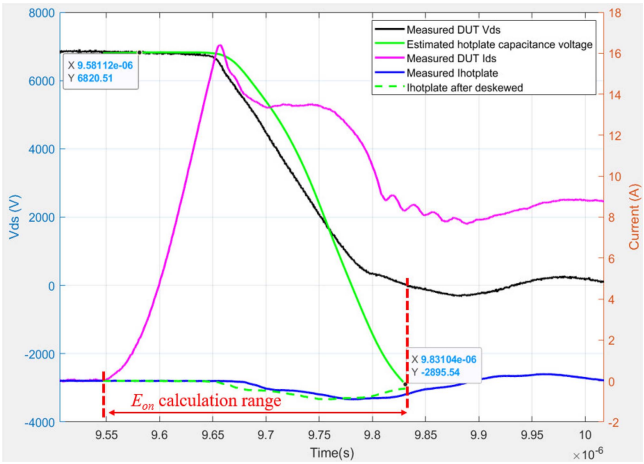


Fig. 20. Estimated voltage on the hotplate parasitic capacitance during the turn-ON transient.

(50.8 mm) ceramic sheets under the same DPT test condition (6.8 kV dc-link voltage and 23 °C junction temperature) is shown in Fig. 19. The current peak with a thin ceramic sheet is around 3.7 A, while the current peak with a thick ceramic sheet is only around 0.94 A. The ratio between the grounding current peak values is close to their corresponding parasitic capacitance ratio, i.e., 40 pF/11 pF. In addition, the resonance and damping of the current waveforms validated the existence of the loop inductance and resistance, and the larger parasitic capacitance results in a longer resonant period.

The voltage on the hotplate parasitic capacitance during the turn-ON transient is estimated using the measured hotplate grounding current. As shown in Fig. 20, because of the resonance in the loop, the parasitic capacitance's voltage changes from 6. kV to −2.9 kV, rather than 0, during the turn-ON transient. Therefore, (10) cannot be used to estimate the energy difference introduced by this parasitic capacitance.

The turn-ON energy E_{ON} and the turn-OFF energy E_{OFF} are calculated based on the DPT test waveforms. First, the switching energy is compared between the thick and thin ceramic

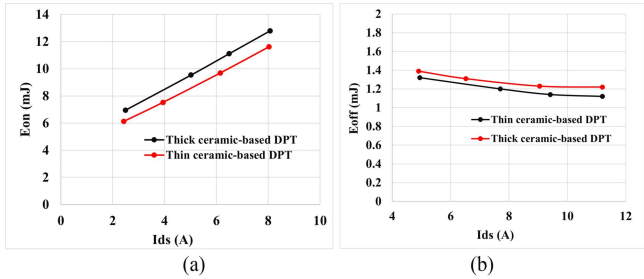


Fig. 21. (a) Turn-ON energy and (b) turn-OFF energy of the 10 kV SiC MOSFET at 6.8 kV dc-link voltage and 23 °C junction temperature.

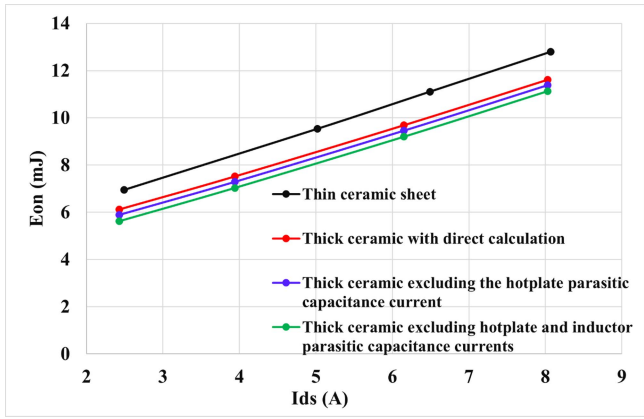


Fig. 22. Turn-ON energy loss comparison among different conditions.

sheet-based DPT, respectively. The load inductor and hotplate parasitic capacitance currents have not been subtracted from the DUT source current. As shown in Fig. 21(a), compared to the calculated E_{ON} values in thin ceramic sheet-based tests, the E_{ON} values in the thick ceramic-based tests are ∼1.2 mJ smaller. This is because the hotplate parasitic capacitance current enlarges the measured DUT current in the turn-ON transient, as analyzed in Section III. As shown in Fig. 21(b), the difference on E_{OFF} is small (∼ 0.1 mJ). This is because ZVS is realized in the device channel, which can be observed from the waveforms shown in Fig. 17, and the device performs as a nonlinear capacitance during the turn-OFF process.

Then, E_{ON} values are further calculated after the measured hotplate and inductor parasitic capacitance currents are subtracted from the measured DUT source current one by one. As shown in Fig. 22, after deducting the hotplate parasitic capacitance current, E_{ON} reduces 0.23 mJ, which is smaller than the energy stored in the hotplate parasitic capacitance (11 pF, 0.25 mJ) since the energy in the capacitance is not fully discharged and some energy is dissipated on other loop resistance. After deducting the inductor parasitic capacitance current, E_{ON} reduces 0.26 mJ, which is larger than the energy corresponding to the calculated inductor EPC (1.35 pF, 0.03 mJ). This is because the transient parasitic capacitance is larger than the EPC, as discussed in Section III. In the E_{OFF} calculation, however, parasitic capacitance currents should not be deducted since the ZVS is realized for the DUT channel during the turn-OFF process.

VII. Discussion

A. Assumption Discussion

The parasitic capacitance current deduction approach deducts parasitic capacitance currents from the measured DUT source current but still uses the measured v_{ds} for the $E_{\rm ON}$ and $E_{\rm OFF}$ calculation. This assumes that parasitic capacitance results in neglectable *dv/dt* change for v_{ds}. This can be achieved when the parasitic capacitance is much smaller than the device C_{oss} since the turn-ON and turn-OFF *dv/dt* is mainly determined by the C_{oss} charging of the upper and lower device, respectively. The C_{oss} of 10 kV/20 A SiC discrete device is 10 nF @1 V and 90 pF @3 kV [11], and the C_{oss} of the 10 kV/100 A power module is 40 nF@1 V and 900 pF @ 1 kV [10]. Although C_{oss} values at higher v_{ds} are not given in papers due to measurement capability, they decrease slowly as v_{ds} further increase. Therefore, after minimizing the parasitic capacitance in the DPT, the parasitic capacitance is much smaller than the device C_{oss}.

B. What is Next?

After minimizing the impact of parasitic capacitance on the device DPT, the intrinsitc device loss is obtained. With the information, the converter design can be conducted. However, in the MV converter, parasitic capacitances also exist, and they could be introduced by the PCB, heat sink, magnetics, and cables. The parasitic capacitance that is connected to the switching node of the converter will have the switching voltage and, thus, high-frequency charging and discharging current, resulting in losses. Therefore, in addition to the device loss, these parasitic capacitance-related losses need to be estimated as part of switching loss and considered in the converter efficiency estimation.

VII Conclusion

The DPT is improved from four aspects for accurate dynamic characterization of MV SiC devices. First, the grounding loop is avoided by adopting isolated probes. Second, parasitic capacitances in the DPT setup are minimized to reduce the impact on the DPT results. Third, to further improve the switching energy loss accuracy, currents contributed from parasitic capacitances are deducted from the measured DUT current. Fourth, the resistor-based method is adopted to obtain the delay difference between the voltage and current probes, and thus, the V-I switching timing alignment can be conducted. Based on the experiment results of the 10 kV/20 A SiC MOSFET DPT test, with the improved DPT the $E_{\rm ON}$ is reduced by 1.69 mJ, which is 24% and 13% of original $E_{\rm ON}$ at $I_{ds} = 2.4$ A and 8.1 A, respectively. The $E_{\rm OFF}$ is not impacted by parasitic capacitances since the ZVS is realized in the device channel.

Acknowledgment

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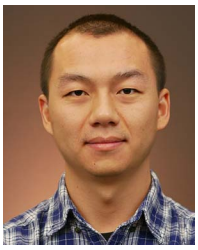

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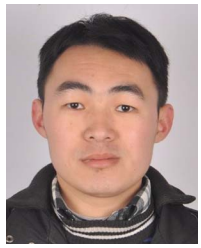

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