# Oscillation Issue and Solution for Solid-State Circuit Breaker Using High Power IGBT Module

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***Abstract*—Power semiconductors need to momentarily operate in the active area of DC solid-state circuit breakers (DC-SSCB) to limit the fault current. During this interval, a severe voltage oscillation is observed, leading to the DC-SSCB overstress and eventually failure. This article aims to understand the mechanism causing the voltage oscillation and devise solutions to suppress it. First, a MATLAB/Simulink model is built with comprehensive considerations of power semiconductors, parasitics, gate drive, and metal oxide varistor (MOV). Then a sensitivity study is performed to identify the critical impact factor(s) causing the voltage oscillation. Afterward, three suppression methods using enhanced gate drive circuitry are proposed and compared. Finally, test results based on a 2 kV/1 kA SSCB prototype demonstrate the accuracy of the derived model and the effectiveness of the proposed oscillation mitigation methods.**

***Index Terms*—IGBT, oscillation, solid-state circuit breaker.**

## I. Introduction

FOR commercial transport airplanes, the electric aircraft propulsion (EAP) system is essential for improving fuel economy, pollutants, and noise levels [1], [2], [3]. The medium voltage direct current (MVDC) system emerges as a promising power configuration for the EAP system to lower the overall weight of the EAP system [4], [5], [6]. Meanwhile, the DC EAP system needs a quick and trustworthy DC protection system. As the key component of the DC protection system [6], [7], [8], [9], the DC solid-state circuit breaker (DC-SSCB) enables the EAP system with safe and reliable operation.

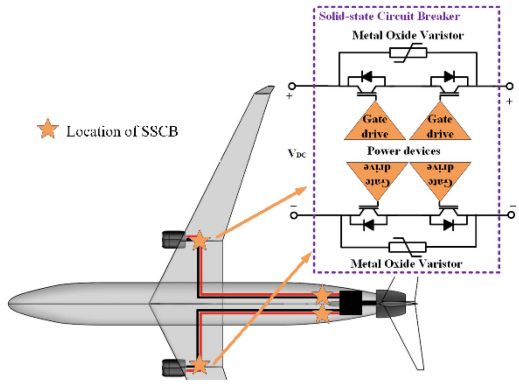


Fig. 1. Topology of a two-pole bidirectional DC-SSCB eliminating current limiting inductor in the NASA STARC-ABL [10].

A bulky and heavy current limiting inductor is typically leveraged in the DC-SSCB to limit the peak value of the system failure current [11]. As illustrated in Fig. 1, to decrease the overall weight of the DC EAP system's protection system, a current limiting inductor-free DC-SSCB is studied in [12], [13]. For the high-power MVDC applications' SSCB, multiple dies in parallel-based power modules are important and will be the target device in this article [14]. In this study, the IGBT is used as an example of a high-power semiconductor switch due to its availability, affordability, and reliability [15]. For such an SSCB without a current limiting inductor, to limit the peak fault current, the power semiconductor switch's *i-v* output characteristics are leveraged. Taking the IGBT as a case, as illustrated in Fig. 2, it can function in the saturation region, active region, and cut-off region. Once the IGBT operates in the active region, through the IGBT *i-v* characteristics, the collector current $i_C$ can be limited as saturation current $I_{sat}$. Accordingly, when a short circuit happens, the power semiconductor device is compelled to function in the active region to realize the system fault current limitation.

Desaturation detection triggers SSCB's protection [16]. However, if the desaturation protection response time is slower than

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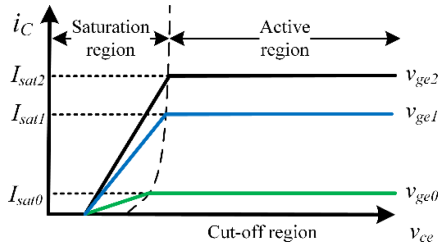



Fig. 2. V-I curve of the IGBT.

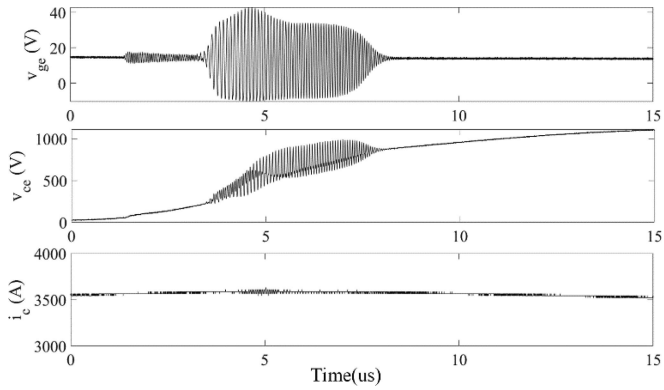



Fig. 3. Experimental oscillation waveform of gate-emitter and collector-emitter voltage.

the fault current approaches the protection triggering threshold (e.g., short-circuit fault close to the SSCB terminal with low fault system inductance), the fault current can still be clamped by the *i-v* characteristics where the $v_{GE}$ stays at the normal on-state voltage. This results in the most challenging situation for IGBTs and is a special operating circumstance for an SSCB without a current limiting inductor that is typically not desired or encountered in a typical pulse width modulation (PWM)-based converter and SSCB with current limiting inductor operations.

As illustrated in Fig. 3, severe oscillation of $v_{GE}$ and $v_{CE}$ is observed in the test when the IGBT enters the active region, which can destroy the device. Meanwhile, IGBT's $i_C$ clamped by its *i-v* characteristics. It should be noticed that during oscillation, the IGBT is not turned off, which is the worst-case scenario in which the gate drive is too slow to turn the IGBT off when the problem occurs. Thus, it is crucial to analyze the mechanism causing the oscillation and suppress it.

The oscillation can typically occur during a switching transition and a short-circuit scenario. Numerous studies have been conducted to analyze the power semiconductor's voltage oscillation, especially for emerging wide bandgap-based devices during the fast-switching transition. The classifications, causes, detrimental consequences, influence of the parasitic parameters, and suppression methods for the wide bandgap switching oscillations are reviewed in [17].

For the SSCB, the oscillation is most likely associated with the "short-circuit" condition where large current and high voltage exist simultaneously. Thus, the review [16] focuses on the oscillation under the short-circuit condition. IGBT oscillation under short-circuit has been studied since 2000. Without differential oscillation, [18] leverages single IGBT die for analysis and concludes that the Miller feedback capacitance is the reason of the oscillation. But neither the IGBT enters the active region nor does the gate-emitter voltage appears oscillation. To analyze the oscillation when the IGBT enters the active region, a small-signal model for the IGBT model with two chips is established in [19]. However, the impact of various parameters between different chips on the oscillation is not evaluated, and the suggested suppression strategy is not satisfactory. The oscillation when the IGBT enters the active region is also observed in [20]. To stop the gate oscillation, a low-pass filter-based gate loop is suggested. To clamp the gate oscillation, a low-pass filter-based gate loop is suggested. However, [20] does not fully explain the reason of the oscillation. The junction temperature and the stray inductance are identified as critical impact factors of oscillation during the IGBT module's short-circuit in [21]. However, [21] only has limited method to suppress oscillation. In [22], [23], [3] analyze and mitigate the IGBT chip oscillation under the short-circuit condition from the level of IGBT inner construction by inserting an n-doped layer at the surface of the IGBT. In summary, the suggested suppression techniques in [20], [21], [22], [23] do not consider the impact of the IGBT module's multi-chip configuration, and they are also quite challenging to execute. Moreover, [24], [25] also proposed methods to suppress the SSCB's oscillation under the short-circuit condition. Nevertheless, their oscillation happens during the turn-off transient, which is insufficient to explain the observed Fig. 3's oscillation.

Table I summarizes the state-of-the-art studies on the power semiconductor oscillation under different scenarios. It can be found that the oscillation phenomenon has been widely investigated. According to the semiconductor operation scenarios, it can be divided into PWM operation in power converters and SSCB operation. Specifically, oscillation can occur during the turn-on/off process or on-state of the power semiconductor. For the SSCB application, there are some works focusing on semiconductor oscillation. A few papers explored the oscillation in SSCB during the switching transition when the gate voltage changes to turn-off voltage to cut off the fault.

However, there is no study of the oscillation in SSCB during short circuit with no change in gate voltage. Thus, this article fills the gap in the study of SSCB oscillation under the short circuit condition. In summary, the contributions of this article include

1) First time analyze of the SSCB oscillation with MOV model during short circuit with gate constantly on. A MATLAB/Simulink model is built to explore the oscillation for power semiconductor entering the active region.
2) First time analyze the SSCB oscillation with a multi-dies semiconductor model with the consideration of multiple parameters/parasitics mismatch. With the help of the tool "Sensitivity analyzer" in MATLB, the influence of the mismatch of the IGBT dies to the oscillation is analyzed.
3) Holistically exploring potential solutions for oscillation suppression by stabilizing the gate-emitter voltage with experimental verification.

The remainder of this article is organized as follows. A model of an SSCB, including IGBT module with multiple chips is

TABLE I
SUMMARIZATION OF THE SEMICONDUCTOR OSCILLATION UNDER DIFFERENT SCENARIOS

| Semiconductor Device Operation Scenario | | Single Die | Power Module with Multiple Chips |
|---|---|---|---|
| Normal PWM operation | Switching transient (gate voltage changes) | [7] | [7] |
| | Short-circuit (gate voltage does not change) | [8][12][13] | [9][10][11] |
| SSCB operation | Switching transient (gate voltage changes) | [15] | [14] |
| | Short-circuit (gate voltage does not change) | No | No (work of this paper) |

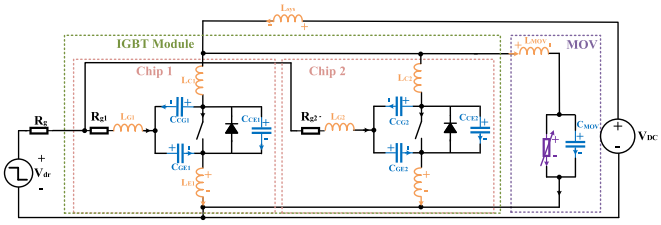



Fig. 4. SSCB model considering two IGBT dies, gate drive, MOV, and associated parasitics.

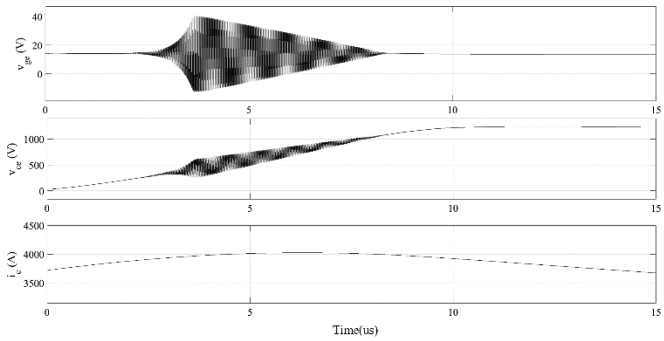



Fig. 5. Simulation waveform of the $v_{GE}$ and $v_{CE}$ oscillation when the two chips parameters have different value.

established in Section II along with simulation results for oscillation analysis. Moreover, in Section II, the sensitivity analysis is applied to the developed model to assess the influence of different parasitic parameters on the oscillation. In Section III, three methods are proposed to suppress the oscillation based on the models and analysis in Section II. Then, the experiment is conducted with a 2 kV/1 kA SSCB engineering prototype to validate the analysis and proposed solutions in Section IV. Finally, Section V concludes this article.

## II. OSCILLATION ANALYSIS

In Fig. 4, a thorough model considering the features of power semiconductor devices, gate drive, MOV, and related parasitics is constructed to analyze the process when the SSCB reaches the active region. Specifically, for the high-power EAP system, a power module with multiple dies is required for SSCB. Accordingly, as illustrated in Fig. 4, the first stage focuses on a power module made up of two chips. For modules containing more than two chips, a similar methodology could be used. Analysis results for three chips and four chips are also presented in this Section.

Specifically, the model in Fig. 4 considers two IGBT channels (including threshold voltage and transconductance) together with corresponding collector-gate capacitances $C_{CG1}$, $C_{CG2}$, collector-emitter capacitances $C_{CE1}$, $C_{CE2}$, gate-emitter capacitances $C_{GE1}$, $C_{GE2}$, collector inductances $L_{C1}$, $L_{C2}$, gate inductances $L_{G1}$, $L_{G2}$, and emitter inductances (i.e., common source inductances) $L_{E1}$, $L_{E2}$. Also, driving voltage $V_{DR}$, outer gate resistance $R_G$, and inner gate resistance $R_{G1}$ and $R_{G2}$ are included in the following analysis. The model also includes MOV *V-I* characteristics, its associated capacitance $C_{MOV}$, and parasitic inductance $L_{MOV}$ contributed by the interconnection (e.g., bus bar) between the IGBT module and the MOV. Additionally, $L_{sys}$ and $V_{DC}$ are the system inductance and DC bus voltage of the system under protection, respectively.

For the SSCB model in Fig. 4, a MATLAB/Simulink model with IGBT details is built up where two chips with mismatched collector-gate capacitances, collector-emitter capacitances, gate-emitter capacitances, collector inductances, emitter inductances, and *i-v* characteristics in the simulation are considered. Based on the datasheet, the *i-v* characteristic is represented with a 1-dimensional look-up table (LUT), and the parasitic values are selected. It is noted that considering that there are two chips in the module, the value utilized in model per chip is scaled based on the IGBT module parameter in the datasheet. Moreover, the nonlinear characteristic of the Miller capacitor of the IGBT and V-I curve of the MOV are also included in the simulation.

Following the same test shown in Figs. 3 and 5 shows the $v_{GE}$ and $v_{CE}$ waveforms when the module enters the active region in the simulation. It can be found that $v_{GE}$ and $v_{CE}$ start to oscillate when the module enters the active region, which agrees with the experimental waveforms in Fig. 3. It is noted that when the two chips share the same parameter values, the simulation results in Fig. 6 show that there is no oscillation on $v_{GE}$ and $v_{CE}$, which further proves that the chip characteristics difference aggravates the oscillation. By considering multi-chips in IGBT module, the oscillation frequency when the IGBT enters the active region has been analyzed in [19] through small-signal analysis. Besides, based on [14], the oscillation may even occur with the same parameters for chips but under different operating conditions. This article furthers the understanding with the consideration that the chips with parameter mismatch could further worsen the oscillation.

Identification of the parameters that are crucial to the oscillation is crucial for its suppression. Accordingly, to determine the most important effect factor(s) on the oscillation, a sensitivity

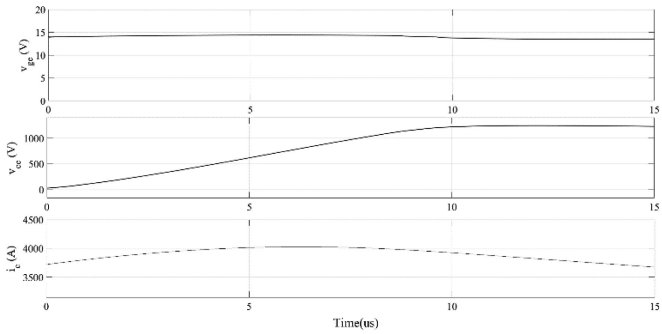



Fig. 6. Simulation waveform of the $v_{GE}$ and $v_{CE}$ oscillation when the two chips parameters have the same value.

TABLE II
PARAMETERS OF CHIP 1

| Parameters | Value | Unit |
|---|---|---|
| Collector-emitter capacitance $C_{CE1}$ | 0.75 | $nF$ |
| Gate-emitter capacitance $C_{GE1}$ | 68 | $nF$ |
| Collector inductance $L_{C1}$ | 50 | $nH$ |
| Emitter inductance $L_{E1}$ | 10 | $nH$ |
| Gate inductance $L_{G1}$ | 30 | $nH$ |
| Gate resistance $R_{G1}$ | 1 | $m\Omega$ |
| Gate threshold voltage $V_{TH1}$ | 7.9 | $V$ |
| Transconductance $gfs1$ | 304.8 | $S$ |

analysis is thus carried out using MATLAB/ Simulink with toolbox "*Sensitivity Analyzer*" through the built IGBT model with multi-chip.

The maximum variance value in (1) of $v_{CE}$ is identified as one of the essential dynamic performance characteristics to measure the severity of the oscillation in the sensitivity analysis.

$$\delta^2 = \frac{\sum (X_i - \mu)^2}{N} \tag{1}$$

where $N$ is the number of the samples; $\mu$ is the mean value of the samples; $X_i$ is the i$^{th}$ sample value.

Considering that the multi internal device can have different parasitic parameters, the parameters of one device and corresponding parasitics in Fig. 4 are selected as sensitivity analysis variables, which include collector inductance $L_{C1}$, $L_{C2}$, gate inductance $L_{G1}$, $L_{G2}$, emitter inductance $L_{E1}$, $L_{E2}$, collector-emitter capacitance $C_{CE1}$, $C_{CE2}$, and gate-emitter capacitance $C_{GE1}$, $C_{GE2}$. Then, the device gate threshold $V_{TH}$ and transconductance $g_{fs}$ are also selected as input variables. Moreover, the parasitic capacitance and inductance of the MOV are analyzed. To analyze which IGBT chip's characteristics mismatch matter on the oscillation, the parameter/parasitic values associated with IGBT chip 1 are fixed in the simulation, shown in Table II. Then, IGBT chip 2's parameter/parasitic values are changed in the sensitivity analysis to get different variance values of the collector-emitter voltage during the oscillation, which is utilized to find out which parameter's difference matters most for the oscillation. Thus, 500 samples are randomly selected based on the Monte Carlo method with the parameter sweep ranges listed in Table III. Additionally, the MOV parasitic capacitance $C_{MOV}$ and the parasitic inductance between IGBT and MOV $L_{MOV}$ are also listed in Table III for sensitivity analysis to study the influence of the MOV on the oscillation when IGBT enters the active region.

TABLE III
INPUT VARIABLES RANGE FOR SENSITIVITY ANALYSIS

| Parameters | Min. | Max. | Unit |
|---|---|---|---|
| Collector-emitter capacitance $C_{CE2}$ | 0.67 | 0.83 | $nF$ |
| Gate-emitter capacitance $C_{GE2}$ | 61 | 75 | $nF$ |
| Collector inductance $L_{C2}$ | 45 | 55 | $nH$ |
| Emitter inductance $L_{E2}$ | 9 | 11 | $nH$ |
| Gate inductance $L_{G2}$ | 27 | 33 | $nH$ |
| Gate resistance $R_{G2}$ | 0.9 | 1.1 | $m\Omega$ |
| Gate threshold voltage $V_{TH2}$ | 7.2 | 8.8 | $V$ |
| Transconductance $gfs2$ | 274.5 | 335.5 | $S$ |
| MOV parasitic capacitance $C_{MOV}$ | 2.7 | 3.3 | $nF$ |
| Parasitic inductance between IGBT and MOV $L_{MOV}$ | 0.09 | 0.11 | $\mu H$ |

Based on the 500 randomly generated samples, Fig. 7 shows the scatter plot of the sensitivity analysis. The scatter subplots display the variance value of $v_{CE}$ as a function of each parameter in the parameter set. The number of points in each scatter plot equals the number of rows in the parameter set. The last column of subplots displays histograms of the probability distribution of the evaluated cost function values. It can be found in Fig. 7 that the variance value of $v_{CE}$ is highly monotonically related to the parameter $L_e$, indicating that the mismatch of $L_e$ between chip 1 and chip 2 has a significant influence on the oscillation.

Then the quantitative analysis is performed to investigate the influence of $L_{e2}, L_{c2}, R_{g2}, V_{TH2}, C_{ge2}, C_{ce2}, L_{g2}, C_{MOV}, L_{MOV}$, and $g_{fs2}$ on the variance of $v_{CE}$ during the oscillation with different number of chips. Results are illustrated in Fig. 8 with tornado plots. Seven indexes (i.e., correlation, rank correlation, Kendall correlation, standardized regression, rank standardized regression, partial correlation, and rank partial correlation) are used to quantify the influence of the input variables on the maximum variance of $v_{CE}$ during the oscillation. Correlation is utilized to analyze how the input variables and the variance value of $v_{CE}$ are related; Standardized regression is used to analyze how the input variables linearly influence the maximum variance value of $v_{CE}$. Partial correlation indicates how the input variables and the maximum variance value of $v_{CE}$ are related without the influence of the other variables. In the tornado plot, the variables are sorted based on the correlation coefficient, which means that the $L_{e2}$ has the most influence on the variance value of $v_{CE}$.

The values of the seven indexes are located between $-1$ and $+1$. The magnitude indicates how much the maximum variance value of the $v_{CE}$ is influenced by the corresponding parameter, and the sign illustrates the increase of the corresponding parameter value relates to an increase or decrease of the maximum variance value of the $v_{CE}$. Specifically, $L_{E2}$, $R_{G2}$, $C_{GE2}$, $L_{G2}$ and $L_{MOV}$ have positive correlation coefficient, indicating that their increase will increase the maximum variance value of $v_{CE}$. Meanwhile, $L_{C2}$, $V_{TH2}$, and $C_{MOV}$ have negative correlation coefficient, indicating that their decrease will increase the maximum variance value of $v_{CE}$. Considering that parameter values of chip 1 is fixed in the sensitivity, analysis, the results in Figs. 7 and 8 further prove that the mismatch between chip 1 and chip 2 can aggravate the oscillation.

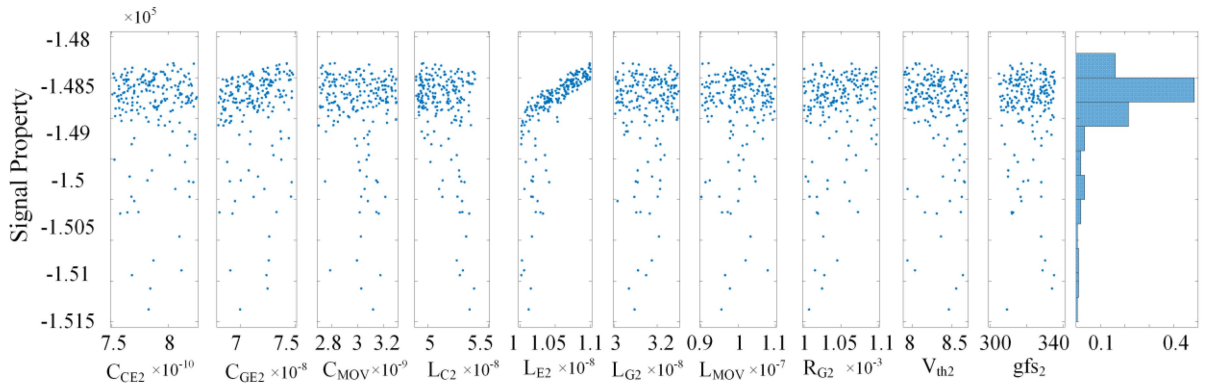



Fig. 7. Scatter plot of the sensitivity analysis for SSCB.

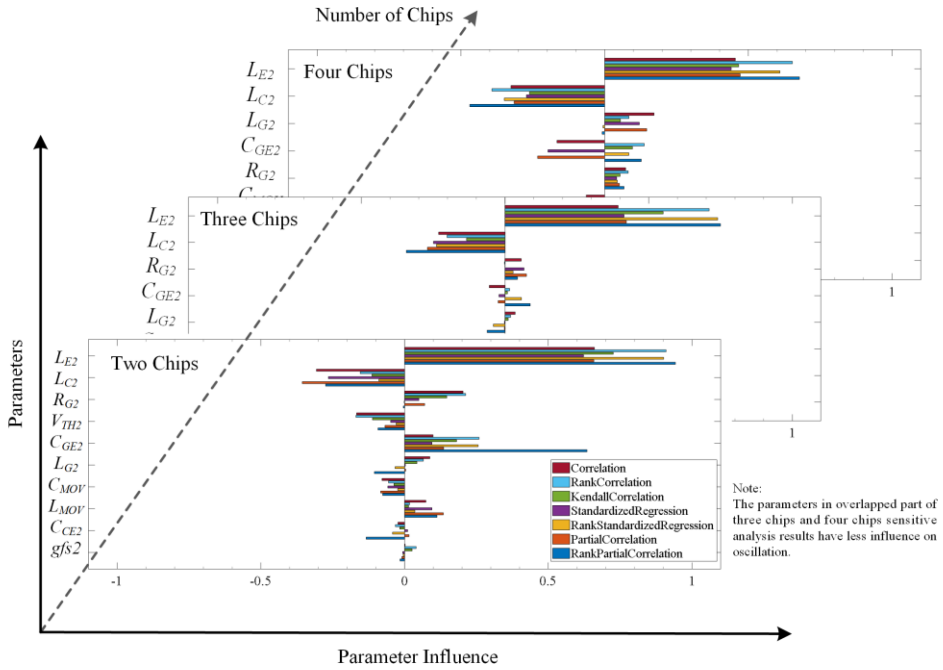



Fig. 8. Parameter influence on the variance value of the collector-emitter voltage.

TABLE IV
THE CORRELATION OF DIFFERENT PARAMETERS

| | $L_E$ | $L_C$ | $R_G$ | $V_{TH}$ | $C_{GE}$ | $L_G$ | $C_{MOV}$ | $L_{MOV}$ | $C_{CE}$ | $gfs$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Transconductance | ** | * | * | * | * | * | * | * | -- | -- |

**: Correlation greatly *: Correlation slightly --: Weak correlation

Thus, based on the result of the tornado plot in Fig. 8, the difference in the $L_E$, $L_C$, $R_G$, $V_{TH}$, $C_{GE}$, $L_G$, $C_{MOV}$, and $L_{MOV}$ can aggravate the oscillation. Meanwhile, the difference in the $C_{CE}$ and $g_{fs}$ do not have so much influence on the oscillation. Table IV summarizes the correlation of different parameters.

## III. OSCILLATION SUPPRESSION METHODS

According to the analysis in Section II, the mismatch between distinct IGBT chips must be eliminated to suppress the oscillation. However, it is difficult for the manufacturer to produce identical chips for every chip. Moreover, it is also challenging for the user to modify the module package's inner parasitic parameters. A gate drive-based oscillation suppression technique is therefore selected. Fig. 9 illustrates the gate drive circuit of the SSCB. As the main function circuit to detect the short circuit fault, detection circuit is leveraged to detect $v_{CE}$. The detected value is compared with the threshold voltage through the comparator to trigger the protection with a fault signal. To reduce *di/dt* during the turn-off process, $R_{soft}$ is

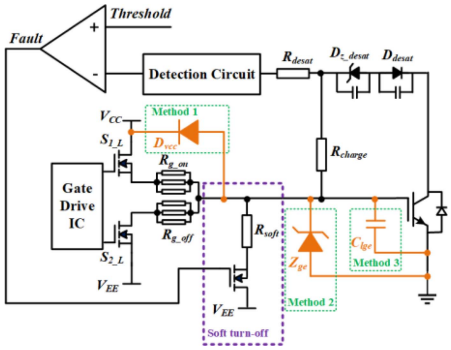
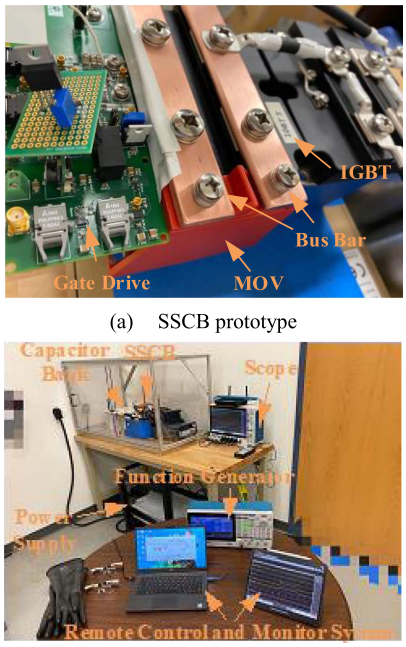



Fig. 9. SSCB gate drive circuit with the proposed oscillation suppression methods.




(a) SSCB prototype

(b) SSCB testbed

Fig. 10. SSCB prototype and testbed for evaluation of the oscillation suppression methods.

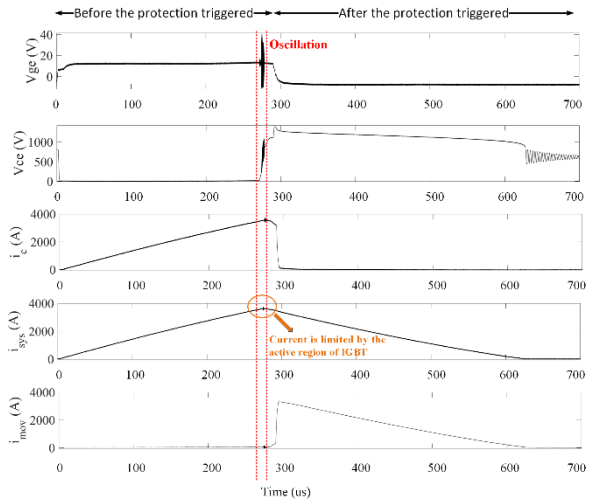
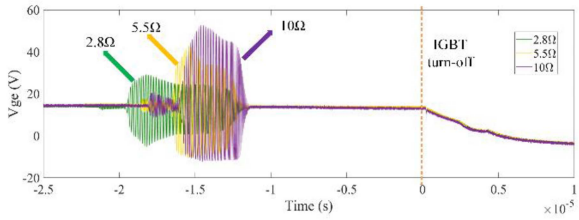
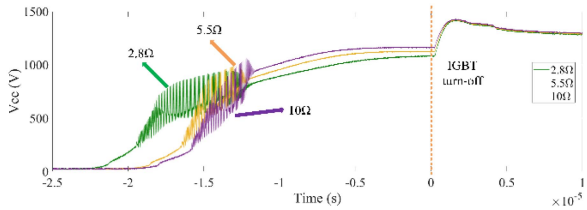



Fig. 11. Waveform of the SSCB without the oscillation suppression methods.




(a) $v_{GE}$ when the IGBT enters active region with different gate loop resistance.




(b) $v_{CE}$ when the IGBT enters active region with different gate loop resistance.

Fig. 12. Waveforms when the IGBT enters the active region with different gate loop resistances.

leveraged to reduce the turn-off speed of the IGBT when the fault occurs. Moreover, $R_{g\_on}$ and $R_{g\_off}$ are the external gate resistors to control the turn-on and turn-off speed of the IGBT. The gate turn-on voltage $V_{CC}$, turn-off voltage $V_{EE}$, and the MOSFETs $S_{1\_L}$ and $S_{2\_L}$ comprise the gate drive buffer circuit to turn on/off the IGBT.

The test waveforms in Fig. 3, and the simulation waveforms in Fig. 5 show that $v_{GE}$ constantly oscillates with $v_{CE}$. When the IGBT enters the active region, according to the *i-v* output characteristics, $v_{CE}$ is highly related to $v_{GE}$. Accordingly, we can stabilize $v_{GE}$ to suppress the oscillation on $v_{CE}$ when the IGBT enters the active region.

The most direct way is to increase the gate loop resistance by increasing the external gate resistance, which can suppress the gate oscillation. It can be realized by increasing the value of $R_{g\_on}$.

Besides the approach to increase the gate loop resistance, three other oscillation suppression methods are proposed in this section, as illustrated in Fig. 9. The fundamental idea behind the three suggested strategies is to stabilize $v_{GE}$, and then suppress the $v_{CE}$ oscillation. The proposed methods include:

*Method 1*: a diode $D_{VCC}$ is anti-paralleled with the gate resistor to directly connect $V_{CC}$ and the IGBT gate terminal to limit $v_{GE}$ to $V_{CC}$. When the gate terminal voltage exceeds $V_{CC}$, it will be clamped to remain at $V_{CC}$.

*Method 2*: a Zener diode $Z_{ge}$ is paralleled with the IGBT gate and emitter terminals. The Zener diode clamps the potential difference between the ground (emitter) and collector. Thus, the $v_{GE}$ value cannot be higher than the breakdown voltage of the Zener diode. It is noted that the Zener voltage should be a little higher than $V_{CC}$ to prevent the influence of Zener diode on $V_{CC}$ during the normal operation of the SSCB.

*Method 3*: a decoupling capacitance $C_{lge}$ is paralleled with the collector and emitter terminals of the IGBT to absorb noise current (e.g., displacement current during *dv/dt*), and then stabilize $v_{GE}$.

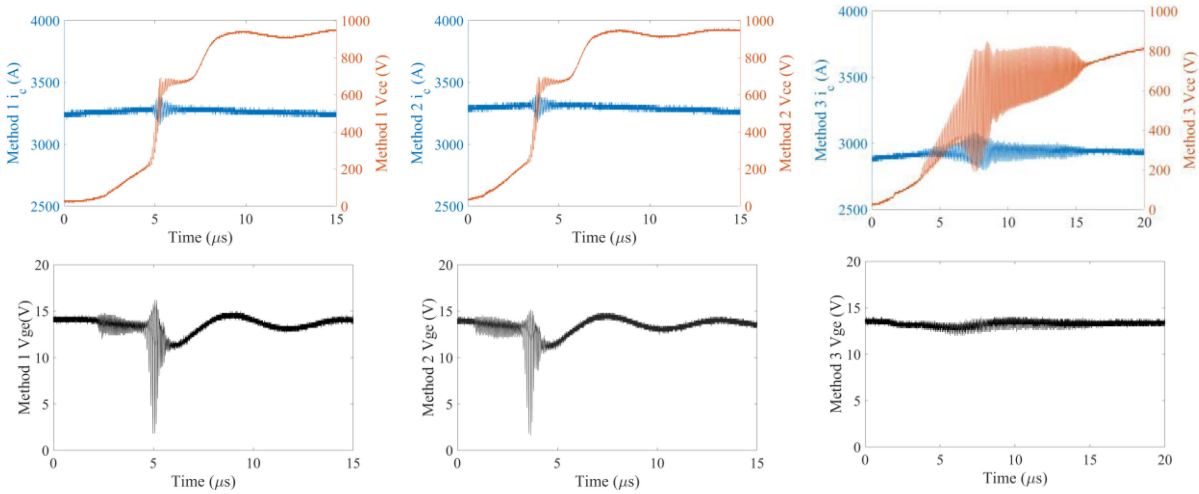



Fig. 13. Waveforms of $v_{ce}$ and $v_{ge}$ when the IGBT enters active region with the proposed oscillation suppression methods.

TABLE V
PARAMETERS OF THE SSCB PROTOTYPE

| Parameters | Value |
|---|---|
| IGBT | FZ1000R33HE3 |
| MOV | V511BA60 |
| $L_{MOV}$ | 250 nH |
| $L_{sys}$ | 55 uH |
| $V_{CC}$ | 13.5 V |
| $V_{EE}$ | -7.5 V |
| $R_{g\_on}$ | Design variable |
| $R_{g\_off}$ | Design variable |
| *Gate Drive IC* | ACPL-339J |

## IV. EXPERIMENTAL VERIFICATION

To validate the analysis and suggested solutions for oscillation suppression in the SSCB application, experiments are carried out. According to the specifications for NASA's STARC-ABL concept [10], Fig. 10 shows a 800V/1 kA SSCB prototype. The effectiveness of the proposed oscillation suppression methods is verified through a practically relevant condition. The key parameters are summarized in Table V.

CWTMini HF30B Rogowski coil with a 6 kA peak-current rating is used to measure the system current. The differential probe TMDP0200 is used to measure the voltage.

### A. Waveform of the SSCB Without Oscillation Suppression

Fig. 11 illustrates the waveforms of $v_{GE}$, $v_{CE}$ the IGBT module current *ic*, the system current $i_{sys}$, and the current flowing through the MOV $i_{MOV}$ during the whole process of a short circuit fault. It can be observed that when the IGBT enters the active region, there is obvious oscillation on $v_{CE}$ and $v_{GE}$. The system current $i_{sys}$ is limited by the IGBT when the IGBT enters the active region.

### B. Verification of the Increasing Gate Loop Resistance Method

To validate the effectiveness of the mitigation approach of increasing the gate loop resistance, additional outer gate resistors with 2.8 Ω, 5.5 Ω, and 10 Ω are introduced into the gate loop, respectively. Fig. 12 illustrate the waveforms of $v_{GE}$ and $v_{CE}$ with different gate loop resistances to suppress the oscillation when the IGBT enters the active region. The SSCB is turned off at 0 s. Before 0 s, the IGBT enters the active region with a specific gate loop resistor. It can be found that there still is obvious oscillation when the gate loop resistance increases to 10 Ω. With the gate loop resistance increase, the $v_{CE}$ oscillation performance becomes a little better. However, the oscillation on $v_{GE}$ and $v_{CE}$ is still obvious, which may cause damage to the SSCB. The reason is that increasing lumped gate resistance is not good enough to dampen the oscillation on the gate terminal, and a larger external gate resistance makes the external gate driver has less control capability to the module. Moreover, increasing the gate loop resistance will affect the switching speed of the power semiconductor, which is important to the SSCB. Therefore, it is not recommended to suppress the oscillation by increasing the gate loop resistance for this kind of oscillation.

### C. Verification of the Proposed Methods

As mentioned in Section III, three other methods are also evaluated in this section. Fig. 13 illustrates the waveforms of $v_{GE}$, $v_{CE}$, and $i_C$ when the IGBT enters the active region with different oscillation suppression methods. According to the test results, it can be found that the diode-based method 1 and the Zener diode-based method 2 work well. The gate voltage is well clamped by both methods; and accordingly, the oscillation on $v_{CE}$ is also damped. Although there still is a little oscillation remaining, it will not influence the operation of the SSCB. It is noted that the oscillation cannot be removed completely with method 1 and method 2. Because the oscillation source is from the inner construction of the IGBT module, method 1 and method 2 cannot change the inner construction of the IGBT module. Table VI summarizes the effectiveness of the proposed suppression methods. It can be found that that the proposed methods can reduce the maximum $v_{CE}$ amplitude during oscillation by about 50%.

TABLE VI
MAXIUM VCE AMPLITUDE DURING OSCILLATION UNDER DIFFERENT CONDITIONS

| | Maximum $v_{CE}$ amplitude during oscillation (V) | Oscillation index |
|---|---|---|
| Without suppression | 403 | 100% |
| Method 1 | 196 | 48.6% |
| Method 2 | 201 | 49.9% |
| Method 3 | 616 | 152.9% |

However, from Fig. 13, the additional $C_{GE}$-based method 3 does not work well and even makes the oscillation on $v_{CE}$ more severe. Meanwhile, $v_{GE}$ is much more stable than method 1 and method 2. Initially, $C_{lge}$ is to increase the value of $C_{GE}$ to stabilize $v_{CE}$. However, the additional gate-emitter capacitance can form a first order oscillation with $L_G$, which aggravates the oscillation and aligns with the sensitivity analysis in Section III.

Therefore, the traditional method of increasing the gate loop resistance has limited effectiveness in oscillation suppression. Methods 1 and 2 in Fig. 9 are preferred for damping the oscillation. However, method 3 will aggregate the oscillation.

## V. CONCLUSION

This article analyses mechanisms causing oscillation of $v_{GE}$ and $v_{CE}$ when the lightweight DC-SSCB without a current limiting inductor enters the active region, and three suppression approaches are proposed by stabilizing the gate-emitter voltage. Analysis results show that the difference in $L_E$, $L_C$, $R_G$, $V_{TH}$, $C_{GE}$, $L_G$, $C_{MOV}$, and $L_{MOV}$ can aggravate the oscillation. The mismatch between $L_E$ has the most influence on the oscillation. Then, experimental results illustrate that clamping $v_{GE}$ by paralleling a Zener diode between the gate and emitter terminals or connecting positive driving voltage and gate terminal through a clamping diode can effectively suppress the oscillation on $v_{CE}$ by about 50%. However, increasing the lumped gate resistance or paralleling an additional gate-emitter capacitor are not effective.

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