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TOPICAL REVIEW

Power Converters Coolant: Past, Present, Future, and a Path Toward Active Thermal Control in Electrified Ship Power Systems

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ABSTRACT Power converters have widespread applications in automotive, renewables, and power systems. The demand for power modules with low power consumption and high efficiency has increased due to advancements in semiconductor devices. So, power converters need to be highly efficient to reduce costs associated with energy dissipation and cooling requirements. This paper discusses various active thermal control methods for high-power power converters. It covers modulation and configuration techniques, ranging from single configurations to cascaded, modular, and multilevel converters. These concepts form the basis of power electronics building blocks, particularly relevant in all-electric ship systems. Power electronics building blocks represent a thriving technology that will advance ship power systems, the thermal design of which plays a crucial role in managing high heat dissipation levels. Hence, thermal management is essential for reliable device performance. The paper thoroughly studies different active thermal control methods and their impact on power semiconductor devices and converters, categorized per configurations, power routing methods, modulation, and control layers. The review then moves to thermal control methods for the PEBBs concept using multilevel converters in all-electric ship systems. The paper eventually outlines future research directions for the thermal aspect of power electronics building blocks.

INDEX TERMS Power semiconductor device, active thermal control, multilevel converter, power electronics building block, modulation strategy, power routing, health monitoring, all-electric ship.

NOMENCLATURE

3L-NPC	Three-level Neutral-Point-Clamped.
2L-VSC	Two-level Voltage Source Converter.
AES	All-Electric Ship.
ALE	Active Lifetime Extension.
ALT-60° DPWM	Alternative 60° Discontinuous Pulse Width Modulation.
ANPC	Active Neutral-Point-Clamped Converter.
ATC	Active Thermal Control.
CAN	Controller Area Network.
CHB	Cascaded H-Bridge.
CHB-MLC	Cascaded H-Bridge Multi-level Converter.
CM	Condition Monitoring.
CONV-60° DPWM	Conventional 60° Discontinuous Pulse Width Modulation.
CTE	Coefficients of Thermal Expansion.
DAB	Dual Active Bridge.
DCCS	Distributed Communication and Control System.

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DFIG	Doubly-Fed Induction Generator.
DPWM	Discontinuous Pulse Width Modulation.
ELT	Estimated Lifetime.
EMI	Electromagnetic Interference.
ESD	Energy Storage Device.
ESS	Energy Storage System.
EtherCAT	Ethernet for Control Automation Technology.
EV	Electric Vehicle.
FC-MLC	Flying Capacitor Multi-level Converter.
FCS-MPC	Finite Control Set Model Predictive Control.
FDDI	Fiber Distributed Data Interface.
FEM	Finite Element Method.
FPGA	Field-Programmable Gate Array.
FRT	Fault Ride-Through.
GaN	Gallium Nitride.
GSC	Grid Side Converter.
HTSSM	High-Temperature Superconducting Synchronous Machine.
HVDC	High-Voltage Direct Current.
HVRT	High-Voltage Ride-Through.
IGBT	Insulated-Gate Bipolar Transistor.
IM	Induction Machine.
IMU	Impedance Measurement Unit.
iPEBB	Integrated Power Electronics Building Block.
LVDC	Low-Voltage Direct Current.
LVRT	Low-Voltage Ride-Through.
MACRO	Motion And Control Ring Optical.
MEA	More Electric Aircraft.
MLC	Multi-Level Converter.
MMC	Modular Multi-level Converter.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
MPPT	Maximum Power Point tracking.
MVAC	Medium-Voltage Alternating Current.
NLM	Nearest Level Modulation.
NPC	Neutral-Point-Clamped.
NPC-MLC	Neutral-Point-Clamped Multi-level Converter.
ONR	Office of Naval Research.
OPT-ZSSPWM	Optimal Zero Sequence Injection Pulse Width Modulation.
PEBB	Power Electronics Building Block.
PESNet	Power Electronics System Network.
PI	Proportional-Integral.
PMSM	Permanent Magnet Synchronous Motor.
PROFIBUS	Process Field Bus.
PROFINET	Process Field Net.
PROFINET IRT	Process Field Net Isochronous Real Time.
PSD	Power Semiconductor Device.
PV	Photovoltaic.
PWM	Pulse Width Modulation.
QAB	Quadruple Active Bridge.
RSC	Rotor Side Converter.
RUL	Remaining Useful Lifetime.
SE	Sync Error.
SERCOS	Serial Real-time Communications System.
SHDCM	Superconducting Homopolar Direct Current Machines.
Si	Silicon.
SiC	Silicon Carbide.
SoH	State-of-Health.
SPI	Serial Peripheral Interface.
SVD	Space Vector Diagram.
SVM	Space Vector Modulation.
SVPWM	Space Vector Pulse Width Modulation.
SyCCo-Bus	Synchronous-Converter-Control-Bus.
ST	Smart Transformer.
THD	Total Harmonic Distortion.
THIPWM	Third Harmonic Injected Pulse Width Modulation.
TSEP	Temperature-Sensitive Electrical Parameter.
VSC	Voltage Source Converter.
WBG	Wide Bandgap.
WRN	White Rabbit Network.
ZCS	Zero-Current Switching.
ZVS	Zero-Voltage Switching.

I. INTRODUCTION

A. BACKGROUND

Power converters find application in a diverse range of fields, including but not limited to renewable energy systems like photovoltaic systems [1], electric vehicles (EVs) and motor drives [2], [3], custom power devices [4], all-electric ship (AES) power system [5], and so on. Reliability and efficiency of converters have been demanding issues, as they play a crucial role in the design of power systems [6], [7], [8]. Power semiconductor devices (PSDs) are typically integrated into modules to increase power density and reduce material consumption [9]. The failure distribution among power electronic components is depicted in Figure 1a. The figure indicates that capacitors and semiconductors stand out as the most fragile components in terms of vulnerability among power electronic components. Figure 1b compares the underlying reasons for stresses and failures in power electronics converters. As can be seen, temperature is the most dominant cause of stress in power electronics converters, highlighting the importance of controlling the temperature of PSDs [10]. This also highlights the crucial role of PSDs in ensuring the reliability of power systems. PSD failure is the underlying cause of power electronics converter faults, indicating that enhancing the reliability of PSDs results in improved power converter reliability.

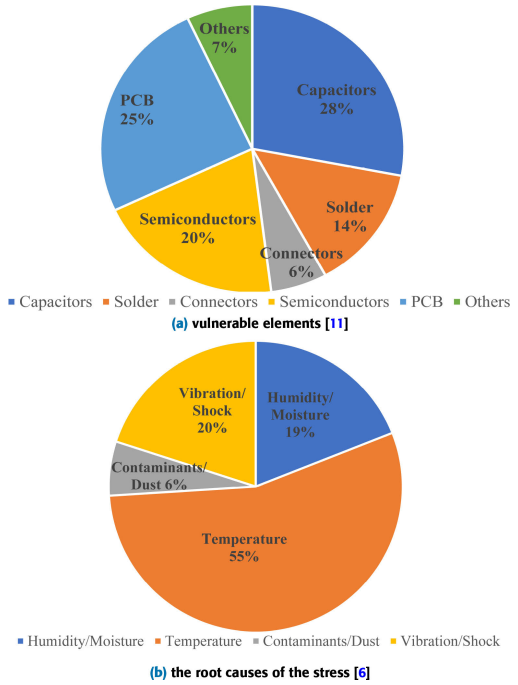


FIGURE 1. Power electronics converters.

B. MOTIVATION

As mentioned, one can declare that the power system reliability is strongly linked to the reliability of the PSDs. PSD failure is the fundamental reason for power converter faults, meaning that improving the reliability of the PSDs leads to an increase in the power converter reliability. To address this issue, several studies have been conducted over the years, including condition monitoring (CM), active thermal control (ATC), and remaining useful lifetime (RUL) estimation methods, as shown in Figure 2. The rationale behind the CM is to utilize physical measurements to detect the occurrence of failures or degradation in the entire power system. Based on the outputs of CM, appropriate actions can be taken to prevent a sudden shutdown of the system.

Another approach to enhance the reliability of the PSDs is the ATC. As shown in Figure 2, the degradation indicator data obtained from online CM methods can be utilized to passively update and, significantly, actively control the system's lifetime through the use of ATC. As mentioned above, thermal stress is the primary cause of PSD failures. ATC mitigates the thermal stress on the components by reducing the amplitude of temperature fluctuations or lowering the average temperature without modifying the converter. This means there probably be no additional expenses for improving the converter design or elements. It is worth pointing out that the thermal control capability and the power system's performance must be simultaneously considered. Finally, the RUL estimation method is, by and large, deployed to design the ATC and then validate its effect. Figure 2 shows the relationship between the method mentioned earlier; CM, ATC, and RUL estimation.

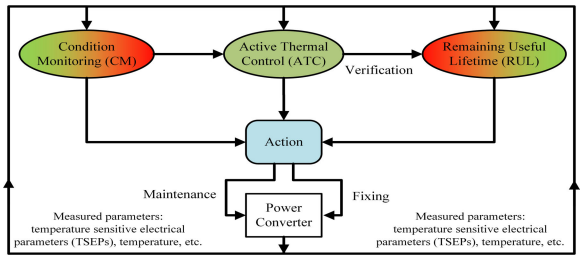


FIGURE 2. Relationship between the CM, the ATC, and the RUL estimation methods.

The material layers in the power converter modules serve to provide both functionality and electrical insulation [12]. In general, aluminum bond wires are used for the electric connection between chips and terminals [13]. Figure 3 depicts the layer sequence of an insulated gate bipolar transistor (IGBT) module tied to a heatsink. Due to ambient temperature and power consumption variations, the layers undergo continuous heating and cooling processes, referred to as thermal cycles [14]. Due to the mismatch in coefficients of thermal expansion (CTE) between the layers, mechanical stress occurs in the module [15], leading to aging and damage to the modules [16]. The magnitude of the thermal cycles contributes to the degree of aging [17]. Short-term cycles mainly cause the bonds' fatigue, leaving bond wire on the surface and rising. Long-term cycles, despite the high thermal capacitance of the base plate, affect its temperature and lead to solder fatigue [18]. Plus, the modules' failure means inevitable maintenance, replacement, and thus outages and the operators' expenses.

Various studies have been conducted to improve the lifetime and reliability of modules, including developing improved connection technologies and assembly methods. In [9], sintering is proposed as an alternative to the chips soldering to improve the strength of the connections. The matching of CTE values and the heat dissipation performance is enhanced with the help of advanced materials [9], [14]. The delamination of the substrate can be reduced by avoiding 90° angles in the pattern, as discussed in [14]. Regulated cooling can mitigate low-term ambient temperature swings, as proposed in [19]. Several methods are deployed for cooling the electronic elements [20], [21]. These approaches are categorized into two main groups, active and passive, as per the fact that an energy resource is needed for the cooling process. Their merits and demerits are provided in [22], [23], and [24]. In the ATC approach, a fluid is normally applied as the coolant, and based on the working fluid's type, a fan or a pump is used to produce the cooling flow and forced convection. Turning to the passive techniques, which are traditional cooling methods, heat sinks, and fins are employed where free convection is the dominant mechanism of heat transfer [25].

ATC is focused on reducing the impact of short and medium-term thermal cycles. The approach uses temperature-related control parameters to adjust the junction

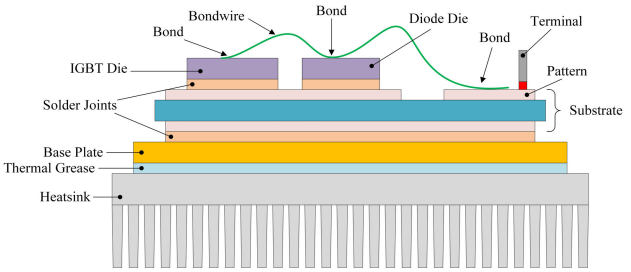


FIGURE 3. Schematic of an IGBT module [32].

temperatures in real time. Its objective is to minimize thermal stress on the module by reducing temperature fluctuations. Thermal control aims to regulate the junction temperatures by adjusting the losses in the targeted chips through specific temperature-related control parameters. These parameters include the switching frequency [26], [27], modulation technique [28], DC-link voltage [29], gate voltage [30], or distributing reactive power [31]. For instance, a short-term temperature drop can be averted or decreased when losses are escalated temporarily by increasing the switching frequency. While CM necessitates understanding the junction temperature, ATC can function without it. Additionally, an electrothermal model can derive real-time estimations of junction temperatures through electrical measurements, enabling more accurate thermal stress management [26].

C. STATE OF CONTRIBUTIONS

Numerous scholars have conducted research on the ATC of power electronics converters, as documented in the literature. A few papers have reviewed the ATC for PSDs and power converters through cooling strategies. Although prior works have proposed various techniques to improve the ATC, CM, and RUL aspects of power electronics converters, there are no solutions to address the ATC of power electronics building blocks (PEBBs) concept, health monitoring of PEBBs, and their aging/degradation. This is particularly important in AESs, where the modular multilevel converter (MMC) based PEBBs concept needs cost-effective ATC methods to reduce maintenance costs and increase reliability/availability. To maintain power converters, it is necessary to anticipate the state-of-health (SoH) and potential damage progression to implement appropriate thermal control measures. The main focus of this research is to provide a detailed overview of various ATC methods applied in different configurations of power electronics converters, including single converter, cascaded or modular converter, and parallel converter configurations. Additionally, the impact of ATC on power module and converter performance is analyzed, with a particular emphasis on reliability, power loss, and junction temperature reduction. Finally, because modular and multilevel converters shape PEBB stacks, the thermal controls of which need to be designed, the paper introduces the concept of PEBBs, specifically focusing on their application in AESs. Furthermore, the scope of future work for ATC of PEBBs in various high-power applications is proposed.

This work will serve as a comprehensive and useful reference for health monitoring, degradation, aging, and thermal management of the PEBBs concept with the help of previous works on power converter topologies in terms of their configuration, modulation strategy, and the most important parameters that are useful for thermal control aspect of PEBBs in AESs.

D. STRUCTURE OF PAPER

The remaining sections of the paper are structured in the following manner. Section II presents various ATC methods categorized by converter configurations (single, cascaded or modular, and parallel) and various ATC methods of power routing for modular converters. Section III provides the ATC methods and various control levels with different bandwidths, such as the ATC methods at the modulation level (including switching loss reduction and conduction loss redistribution), the system function level (including active power or energy storage and reactive power), and the other levels. Section IV provides the discussion, challenges, and scope of future work in the AES power system. This section starts with the introduction of PEBBs concept, the thermal aspect of the PEBBs concept and moves to the discussion on ATC for various topologies related to the PEBBs concept (such as multilevel converters, multi-phase converters, and soft-switched converters). Then it presents ATC methods in the PEBBs concept, the communication protocols of PEBBs, and how they can help ATC methods. After that, this section details the advantages and disadvantages of different converters used for shaping high-power rating converters in the PEBBs concept. Ultimately, this section finishes with thermal data acquisition, health monitoring and degradation, cost analysis, ATC's effect on the system's operation, and PSD technology and packaging aspects for future work. Finally, Section V concludes the paper.

II. ATC METHOD

Before reviewing the ATC methods, a brief explanation of the thermal model used in the literature review should be provided.

A. THERMAL MODEL

Improvement of thermal management systems can be achieved with a highly accurate estimation of semiconductor device temperature. To do so, high-fidelity thermal models must be developed. There are several approaches to developing thermal models, which are discussed below. The measured response from real systems can be adapted to fit the parameters of thermal equivalent circuits. Two standard forms of the thermal circuit have been extensively used for thermal modeling, as shown in Figure 4: Cauer and Foster networks [33]. The following section provides an overview of these two thermal networks.

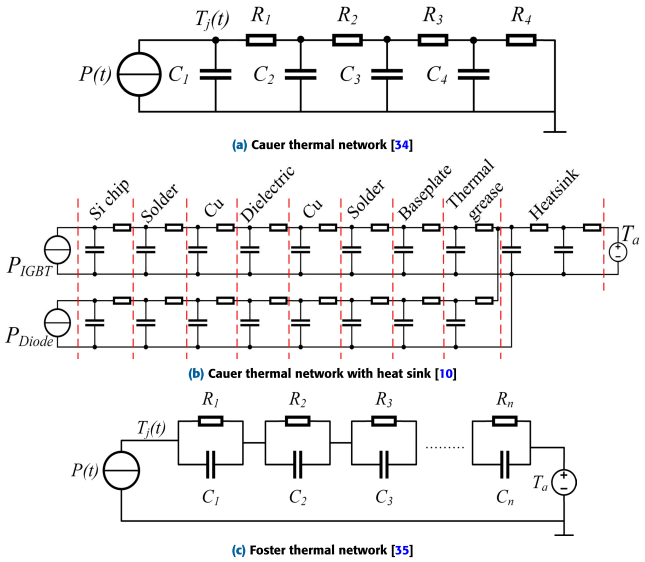


FIGURE 4. Thermal models.

1) CAUER NETWORK

The heat conduction path of a semiconductor material can be modeled by an equivalent electrical circuit, as presented in Figure 4a. This circuit is called the Cauer network [34]. Thermal resistance over the heat conduction path is denoted by R, and C denotes thermal capacitance. The junction and ambient temperatures are indicated by T_j and T_a, respectively. The power dissipation is denoted by P. The Cauer network represents the physical properties of the heat conduction path more accurately, which is a significant advantage. Moreover, this network allows independent modeling of the heat sink and power semiconductor device, as shown in Figure 4b. Later they can be combined to develop intricate thermal models [36]. Nevertheless, the Cauer network is not precisely accurate due to heat spreading. Also, providing exact parameters to the model is a complex process. The advantage of Foster networks is that they are easy to use [35]. However, the use of the Foster network is restricted to specific applications only. And unlike the Cauer network, the elements of the Foster network cannot be designed individually and combined later.

2) FOSTER NETWORK

Foster networks are a non-parametric model tuned to step response data of the thermal conduction path. There is no physical significance of the components in this circuit, and each component only represents a time constant. A typical foster network is presented in Figure 4c. The advantage of Foster networks is that they are easy to use [35]. However, the use of the Foster-type circuit is restricted to specific applications only. And unlike the Cauer model, the elements of the Foster network cannot be designed individually and combined later.

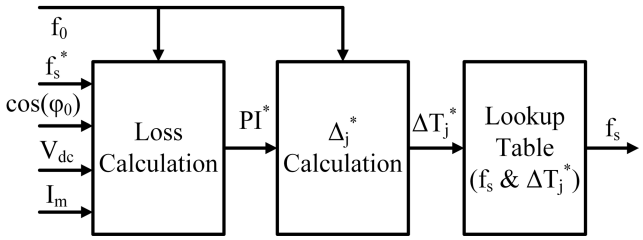


FIGURE 5. ΔT_j control in PWM method [46].

It should be noted that authors in the literature review used various thermal networks with different accuracy and layers depending on the focus of their work (see Figure 3). The thermal modeling of power converters and related mathematical equations used in each paper deserve a separate review paper which is out of this work's scope. Since this paper only focuses on the ATC methods, this work does not review the thermal networks in the literature. Table 1 compares the various thermal models for complexity, accuracy, and multi-chip interfaces [40]. More details and mathematical models of thermal networks can be found in [36] and [40].

B. ATC IN DIFFERENT CONVERTER CONFIGURATIONS

The ATC, as a newly-presented method to modify power losses and thermal stress, will be represented in this section. The central concept behind this problem is to adjust the power converter's control variables related to temperature to modify the junction temperature and reduce damage caused by thermal cycling, as discussed in [27] and [32]. The ATC enhances the reliability of PSDs, thereby increasing the power system's lifetime. The primary objective has been to regulate junction temperature and other related-temperature values. Based on the type of converter, one can categorize the ATC into single, cascaded, and parallel converters. Single converter configurations include 2L and 3L converters in AES and drive applications, as well as converters in solar applications, as discussed in [41] and [42]. Cascaded converter configurations consist of cascaded h-bridge (CHB) converters and modular multi-level converters (MMC) [43], [44]. Lastly, parallel 2L and 3L DC/DC converter configurations have been used in wind energy and motor drive applications.

1) ATC IN SINGLE CONVERTER CONFIGURATIONS

One clear-cut way to adjust the switching frequency is to realize thermal control, which directly affects the power losses [27], [45], and a negligible effect on the power system's working condition. In [46], a method was presented to reduce the switching frequency of a 2L converter in an adjustable speed drive based on changes in junction temperature. As shown in Figure 5, there are three stages to control ΔT_j. First, average power losses are calculated based on power factor and commanded switching frequency (f_s^*). Second, the temperature variation (ΔT_j^*) of the PSD

TABLE 1. Comparison of the most commonly used thermal networks.

Thermal Network	Complexity	Individual Layer	Accuracy	Experimental Input	Multi-chip Interface	Notes
Foster [35]	Simplest	No	Less accurate at high frequency	No	No	Commonly used in industry
Cauer [34]	Less complex	Yes	Accurate	No	No	Commonly used
Finite element method (FEM) [37]	Less complex	N/A	N/A	No	Modeled	high computation burden
Modified Elmore [37]	Complex	Yes	More accurate	Specific points	Modeled	Combines FEM and two RC parallel circuits, Less computation
Modified FEM [38]	Complex	Yes	Most accurate	Specific points	Modeled	Combines FEM and four RC parallel circuits, Less computation
Fourier [39]	Complex	Yes	N/A	No	Modeled	Thermal diffusion, high computation burden

Note. N/A: Information is Not Available in the paper.

is calculated. Third, the switching frequency is determined using a hysteretic control [46]:

$$fs = \begin{cases} f_s^{min} & \Delta T_j^* > T_1, \\ f_s^* & \Delta T_j^* < T_2, \\ unchange & T_1 < \Delta T_j^* < T_2 \end{cases} \quad (1)$$

In the above equation, T_1 and T_2 represent the upper and lower boundaries for the hysteretic temperature variations (ΔT_j^*), and f_s^* is commanded switching frequency. They adjust the switching frequency, which is calculated based on the average temperature (T_{jm}) and the temperature variation (ΔT_j^*). While the results indicate that this control method can enhance reliability more effectively than controlling a single parameter, combining control parameters can increase the computational complexity of the control system.

Modifying the modulation strategies and applying modern control approaches is an excellent way to address the above issue. In [47], a switching control method based on pulse width modulation (PWM) is proposed for managing power losses in the three-level neutral-point-clamped (3L-NPC) converter. The technique described here is active lifetime extension (ALE) and does not require additional equipment. It can be applied to the modulation index (m) range between 0.5 and 1. In this inverter, there exist 27 various switching states in the 3L-NPC, as displayed in Figure 6. Applying different switching states can reduce switching losses or conduction losses. For instance, the region highlighted in light yellow in Figure 6 remarks redundant switching states. Should the conduction losses need to be reduced, the switching states resulting in higher conduction losses are eradicated from the switching sequence. Otherwise, if the reduction of switching losses has priority, the corresponding states are prohibited, as depicted in Figure 7.

The use of different switching states can help to decrease switching or conduction losses. The light yellow section in Figure 6 represents redundant switching states. If it is

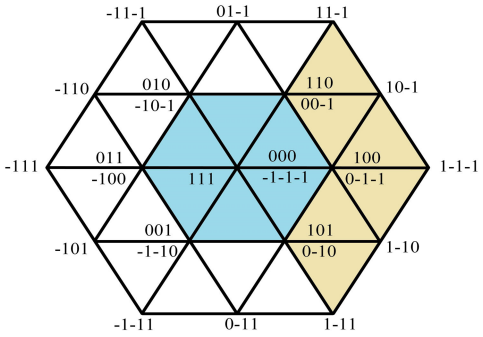


FIGURE 6. Various kinds of switching states in the 3L-NPC inverter [47].

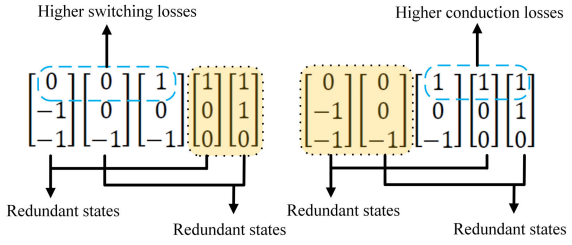


FIGURE 7. The effect of redundant states on switching and conduction losses [47].

necessary to decrease conduction losses, the switching states that result in higher conduction losses are eliminated from the switching sequence. On the other hand, if reducing switching losses must be decreased, the related states are prohibited, as depicted in Figure 7.

The inner hexagon region highlighted in light turquoise in Figure 6 contains redundant switching states that can be utilized to alter the current paths flowing in the PSDs. This alteration helps lower the conduction or switching losses depending on the priority. This control strategy is particularly useful for grid-connected power electronics converters during

fault ride-through (FRT) scenarios, such as high-voltage ride-through (HVRT) and low-voltage ride-through (LVRT), and during start-up operation of drives, where the modulation index is not high, and the voltage reference is in the inner hexagon of Figure 6, as presented in [48], [49], and [50].

The study presented in [51] proposes a junction temperature controller for a 2L-3P converter based on the finite control set model predictive control (FCS-MPC). The controller aims to control the amplitude of thermal cycles and estimates the load current, junction temperature, and leading to thermal stress for all space vectors of the next sampling instant. The cost function parameters are then obtained per these predictions, including the error from the current reference, the thermal stress across the switches, the temperature discrepancy between the chips, and the PSDs' total power losses. After that, the parameters are weighed, and the space vector concerning the lowest cost function is selected and applied to the converter. Figure 8 provides a visual representation of this approach. According to this method, a control sequence for a current-source active rectifier was presented in [52] as a control algorithm based on a finite number of switching states of the power converter. To opt for the optimal switching state, an objective function calculates the error between foreseen and reference values of both electrical and thermal objectives. The results show that the electrical and thermal objectives can be attained by minimizing the multi-objective weighted cost function. It is worth pointing out that the power converter's output performance might decrease, and the computation's complexity might increase.

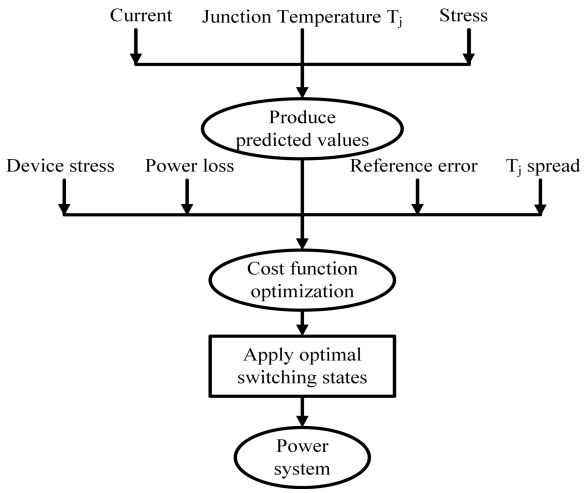


FIGURE 8. Schematic of ATC method based on FCS-MPC [52].

In the study conducted in [52], the authors proposed a control algorithm for a rectifier based on a finite set of switching states of the power converter. The algorithm aims to opt for the best switching state by calculating an objective function (which is based on electrical and thermal objectives) that measures the discrepancy between predicted and reference figures. The findings indicate that the multi-objective weighted cost function can be optimized for the purposes. It bears pointing out that the power converter's output performance may decrease, and the computation's complexity may rise due to the algorithm's implementation.

2) ATC IN CASCADED OR MODULAR CONVERTER CONFIGURATIONS

Modular or cascaded power converters are becoming more prevalent in different voltage ranges. As previously mentioned, the most commonly used topologies for modular power converters are CHB converters and MMCs. For having many cells and submodules, these converters are susceptible to uneven thermal stress, which can negatively impact the PSDs and the overall reliability of the power converter. Ref. [53] presented a thorough review of current state-of-the-art opportunities and the future perspective of MMCs for transportation electrification applications.

In [54], a power routing method was proposed to implement ATC by unevenly distributing the load among the cascaded or modular configuration modules. As shown in Figure 9, power routing involves optimizing the allocation of power among each module to improve the efficiency and reliability of the system [54]. The modules may be connected in series, parallel, or a series-parallel configuration. When connected in a series, the modules share the same current, but each module has the ability to regulate its output voltage. This allows for customization of the power output of each individual module by adjusting its output voltage. Similarly, when connected in parallel, the modules share the same voltage, but each module can independently control its output current, which provides flexibility in adjusting the current output of each module. To regulate the cell's power, the current is the parameter manipulated instead of the voltage. Therefore, this methodology involves using the power routing technique for the CHB converters [55], a modular smart transformer (ST) that comprises a CHB to convert medium voltage AC to medium voltage DC [56], and dual active bridges (DAB) for converting medium voltage DC to low voltage DC [57]. It should be mentioned that the most damaged cells can be conserved with the help of this method. The power routing will be discussed in detail in the next section.

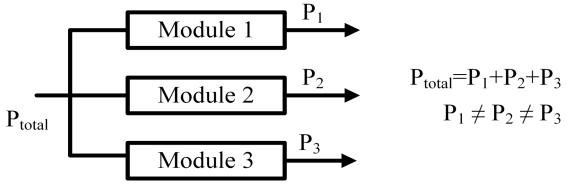


FIGURE 9. The basis of the power routing method [54].

Turning to MMCs, a wide variety of research works have been done on MMCs to enhance the output performance [58], [59], [60], [61], decrease the complexity of computation [62], [63], [64], and also provide a cost-effective power loss balance among submodules [57], [65], [66]. Hence, the ATC technique is commonly utilized to achieve a uniform

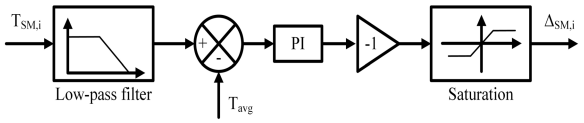


FIGURE 10. The control schematic of the submodule's temperature [70].

distribution of thermal stress across the various submodules of the system, which helps to enhance the lifespan of the power system [57]. For instance, the unbalanced thermal distribution among submodules brought about by the mismatch in the parameters of the submodule was proposed in [67]. Because the capacitors in the submodules are not identical, the switching and conduction losses of the associated submodules will differ, resulting in uneven thermal stress distribution across the submodules. To overcome this issue, an active thermal balancing control method was proposed, which involves integrating the lower IGBT's junction temperature and the capacitor's voltage into an algorithm that employs a weight function. The weight factor is varied between zero and a predetermined value to ensure that there is both equal thermal circulation among the submodules and balanced capacitor voltage levels [68]:

$$L_i = (1-\alpha) \times v^i_{norm} - (\alpha) \times T^i_{norm} \times sing(i_{arm}) \quad (2)$$

In which α represents the weight factor, and v^i_{norm} and T^i_{norm} indicate the variance in the capacitor's voltage and the junction temperature, respectively. The experimental study was done in various case studies considering different submodule capacitors. The findings were used to validate the suggested thermal balancing control techniques that enable uniform distribution of temperature across submodules [67]. Reference [69] presents an approach to incorporate the junction temperature into the capacitor voltage balancing algorithm to achieve uniform thermal distribution among the submodules. Unlike the research in [67], the temperature of the devices within the submodule is combined individually with the dedicated capacitor voltage, resulting in different distinct cost functions for the upper/lower IGBTs and upper/lower diodes. The appropriate cost function is chosen for each sampling instant, considering the current direction in each leg and the need to either insert or bypass submodules. The outcomes indicated that the suggested approach significantly reduced the inconsistency and temperature dispersion among the submodules.

In [70], submodule thermal balancing was achieved by adjustment of the capacitor's voltage of each submodule in a leg and simultaneously maintaining the sum of the voltages of the submodule's capacitor at the rated value to control the voltage of the DC-link. Figure 10 illustrates the comparison between the temperature of each submodule, denoted as $T_{SM,i}$, and the average temperature of all submodules in the leg denoted as T_{avg}, where the difference is fed into a proportional-integral (PI) controller. The PI controller generates the voltage differential for each submodule voltage

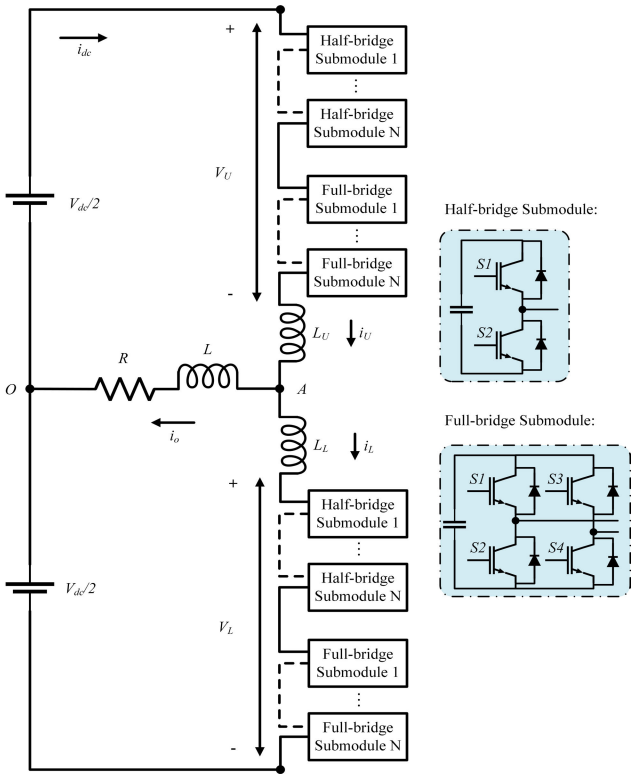


FIGURE 11. 1P hybrid-based MMC topology [71].

reference, as described in [70]. The capacitors' voltages can be adjusted per the work done in [72], but additional terms related to the temperature were considered. It should be noted that while the temperature among submodules was balanced, the capacitors' unbalanced voltages resulted in a distorted voltage waveform of the multi-level leg.

Figure 11 shows that the thermal stress circulation among the submodules of hybrid-based MMC can become more unbalanced under a high voltage modulation index, as noted in [71]. The ATC was introduced for half- and full-bridge submodules to address this issue. In the case of full-bridge submodules, two kinds of bypassed switching modes were modified to produce a symmetrical switching arrangement when the leg voltage is positive, as depicted in Figure 12 [71]. The same procedure is applied when the voltage of the leg is negative. While the power loss distribution in full-bridge submodules is more balanced, the symmetrical switching arrangement does not negatively affect the performance, decreasing thermal stress on the most highly stressed devices. In addition, a thyristor that can resist high current is connected in parallel with the lower leg of the submodule, as shown in Figure 13, to bypass the positive current of the leg to decrease the thermal stress across the lower IGBT.

3) ATC IN PARALLEL CONVERTER CONFIGURATIONS

A feasible solution is to use a parallel connection of many power converters to address the challenges of applications where the current is high and the output voltage is low.

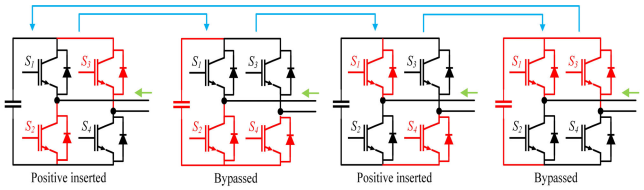


FIGURE 12. The configuration of switching states when the leg voltage is positive [71].

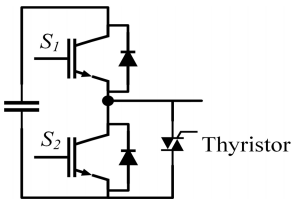


FIGURE 13. Half-bridge submodule with a parallel thyristor [71].

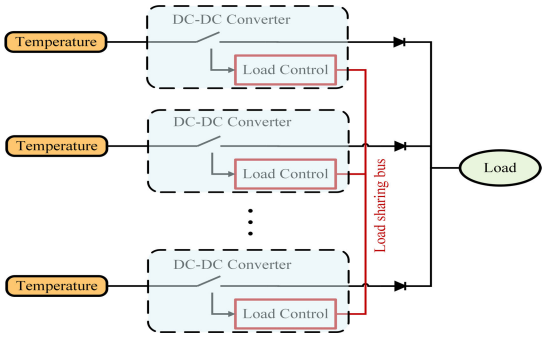


FIGURE 14. The thermal loading control method [73].

This configuration enhances the system's reliability as redundancy can be straightforwardly applied. However, even though sharing the load is used to dispatch the load current and achieve an equal load sharing, it does not ensure an equal thermal stress circulation among the parallel converters. To address this, an active thermal sharing for the parallel DC/DC converter was presented in [73], [74], and [75]. This approach uses the power converters' temperature values to redistribute the load current between parallel converters. Figure 14 shows that the current and temperature data were combined, and the resulting data was utilized to improve load sharing. The purpose of this control diagram is to ensure that the thermal stress is spread evenly. The merit of this method is its ease of implementation. However, it should be noted that there may be a small rise in the failure rate of individual converters.

Implementing a droop-based ATC method, as described in [81] and [82], can enhance the system's reliability. In addition, [76] proposed a control approach for sharing the load in which the droop gain is adjusted per the computed lifetime and calculated as the sum of the used lifetime. This is expressed in the following equation:

$$R_{d,k} = ACL_{k(pu)} \times R_{do} \tag{3}$$

where R_{do} is the highest acceptable value of the droop gain. To achieve load sharing among the converters based on the thermal stress across the PSDs and ensure equal used lifetime for all converters, it is necessary to regulate the corresponding droop gains in accordance with the used lifetime of each converter. By doing so, the accumulated used lifetime of the converters can be balanced, resulting in the improved overall reliability of the system.

The power routing approach can also be utilized in a parallel configuration to achieve balanced aging of the converter cells. This method was proposed in [77] and [78] for a parallel DC/DC converter and a two-level voltage source converter (2L-VSC) in a permanent magnet synchronous motor (PMSM), respectively. Specifically, it reallocates power to each converter cell based on its aging status, accomplished by regulating the duty cycle to produce the appropriate switching pulses. By extending the lifetime of the most aged cell, the reliability of the entire system is enhanced.

In wind power applications, as depicted in Figure 15, the parallel converter configuration has a drawback of significant temperature variation for the fluctuation of the wind speed. To mitigate temperature fluctuations in the PSDs resulting from changes in wind speed, such as wind gusts, the ATC method was implemented in the wind power system, taking into account reactive power, as shown in Figure 15 [31], [79], [80], and [83]. The delivered reactive power can considerably affect components' loading in this configuration. It also does not affect the converter's existing mechanical/electrical power.

The reactive power can regulate the phase angle (between the output current and voltage). It also alters the current flowing through the PSDs, which will impact the power loss and thermal stress across the PSDs. Using an appropriate amount of reactive power to heat the device when the power is low will significantly reduce the temperature fluctuation of the PSDs. However, it bears noting that using reactive power has some demerits, including being applicable only in parallel converter configurations and increasing the diodes' thermal load.

Table 2 summarizes the most critical ATC methods for power converters based on various configurations.

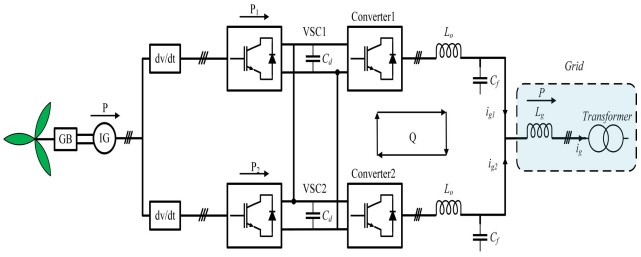


FIGURE 15. Wind power system with parallel converter configuration [79].

C. ATC AND POWER ROUTING

Power routing is an advanced active thermal management technique that balances the thermal stress within modular

TABLE 2. Summary of important ATC methods based on power converter configurations.

Config.	Converter	Method	Advantages/Highlights	Disadvantages/Comments
Single Converters	1P H-bridge inverter [45]	Switching frequency control	Reduces thermal swing resulting from power cycling.	Changing switching frequency may increase harmonics.
	2L converter [46]	Switching frequency control	Adapts switching frequency to junction temperature changes for reduced power losses.	Added 3rd-order harmonic to increase the voltage transfer ratio, but no harmonic result was provided.
	3L-NPC converter [47]	Switching control based on PWM	Reduces switching or conduction losses via space voltage vector redundancies.	Increased ripple and potential higher computational burden.
	3L-NPC converter [48] - [49]	SVM	Optimal loss and thermal redistribution under LVRT	The proposed method's dependency on heat sink design and PSD usage can alter thermal distribution.
	2L-3P converter [51]	FCS-MPC	Controls thermal cycles and optimizes power losses through cost function-based selection of space vector.	Computation burden should be analyzed.
	2L-3P converter [52]	FCS-MPC	Optimizes switching states by minimizing a multi-objective weighted cost function: DC-link control and ATC	Computation burden should be analyzed.
Cascaded or Modular Converters	Modular STs with CHBs [54] - [56]	Power routing	Unevenly distributes load among modules to improve efficiency and reliability	Efficiency in modular architecture requires simultaneous attention.
	Modular STs with CHB & DABs [57]	Power routing	Enhances block lifetime by internally routing power in a modular power converter, including a CHB connected to DABs.	Applicability limited to ST systems not mentioned.
	MMC [67] - [71]	Sorting algorithm	Achieves thermal stress balance by integrating junction temperature and capacitor voltage into control algorithms.	Computation burden should be analyzed.
Parallel Converters	DC/DC converter [73] - [76]	Load sharing control	Utilizes temperature values to redistribute load current among parallel converters, ensuring equal thermal stress distribution.	Possibility of slight increase in individual converter failure rate.
	DC/DC converter [77] - [78]	Power routing	Achieves balanced aging of converter cells by reallocating power based on aging status.	No studied effects of power routing on harmonics.
	Parallel converter [31], [79] - [80]	Reactive power control	Alleviates temperature fluctuations by utilizing reactive power to regulate phase angle and minimize thermal stress.	Reactive power circulates exclusively within parallel converters to heat up PSDs without being injected into the power grid.

power electronic converters [84]. Through the power routing approach, each modular power electronic converter module manages a different amount of power to mitigate the thermal stress generated by thermal cycling. The primary goal of this method is to prolong the lifetime of the most vulnerable modules in a modular power electronic converter. This is achieved by operating the modules under uneven loading conditions and reducing the stress on the most deteriorated modules by transferring their load to less vulnerable modules.

Figure 16a shows a modular converter with three modules where modules 1 to 3 handle power P_1 to P_3, respectively. So, the total power will be $P_T = P_1 + P_2 + P_3$ where $P_1 = P_2 = P_3$ under regular operating conditions. However, under balanced load-sharing conditions, the aging of the modules will be unequal, which might lead to an untimely breakdown of the modules and, thus, unscheduled maintenance. Figure 16b shows that, with the implementation of power routing, each module handles a different power value depending on its aging status. In this way, power routing can be applied to optimize the maintenance schedule and increase the lifetime of modular power converters. The cells within a modular converter can be linked in a series, parallel, or hybrid arrangement, as shown in Figures 17a, 17b, and 17c, respectively [85].

In the case of modules connected in series, the output power of each cell can be managed by adjusting the output voltage of each cell. Likewise, for parallel connected modules, the output power from each cell can be regulated by adjusting the output current from each cell. Lastly, for a combined series and parallel structure, the current, voltage, or both can be controlled to regulate the power output from each cell. The primary goal of power routing is to improve the converter's lifetime by optimizing its maintenance schedule. Calculating the converters' RUL and SoH is necessary to apply power routing methods effectively. Then maintenance can be scheduled simultaneously for all the modules of a power electronic converter by considering the RUL of the modules. This concept is illustrated in Figure 18 in which RUL equalization is achieved between two PEBBs. Here the red bars indicate the expected failure time of the two PEBBs,

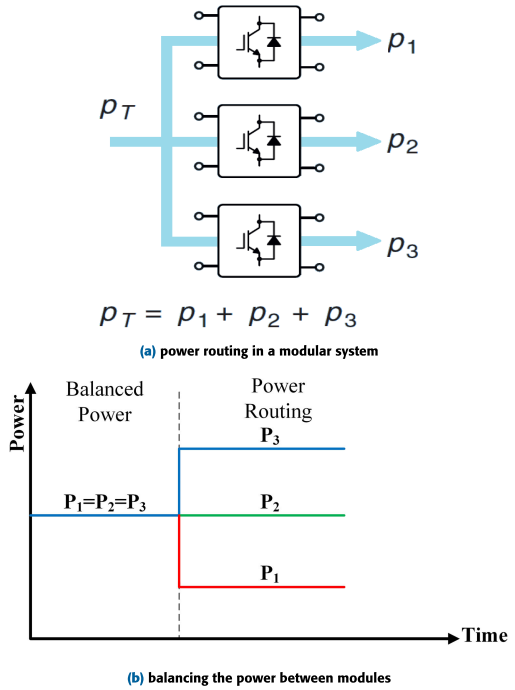


FIGURE 16. Power routing concept [54], [85].

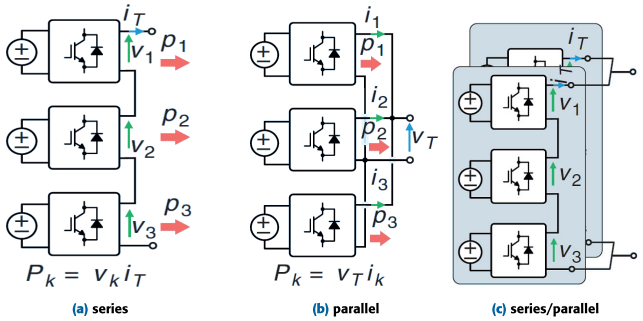


FIGURE 17. Power routing in different modular converter topologies [54].

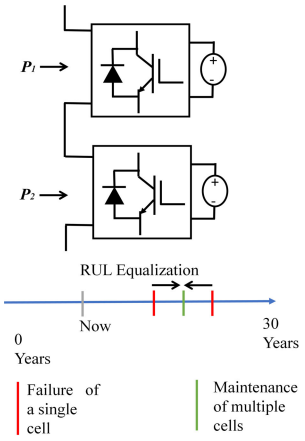


FIGURE 18. RUL management via power routing [84].

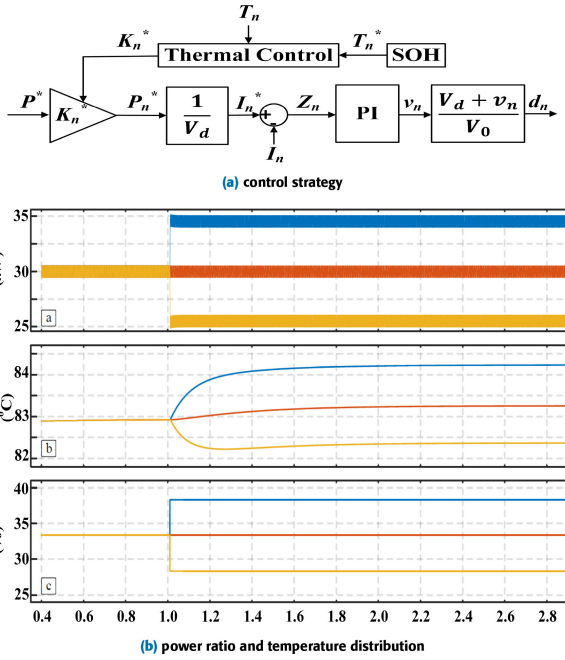


FIGURE 19. Power routing in three-cell DC/DC boost converter [77].

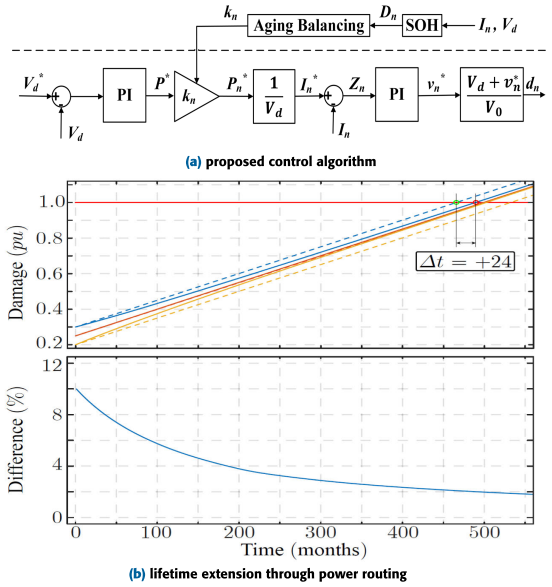
and P_1 and P_2 indicate the power each PEBB processes. By applying the power routing method, the power managed by each PEBB can be manipulated so that maintenance for both PEBBs is scheduled at the exact same time. The green bar represents the unified maintenance schedule for both PEBBs.

The power routing method can be employed for modular converters to regulate the temperature of the PSDs and increase their RULs. Several approaches have been investigated in literature for implementing power routing techniques with series and parallel connected converters, as discussed in the sections below.

1) POWER ROUTING IN PARALLEL-CONNECTED MODULAR CONVERTER

A closed-loop controller has been implemented in [77] that considers the SoH of a three-cell parallel-connected DC/DC converter to improve the maintenance cost of the system, as shown in Figure 19a. Figure 19b shows the control scheme for such a converter and the simulated results.

Here, the SoH block estimates the aging of each cell by utilizing data on the usage of the power system and instantaneous electrical measurements. Then it provides a temperature reference (T_n^*) to the thermal controller block, determining the appropriate power-sharing factor (k_n^*) for the parallel cells. Afterward, the reference power for each individual cell (P_n^*) is determined by dividing the total instantaneous reference power (P^*) by the control factor (k_n^*). From the reference power, it is possible to determine the reference current (I_n^*), which can be utilized to calculate the voltage (v_n) that must be modulated by each individual cell. A conventional PI controller assists in determining v_n. The proposed



(a) proposed control algorithm

(b) lifetime extension through power routing

FIGURE 20. Lifetime estimation of three-cell DC/DC boost converter [86].

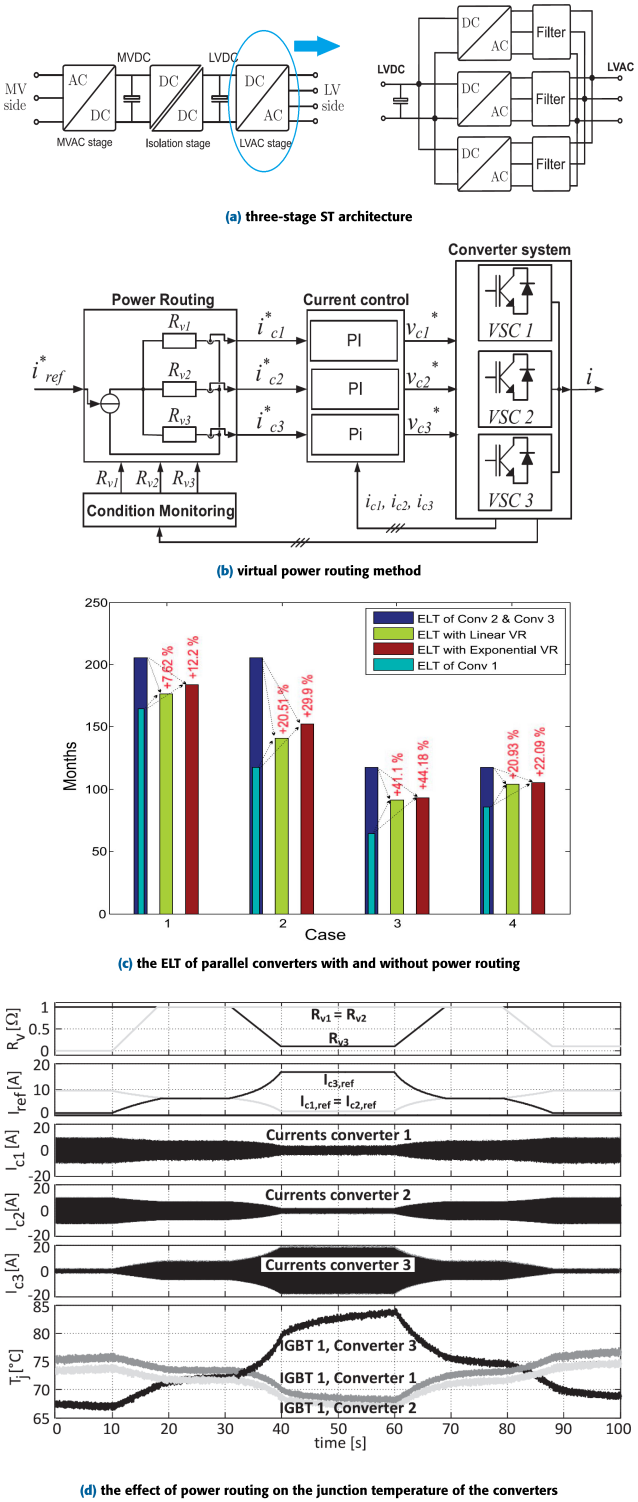
algorithm successfully redistributes the power among the cells and achieves thermal management.

A power routing mechanism is presented in [86] that decreases the aging imbalance in an interleaved boost converter with three modules. Figure 20a depicts the proposed control algorithm. The upper segment of the control scheme determines the power that needs to be processed by each module to re-balance the RUL of the modules. The bottom segment of the control scheme employs two PI controllers to determine the reference power P_n^* and reference voltage for the power electronic devices. The application of power routing allows proper thermal management of the cells and extends the converter's overall lifetime, as shown in Figure 20b. By the utilization of the suggested power routing approach, the lifetime of the most vulnerable power module has been extended by 24 months.

A virtual resistance-based power routing technique for parallel converters of the low voltage stage of an ST is presented in [56]. The power routing method is utilized when the power system is under partial load. The arrangement of the 3-stage ST for power routing is depicted in Figure 21a. The LV side consists of three parallel connected converters. The proposed control framework for implementing the power routing method is depicted in Figure 21b. Here, three virtual resistors (R_{v1}, R_{v2}, and R_{v3}) are used to distribute power among the three converters. The values of resistors are adjusted based on the feedback obtained from the CM and are determined as a function of the cumulative damage:

$$R_{vi} = f(D_{acc}) \tag{4}$$

The accumulated damage is estimated by sensing the semiconductor device's junction temperature (T_j). A path with high resistance indicates low loading, and vice versa for a low-resistance path. The reference current for any specific converter (i_{cn}^*) can be calculated by using the total reference current (i_{ref}^*) generated by the voltage controller and the



(a) three-stage ST architecture

(b) virtual power routing method

(c) the ELT of parallel converters with and without power routing

(d) the effect of power routing on the junction temperature of the converters

FIGURE 21. A virtual power routing technique for parallel converters in an ST [56].

virtual resistors as expressed below [56]:

$$[i_{c1}^*, i_{c2}^*, i_{c3}^*] = \left(\frac{i_{ref}^*}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}}\right) .[R_{v2}R_{v3}, R_{v1}R_{v2}, R_{v1}R_{v3}] \quad (5)$$

Figure 21c depicts the converters' estimated lifetime (ELT) with different initial damages. The converters will break down after different intervals if power routing is not applied. The ELT of the most aged cell in the system can be extended with the virtual resistor-based power routing technique. Figure 21d illustrates the effect of the suggested power routing approach on the converters' junction temperature. Initially, the load on converter number 3 is less than the other two converters, and after $t = 20s$, converter number 3 is loaded more than the other converters.

The graph shown in Figure 21d illustrates that the virtual resistors cause the current to vary, and as a result, the junction temperature changes with the loading of the converter. When a converter is not in use, the junction temperature decreases, but when the load on the converter increases, the junction temperature rises again. A power routing algorithm for a more electric aircraft (MEA) with four parallel DABs has been proposed in [87] and [88] to improve the system's lifetime. The MEA architecture and the control algorithm are shown in Figures 22a and 22b, respectively. The power routing algorithm presented in this study estimates the RULs of the converters by analyzing the junction temperature profile generated by the converters' mission profile. The total damage for each converter can be calculated as follows [88]:

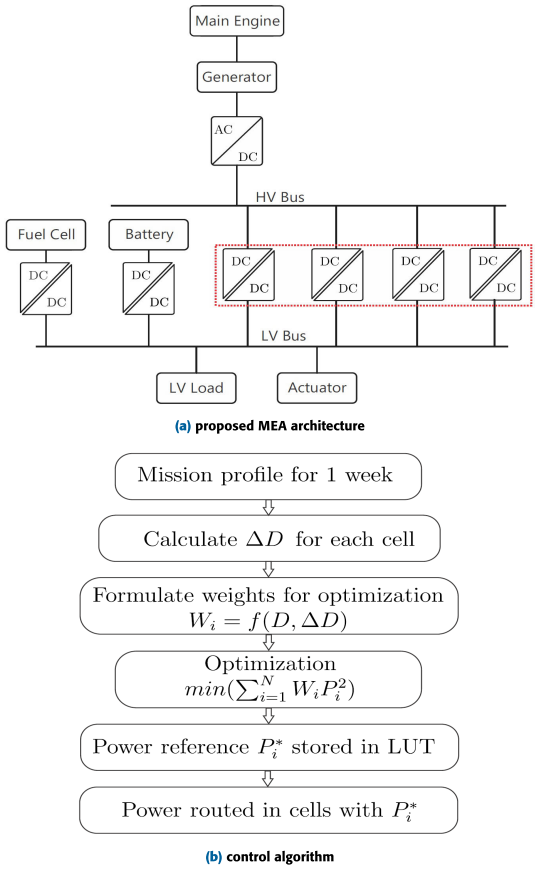


FIGURE 22. Power routing for an MEA [88].

$$D_i = D_{ini,i} + \Sigma_{period=1}^{m} \Delta D_i \quad (6)$$

where D_i is total accumulated damage and $D_{ini,i}$ is initial damage. The RUL for a specific converter can be expressed below [88]:

$$LT_{exp,i} = \frac{1 - D_i}{\Delta D_i} \quad (7)$$

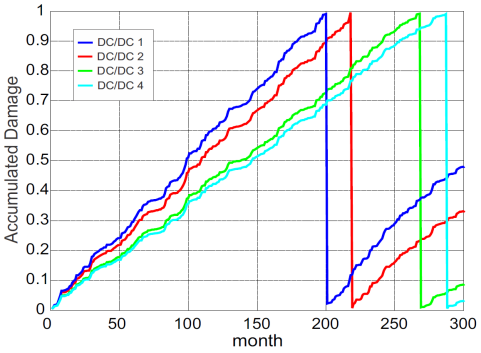
where ΔD_i is the rate of damage change over a specific time interval. Due to thermal cycling, the RUL for each converter is different, and the controller determines the power each converter must process to extend the lifetime of the converter. During the full load operation, all converters process an equal amount of power, while the power routing algorithm is solely operational under partial load conditions. Figure 23a illustrates the accumulated damage of the converters, both with and without the implementation of power routing. The cells wear out at a different rate when no lifetime control method is activated. The cells process power as per their thermal stress with active lifetime control. Thus, the accumulated damages converge to a common point, as seen in Figure 23b.

The effect of power routing on the aging of the ST's ten parallel connected DAB cells is investigated in [89]. The finding from this study is depicted in Figure 24. Figure 24a illustrates the damage sustained by the DAB cells while sharing the power equally for 400 months. The first breakdown occurs in the 200th month, and the last occurs in the 370th month, leading to several interruptions in regular operation due to maintenance intervals. However, while the power routing algorithm is implemented, the breakdown of all cells occurs in the 293rd month (Figure 24b), which reduces the maintenance intervals.

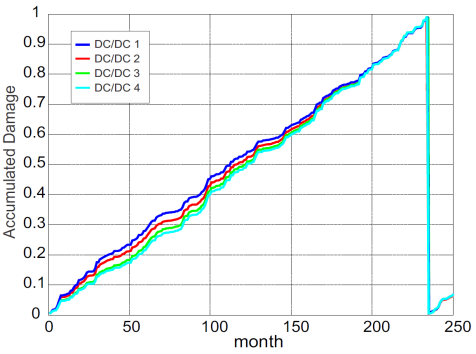
A case study has been presented in [54] to demonstrate the effectiveness of power routing in reducing the thermal cycling of the most deteriorated cells of the low-voltage conversion stage of an ST. Figure 25 shows the results from this study, where cell 1 was the most deteriorated cell. The proposed power routing technique reduces the thermal cycling in cell one, which results in the extension of the lifetime of cell one. The efficacy of the virtual resistors-based power routing method in reducing thermal stress in a modular DC/DC converter, in which several quadruple active bridges (QABs) converters are included, has been investigated in [90]. The outcomes obtained indicate the efficiency of the control algorithm in postponing the system failure.

2) POWER ROUTING IN SERIES-CONNECTED MODULAR CONVERTER

Modulation strategies that have been modified can be utilized to apply power routing in modular converters that are connected in series and parallel. These strategies enable the

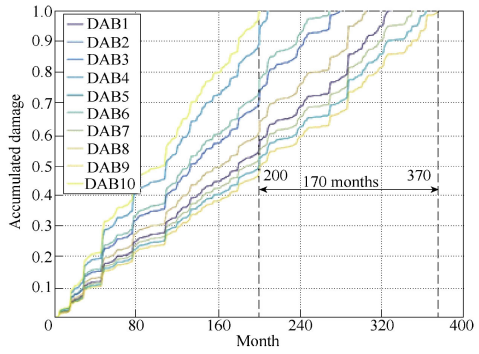


(a) when power routing is not enabled

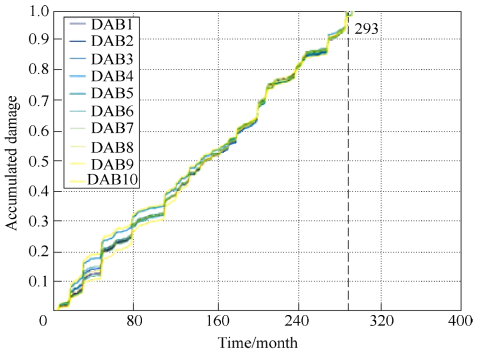


(b) when power routing is enabled

FIGURE 23. Impact of power routing on the accumulated damage [88].



(a) when power routing is not enabled



(b) when power routing is enabled

FIGURE 24. The impact of power routing on the aging of DAB cells [89].

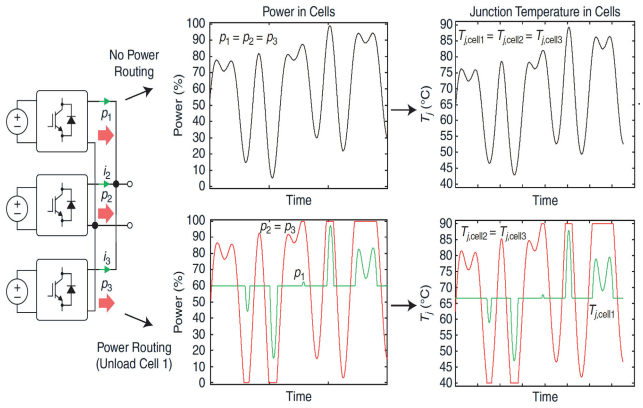
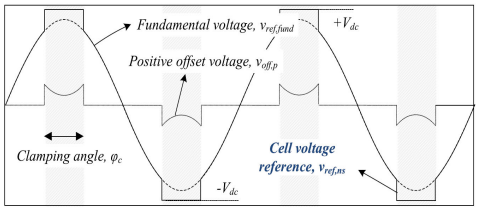
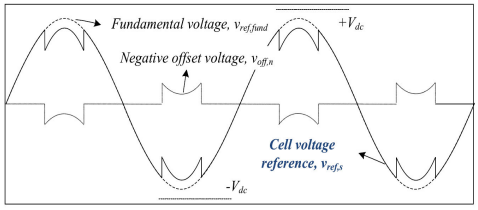


FIGURE 25. Thermal cycle reduction in the most aged cell of the LV stage converter in an ST [54].

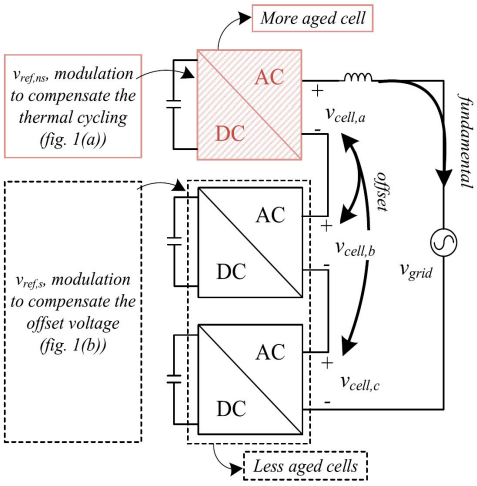


$v_{ref,ns}$ for a reduction of the switching losses



$v_{ref,s}$ for compensation of the offset voltage

(a) proposed DPWM method



(b) proposed modulation strategy

FIGURE 26. Power routing with DPWM method [91].

control of the thermal stress of each converter individually. A discontinuous PWM (DPWM) based power routing technique for CHB converters is presented in [91]. The DPWM reduces the switching loss by clamping the output voltage at either the positive or negative DC-link voltage. The loss reduction is significant compared to the continuous PWM

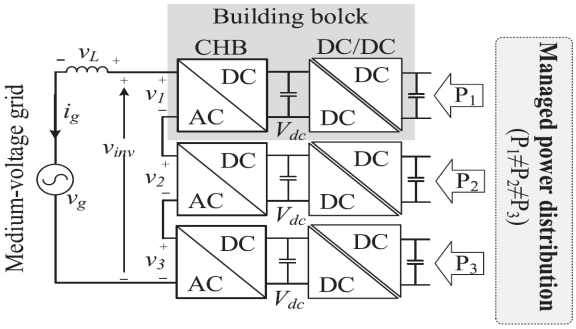


FIGURE 27. Modular ST [92].

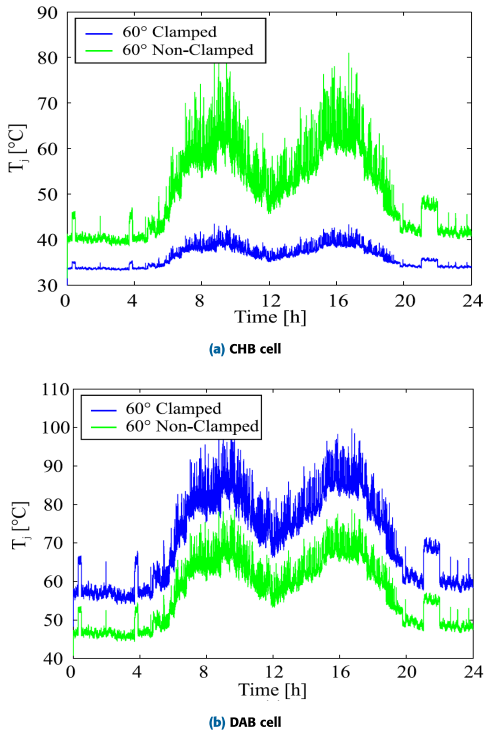


FIGURE 28. Junction temperature of CHB and DAB cells with and without clamping signal [92].

techniques because the semiconductor devices cannot switch in the clamping region. As shown in Figure 26a, the proposed method has two modulation signal types. A positive offset voltage $V_{off,p}$ is added to the fundamental reference voltage $V_{ref,fund}$ to obtain the modulation signal $V_{ref,ns}$, which has a clamping zone. The most vulnerable converters are modulated with $V_{ref,ns}$ as the clamping region reduces the generated losses. The other modulation signal $V_{ref,s}$ has no clamping region and a negative offset voltage $V_{off,n}$, compensating the clamping of other converters. The less vulnerable converters are modulated with this signal. The ultimate goal of the modulation strategy is to delay the failure of the most vulnerable converters. The modulation strategy's application is depicted in Figure 26b, depending on the converters' condition. The converter with lesser RUL is modulated with $V_{ref,ns}$ to decrease the thermal stress, and the one with higher RUL is modulated with $V_{ref,s}$, compensating for the positive offset voltage.

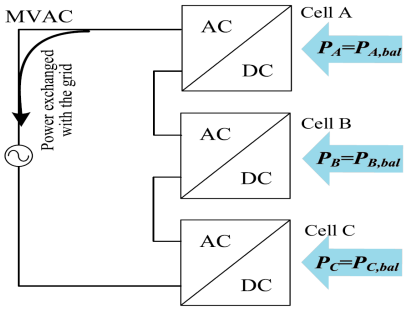
The power routing concept presented in [91] is extended in [92] that applies a discontinuous modulation technique to the medium-voltage alternating current (MVAC) to low-voltage direct current (LVDC) building block of an ST to achieve thermal management (Figure 27). This study considers the DAB as the DC/DC converter. After applying the proposed modulation technique, the estimated CHBs' and DABs' junction temperatures with a fixed 60° clamping angle are shown in Figures28a and 28b, respectively. For the CHB cell, the junction temperature rises to 82°C with the non-clamped signal, while for the clamped one, the junction temperature reaches around 43.5°C. For the DAB cells, the maximum junction temperature reaches 99.8°C with the clamped signal and 78.7°C for the non-clamped signal.

An advanced discontinuous modulation technique for implementing power routing in STs has been proposed in [93] that manages the thermal stress within the CHB converters and the isolated DC/DC converters. Another power routing technique for improving the thermal performance of CHB converters has been proposed in [94]. This work has applied a non-conventional phase-shifted PWM that increases the most vulnerable cells' lifetime and reduces the cells' harmonic distortion. A multi-frequency modulation-based power routing technique is presented in [55], where a third harmonic component is injected into the duty cycle of CHB converters. The injection of a third harmonic component maximizes the utilization of DC-link voltage, akin to the third harmonic injected PWM (THIPWM) method. Figure 29 illustrates a 3-cell CHB converter featuring three paths (P_A, P_B, and P_C) for power flow. Failure of any single cell or power path will stop the operation of the converter. One approach to avoid this situation is to decrease the load on the power path with the highest degradation level. Figure 29b depicts a scenario where the loading on power path A is reduced to protect cell A from untimely breakdown.

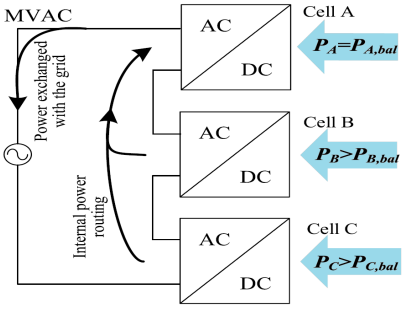
Figure 29 demonstrates the concept of unbalanced power-sharing between a three-cell CHB where the first three rows show the duty cycle of the cells, and the fourth row shows the power-sharing between the cells. In Figure 30a, the power-sharing is balanced between the cells, with each cell having the same duty cycle. Figure 30b shows unbalanced power sharing between the cells where the cells with higher loads have a higher duty cycle. Here, the unbalanced power sharing is restricted when the duty cycle becomes maximum. The power imbalance capacity is extended when the third harmonic voltage is injected with the fundamental voltage, as shown in Figure 30c.

III. ATC METHOD AND CONTROL LEVELS

The failure procedures of power converter elements are not straightforward and rely on several decisive factors [10], [68], [95], [96], [97]. Thermal cycling, which refers to temperature variations of the power converter, is a common cause of

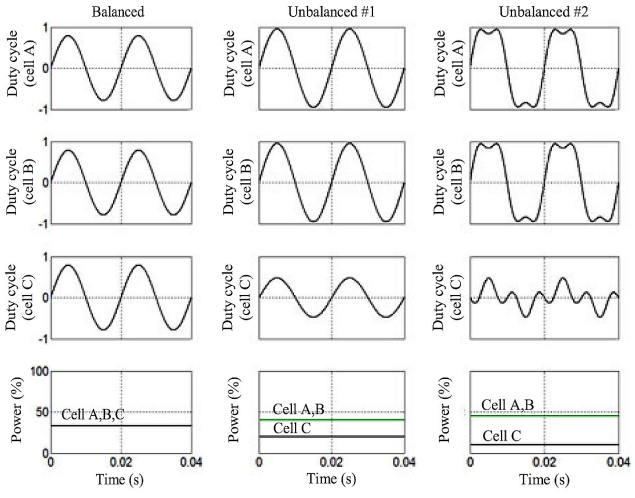


(a) 3-cell CHB with balanced power-sharing



(b) 3-cell CHB with unbalanced power-sharing

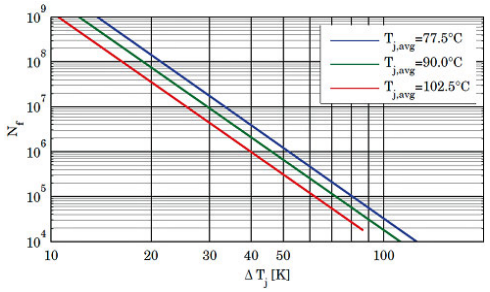
FIGURE 29. Power flow between CHB cells in case of balanced and unbalanced power-sharing [55].



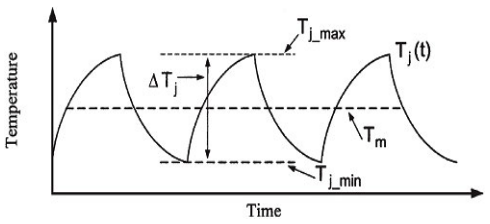
(a) balanced with the same duty cycle (b) unbalanced with fundamental voltage (c) unbalanced with third harmonic injected

FIGURE 30. Power routing technique [55].

failures in converters. Temperature fluctuations on various materials with different CTE can bring about continuous interruptions in the contacting areas within or between the elements, ultimately leading to a shortened lifespan of the entire power converter. A multitude of producers of power converter elements, like the PSD or capacitors, have modified their lifespan approaches, which are more than capable of making an accurate and reliable estimation of the lifespan as per specific thermal behaviors seen by the elements [12], [98], [99], [100]. A research study conducted in the 1990s aimed to establish a numerical correlation between the thermal cycling features of the IGBT, the quantity of failed thermal cycles, the rise in the temperature fluctuation dT_j, and the average temperature value T_m. The study found that the lifetime of PSDs decreases as the temperature fluctuation and mean temperature level increase, as shown in Figures 31a and 31b, respectively. This correlation was described and validated based on several analytical models and lifespan tests in [12], [101], [102], [103], and [104]. What is more, other determining factors; such as the extensive usage of power electronics, network, and electric machine faults, short-circuits and open-circuits, inrush current, etc.; can have a negative role in thermal loading and hence bring about overheating damages to the converter. In general, the power determines the voltage or current of the converter. The variation in the loading of power converter components can hugely influence the variable mission profiles, especially in applications like motor drives, photovoltaic systems, or wind turbine systems, where the power is inconsistent. This leads to complex thermal behaviors and burning-out failures of the elements [105].



(a) cycles/failure ratio of the IGBT in different temperatures [51]



(b) typical average junction temperature profile of IGBT [27]

FIGURE 31. Numerical correlation between the thermal cycling characteristics of the IGBT and the quantity of failed thermal cycles.

The thermal cycling in each device varies depending on the place and reasons for the failure. As a case in point, an empirical temperature measurement study on an opened IGBT using an infrared camera is depicted in Figure 32, where the IGBT's real-time temperature in a 10kW 3P-3L-NPC photovoltaic (PV) inverter is presented. The configuration of the power converter is illustrated in Figure 33 [106]. The chip temperature T_j and base plate temperature T_c are two testing points for measurement. The thermal profiles of these measured temperatures are represented in Figure 32a, in which the converted power alters as the solar irradiance changes. Figure 32a illustrates that the temperature of the junction (T_j) is higher than that of the case (T_c) when there are bigger magnitudes

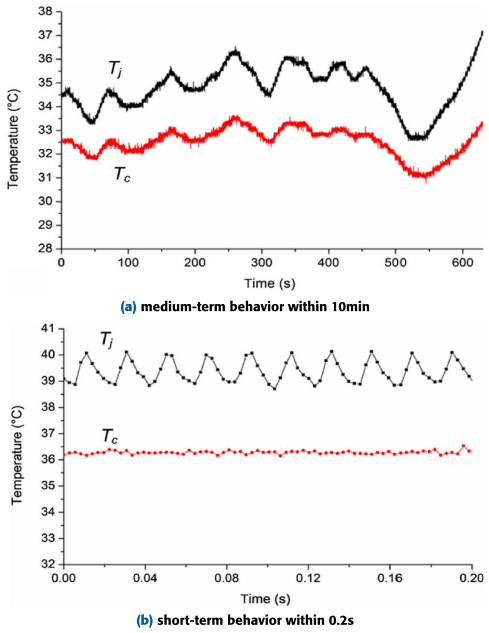


FIGURE 32. Testing outcomes of thermal behaviors inside the PSD [106].

of thermal variations and slow variations in temperature due to power changes. The thermal behavior of T_j and T_c over a shorter time period of 0.2s is shown in Figure 32a, where the solar irradiance maintains consistent, and the converter is loaded at a nominal power of 10kW. Another type of thermal cycling is shown in Figure 32b, where T_j fluctuates faster at a frequency of 50Hz with a smaller but steady magnitude.

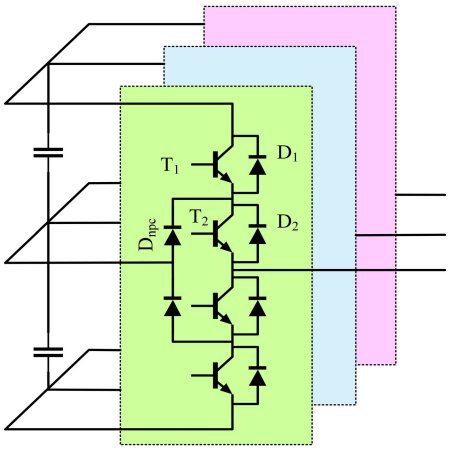


FIGURE 33. Configuration and testing conditions for figure 32 [106].

It can be concluded that the lifespan and reliability of a converter rely heavily on the thermal loading of the PSDs. Various aspects of the energy conversion system's operations can affect the converter's thermal feature. Consequently, the thermal stress across the PSDs can vary significantly as per their places and the disturbances for the converter's load, resulting in different behaviors and time constants.

By and large, the failure of an individual element can occur due to a discrepancy between the stress level, which refers to the thermal loading or cycling of the device, and the strength level, which is represented by the device's intrinsic ability or rating to endure thermal stress. According to Figure 34, the thermal stress experienced by a PSD relies heavily on the user's behavior and mission profile, making it preferable to have a range of stress levels instead of a single point of focus. Furthermore, the strength of individual elements must have a distribution degree to account for variations in production and installation into the system. Consequently, an intersection area between the stress and strength levels can be recognized, which indicates a likelihood of failure.

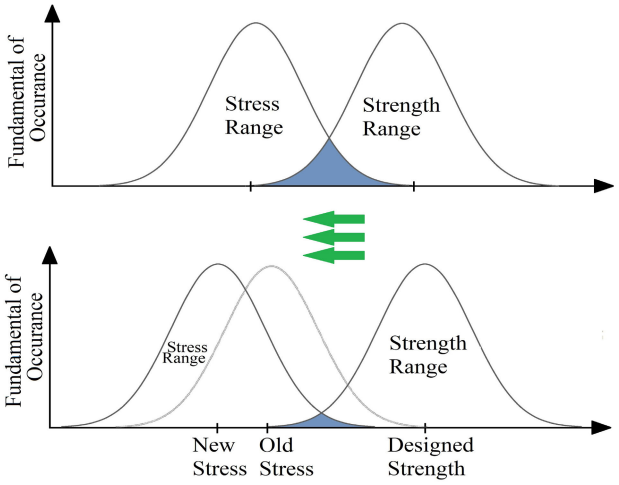


FIGURE 34. ATC for enhanced reliability of power converters.

One practical approach to reduce the probability of failure or increase the reliability of power electronic elements is to minimize the crossing area between the stress and strength levels, which can be achieved by reducing the stress range. As shown in Figure 34, this can be accomplished by decreasing the thermal loading of the PSD by minimizing fluctuations or reducing the mean temperature. Thus, the converter's strength does not require to be altered, and no extra hardware cost is required to improve the strength of elements.

As mentioned earlier, several aspects with different time constants influence a converter's thermal behavior. Therefore, there are ample opportunities and degrees of freedom to modify the thermal loading of the PSDs, resulting in more desirable reliability characteristics. Due to the relatively high power loss density and intense thermal cycling, PSDs are considered one of the most fragile elements in power electronics converters [10], [68], [97].

The control layers and variables in a converter provide various possibilities to change the thermal behavior of the PSDs. Figure 35 depicts the different control levels, with the gate driver being the lowest. At this level, the voltage and current of the drive and gate resistance can be adjusted to revise the PSD's switching power loss and temperature. The bandwidth

at this level is relatively high, around a few microseconds. The modulation level can be used to control thermal behavior by adjusting the switching frequency, as shown in Figure 35. This method can modify the switching and conduction losses of the PSDs without affecting the converter's performance. The bandwidth at this level depends on the switching frequency, around ten to hundreds of microseconds. At higher levels, thermal control can be achieved by changing the output voltage, the output current, the DC-link voltage, the active power, and the reactive power. The bandwidth at this level is quite low, around a few milliseconds.

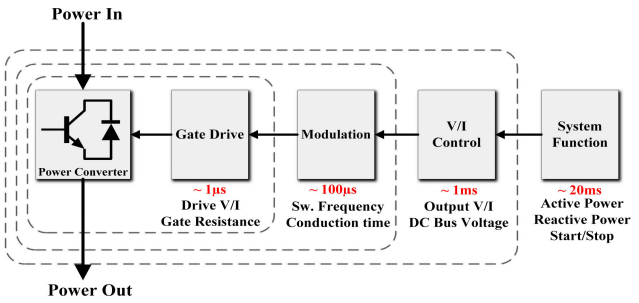


FIGURE 35. Various control layers to manage the thermal behavior of the power converters [107].

A. ATC AT MODULATION LEVEL

Switching control methods in power converters influence the total harmonic distortion (THD) of the output voltage and current. It also determines the path of the current in the PSDs. Many switching control methods have been advanced to reach higher DC-link voltage, lower loss distribution, and lower THD values [108], [109]. Since the switching control methods can change the PSDs' loading, they can enhance the loss distribution among PSDs, leading to superb thermal loading and reliability. The switching control method's effect on the PSDs' thermal loading can be described according to the switching and conduction loss.

1) MODULATION WITH SWITCHING LOSS REDUCTION

Utilizing improved PWM techniques such as DPWM or declining the carrier frequency can remarkably reduce switching losses [110], [111], [112], [113], [114], [115], [116]. However, a trade-off must be considered, as a reduced number of switching counts can lead to higher current ripples [117]. Declining switching loss in a 2L-VSC is a highly recognized approach, as seen in Figure 36. DPWM is a method that is used to decrease switching loss. It involves clamping the voltage reference of the output to the upper or lower section of the carrier during specific intervals to maintain the related PSDs in their current state without turning ON or OFF, reducing switching loss during that subinterval. The process is depicted in Figure 37. DPWM can decline the total loss of the IGBT, resulting in a lower junction temperature swing. Figure 37b shows that the conduction loss of the device can also be altered with DPWM.

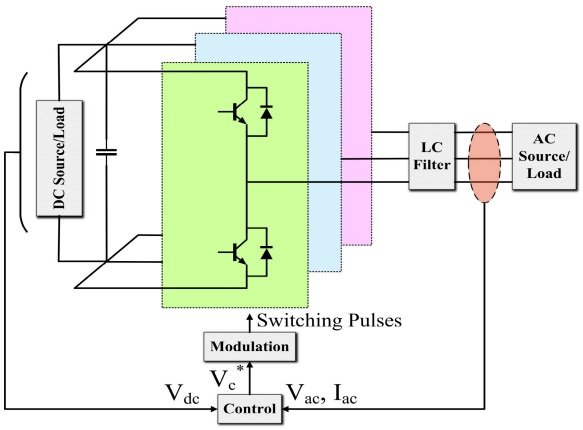


FIGURE 36. The 3P-2L-VSC converter: configuration and control approach [32].

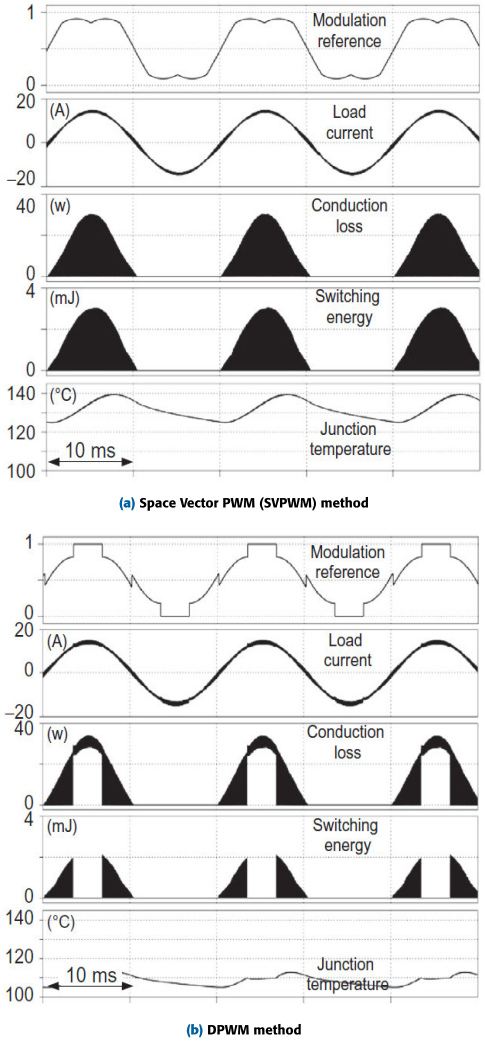


FIGURE 37. The 2L-VSC converter: power loss and junction temperature measurements [32].

The DPWM is not restricted to the use of 2L-VSCs. Multi-level converters can also be applied for this end [118]. Reference [116] presents a case study on a 3L-NPC converter,

in which some various DPWM methods based on optimal zero sequence injection PWM (OPT-ZSSPWM), such as conventional 60° DPWM (CONV-60° DPWM) [27], and alternative 60° DPWM (ALT-60° DPWM) [119], are discussed. It was concluded in [116] that using CONV-60° DPWM and ALT-60° DPWM can significantly reduce the thermal stress on the overheated PSD in the converter [116].

2) MODULATION WITH CONDUCTION LOSS REDISTRIBUTION

Another approach to modifying the thermal loading is conduction loss, particularly when it comes to switching redundancy like the 3L-NPC converter, as shown in Figure 33 [116]. In a 3-phase converter system with a typical star connection, introducing a common-mode offset to the voltage references does not impact the current. However, it will alter the distribution of conduction loss among the PSDs. The space vector diagram (SVD) of the 3L-NPC converter, as depicted in Figure 38, indicates that all vectors located within the inner hex possess switching redundancies. This provides greater control flexibility to adjust the current paths flowing through the PSDs for better LVRT capability.

A wide variety of modified and optimized thermal modulation methods are represented in [48], [49], and [120]. Figure 39 displays the space vector modulation (SVM) method over one switching period. In this figure, the state vector 1-1-1 is removed, meaning that the converter state's time is declined when current flows via the clamped diode and associated switch. Figure 40 depicts the outcomes of the PSD's temperature in the converter under an extreme LVRT process. The results indicate that an optimized or modified modulation sequence leads to more symmetrical thermal loading and decreased thermal stress on the most stressed PSDs during LVRT.

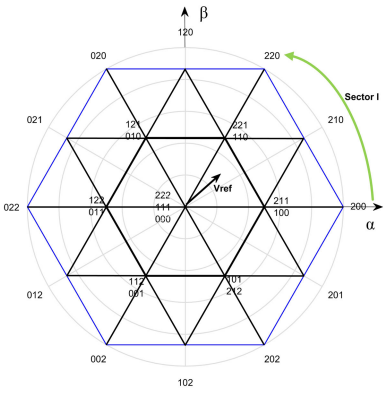


FIGURE 38. Switching redundancies in the 3L-NPC converter [32].

B. ATC AT SYSTEM FUNCTION LEVEL

To maintain the desired energy conversion level, this thermal management level is solely suitable for a limited number of power converters, as shown in Figure 41 [32]. Thermal controlling can be attained by recirculating parallel power converters' active and reactive power. Regardless of some drawbacks, such as higher losses in some overloaded power converters, it is not confirmed whether controlling the PSDs' losses and temperatures in one of the parallel converters is feasible.

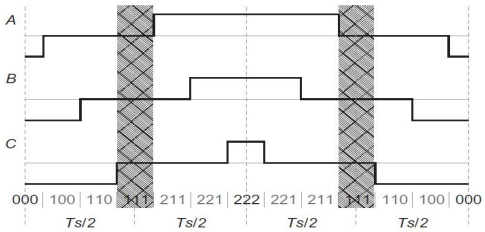


FIGURE 39. Modified modulation sequence for higher device temperature during LVRT [32].

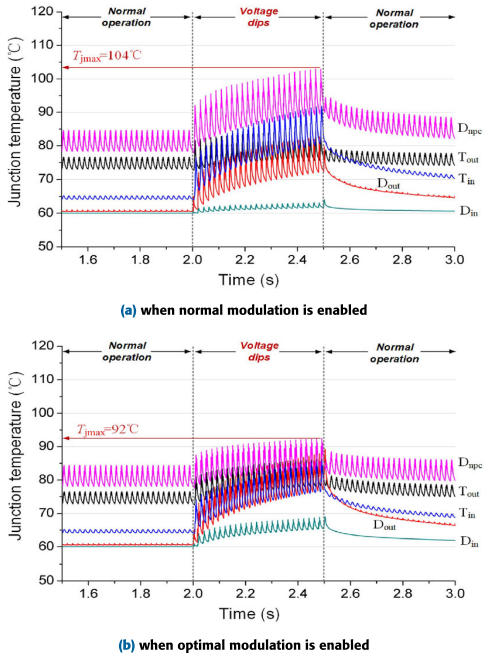


FIGURE 40. PSDs' temperatures in the 3L-NPC converter under LVRT [48].

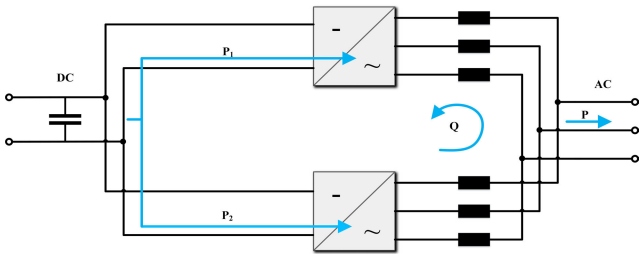


FIGURE 41. Active/reactive power routing to balance thermal stress among converters [32].

1) ATC BY REACTIVE POWER

The amount of reactive power a converter can provide is not necessarily limited to the power at the converter's input. It can

significantly affect the loading of elements, so it is an amp approach to reach the ATC for enhanced reliability. Figure 42, presented in [31], illustrates the impact of varying reactive power on the loss distribution of the same 3L-NPC converter. The figure shows that reactive power modifies the phase angle between the voltage and current of the output and alters the PSDs' current amplitudes. Furthermore, the reactive power delivered to the power network is closely connected to its power stability and voltage level, particularly when it comes to weak grids with restricted power capacity [121], [122], [123], [124], [125]. Consequently, many grid codes have been established to restrict the amount of reactive power injected by power converters. The mentioned codes can markedly restrict the thermal control capability that can be achieved by utilizing the converter's reactive power.

Figure 43 depicts a doubly-fed induction generator (DFIG) wind turbine system. The DFIG structure allows for the support of reactive power from either the stator side or the grid side converter (GSC) [126], [127]. So, the reactive power that is being distributed among the DFIG system is controllable. Figure 43 shows that the amount of reactive power injected into the power grid remains constant, thereby significantly extending the applicable reactive power for controlling device temperature, regardless of grid codes. However, certain restrictions, such as over-modulation, the current capacity of the PSDs, and DFIG, must also be considered when implementing this control approach [126]. If there are increases in the wind speed, these sudden changes in adverse thermal cycling in the converter. Hence, an appropriate reactive power control scheme in a DFIG system can regulate the swings of junction temperature under such circumstances. Figure 44 illustrates the basic control diagram for this approach [126]. The IEC 61400-1:2019 defines a standard wind gust with a one-year return period. The thermal cycling of power converters with/without thermal reactive power control is shown in Figures 45a and 45b, respectively. Based on Figure 45a, the thermal stress is least severe at a synchronous wind speed due to the lack of active power in the GSC and most severe in the rotor side converter (RSC) due to the small fundamental frequency of the rotor current. The maximum junction temperature fluctuation in the GSC declines from 11°C to 7°C with extra reactive power, as displayed in Figure 45b. However, this fluctuation remains the same at 18°C in the RSC.

Likewise, controlling the PSD's temperature by reactive power is attainable in a parallel converter-based wind system with several converters (see Figure 46). Here, the converter is required to control thrice more power than the wind system depicted in Figure 43, but with the exact generator capacity. To cope with this, parallel converters are generally used, which allow for temperature control of the PSDs by distributing reactive power within the converters [31]. The results are shown in Figure 47 where it can be observed that the temperature swings of the overheated PSD can be significantly decreased, from 32°C to 12°C.

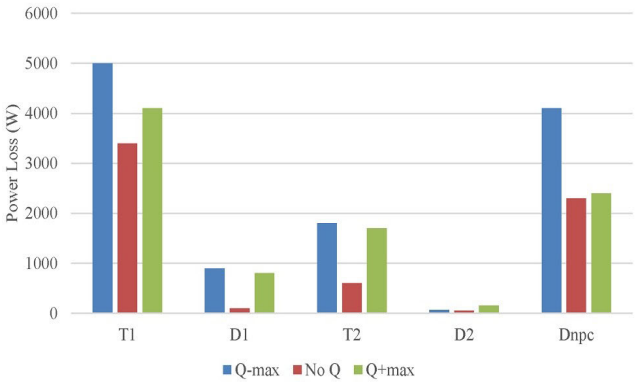


FIGURE 42. Distribution of losses in the 3L-NPC converter based on various reactive power values [31].

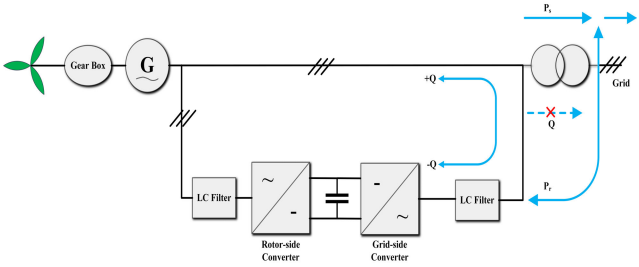


FIGURE 43. Junction temperature regulation in the power converter of a DFIG wind turbine system by implementing reactive power control [126].

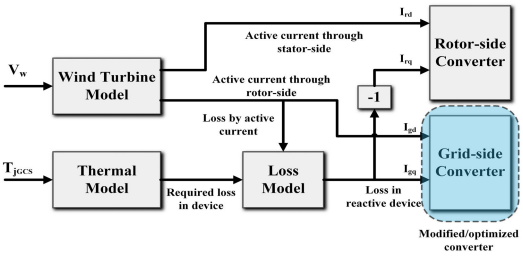
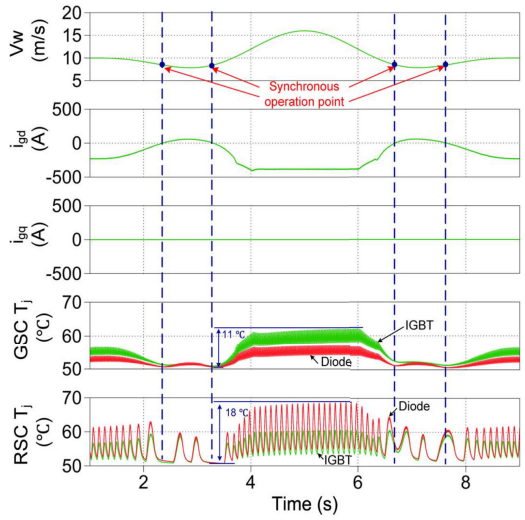


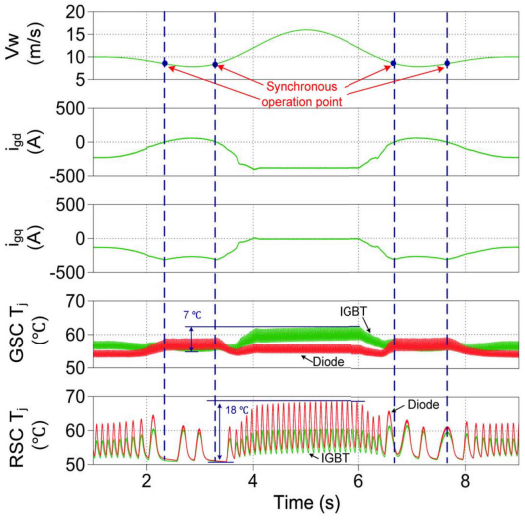
FIGURE 44. Thermal control diagram of the converters in the DFIG system [126].

2) ATC BY ENERGY STORAGE OR ACTIVE POWER

The power converter's current magnitude is significantly influenced by the active power, affecting the power semiconductor devices' loss and thermal loading. Unlike reactive power, controlling the available active power in the converter is generally not feasible. However, an energy storage system (ESS) can be used as an additional source of active power [128], thereby enabling this control function. The ESS can be located in the DC-link, as shown in Figure 48, to reduce thermal excursions in the grid-side converter and instabilities in power injected into the grid. However, some challenges associated with using ESS include determining the type of energy storage technology, sizing the ESS appropriately, and evaluating the thermal enhancement provided by the ESS. The ESS comprises an energy storage device (ESD)



(a) when reactive power control is not enabled



(b) when reactive power control is enabled

FIGURE 45. Thermal cycling of the back-to-back power converters in the DFIG system during abrupt wind speed changes [126].

and a bidirectional power converter. Figure 48 illustrates the power control method for the ESS [128]. Initially, the wind turbine's power production is calculated. Then a high-pass filter is used to obtain short-term power variations that serve as a reference for the ESS's charging power. This helps smooth out the power flow in the GSC and offers independence in controlling the wind power converter from the ESS.

Figures 49a and 49b show the power and temperature characteristics of the power converter when combined with the ESS, respectively. Case 1 has P = 0.05 MW, E = 270 kWh, and the weight is 1.7 t Li-ion. Case 2 has P = 0.177 MW, E = 6.25 kWh, and the weights are 1.25 t Ultracapacitor and 0.12 t Li-ion. Case 3 has P = 0.200 MW, E = 2.6 kWh, and the weight is 0.52 t Li-ion. As per this figure, the power is smoothed with the help of the ESS. Thus, the thermal fluctuation is decreased. What is more, the temperature gets smoother as the ESS becomes larger [128].

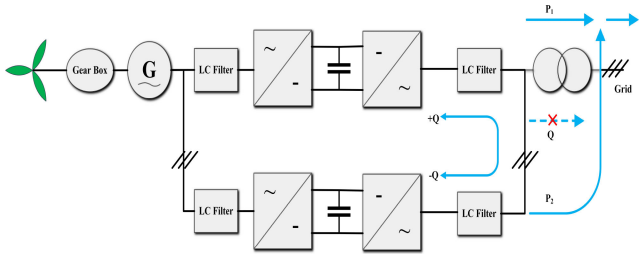
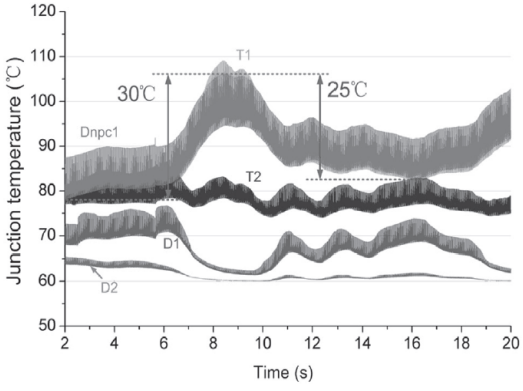
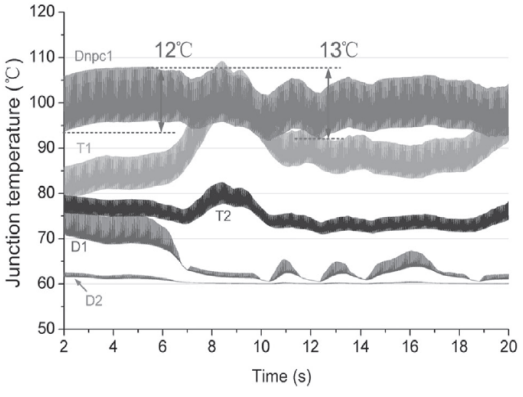


FIGURE 46. Reactive power distributing between parallel converters in a wind turbine system [31].



(a) when reactive power control is not enabled



(b) when reactive power control is enabled

FIGURE 47. PSDs' temperatures of the 3L-NPC converter with paralleled converters during abrupt wind speed changes in the DFIG system [126].

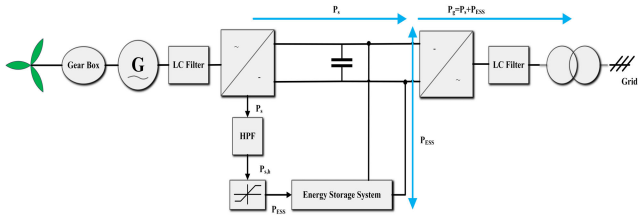


FIGURE 48. Junction temperature control with the integration of ESS and back-to-back converters in the DFIG system [128].

C. ATC AT OTHER LEVELS

Over the years, other techniques have also been developed for the ATC of power converters. Active gate control is one such technique that can regulate the losses of PSDs without

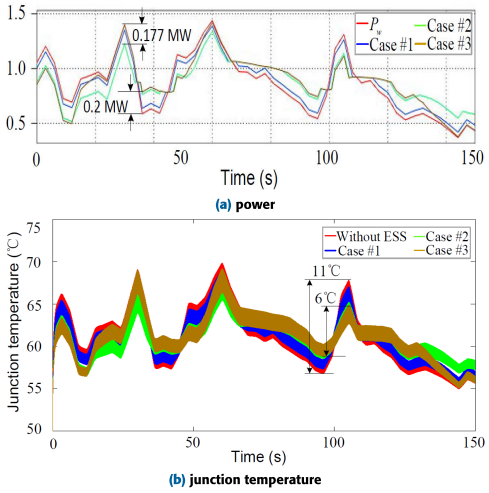


FIGURE 49. The GSC as per various energy storage capabilities [128].

affecting their functionality. Adjusting the gate drive voltage allows both losses (conduction and switching) of the PSDs to decline, thereby reducing the thermal cycling magnitude [30]. For example, an active gate driver has been proposed in the literature to compensate for variations in the on-state resistance of IGBTs [129]. A different active gate control has been used to balance currents among parallel-connected IGBTs [130]. Modifying the control parameters of active gate control can also reduce the thermal cycling in the PSDs.

Changing the switching frequency is another effective solution for managing the thermal behavior of power devices. As seen in previous studies, this can be achieved through linear or hysteresis control [26], [27], [28]. The ATCs used in these studies have lowered the switching frequency compared to the uncontrolled system, albeit with an increase in the current ripple [27], [28].

One approach to managing thermal behavior is to vary the modulation index using the DC-link voltage, which affects the loss distribution between IGBTs and diodes [32]. Another method is presented in [27], where a dynamic current limitation is set to prevent overheating and potential damage to the PSD. This allows for low-power operation of nearly overheated systems. In MMCs, specific submodules are subjected to higher thermal stress than others. An algorithm is suggested in [131] to balance MMC submodules' junction temperatures.

It bears noting that almost all ATC methods discussed in the literature are open-loop and do not rely on temperature feedback from the device. This is primarily because temperature measurement within PSDs is not straightforward in real-world applications such as AESs, where high power densities are involved. The thermal model-based estimation is a potential solution, but it heavily depends on accurate models for losses and the thermal behavior of the converter. These models are still not advanced enough to protect the converter's intricate functioning conditions, power device packaging technologies, and cooling methods. Therefore, they remain areas of active research.

Table 3 summarizes the most important ATC methods based on various control levels.

IV. DISCUSSION, CHALLENGES, AND SCOPE OF FUTURE WORK IN AES POWER SYSTEMS

Several studies have explored open-loop thermal loading controls that do not rely on the device's temperature feedback. This is because measuring a PSD's temperature during the process is challenging, particularly in high-power-density applications such as AES power systems. One potential solution is to use thermal models to predict PSD's temperature, but this method heavily relies on the converter's loss and thermal models' precision. These areas are currently the subject of extensive research as existing models are not yet advanced enough to fully account for the complex operating conditions of the converter, packaging technologies, and cooling requirements and procedures.

Since this work focuses on ATC methods of power electronics converters specifically for AES power systems, this section will first discuss and compare various high-voltage power converters (e.g., multilevel and modular converters) which shape the concept of power electronics building blocks (PEBB) in AES power system applications. It is worth pointing out that although the thermal management issue may initially appear simple, considering the moderate heat generation and available surface area for heat dissipation on each PEBB, there are two challenging constraints to overcome. Firstly, direct liquid cooling is impossible for PEBBs, meaning liquid connections cannot be established. Secondly, the PEBBs must be easily replaceable by the ship's crew while the ship is underway, requiring them to be compact, lightweight, and resistant to physical damage. A large finned air-to-air heat exchanger is out of the question. These constraints pose a significant challenge in transferring heat from the PEBBs to the corridor, as these limitations render many existing electronics cooling technologies ineffective.

Then this section will explain how the ATC methods reviewed so far can be applied and improved in the PEBBs concept for AES power systems. Next, future research opportunities in the ATC methods will be presented because they are pivotal to considering other possible scenarios for future design.

A. THERMAL CONTROL OF PEBBS CONCEPT

Newly emerging materials, components, and system concepts; such as wide bandgap (WBG) materials, silicon carbide (SiC) based PSDs, PEBBs, and integrated power systems; have been, are, and will continue to enable future marine systems as different from today's systems as steamships were to sailing ships [132]. Shipboard electric power systems benefit from the progress made in power converters, which are supported by many different elements, subsystems, and system technologies [133]. One notable technology is the PEBB, which was initially conceptualized and proposed

TABLE 3. Summary of important ATC methods based on control levels.

Control Level	ATC Method	Advantages/Highlights	Disadvantages/Comments
Modulation Level	Switching loss reduction [110] - [116]	Enhanced PWM techniques minimize switching losses but may increase current ripples.	Each method has drawbacks and cannot simultaneously improve all requirements, e.g., lower switching counts result in higher current ripple.
	Conduction loss redistribution [48] - [49], [120]	Conduction loss redistribution in the 3L-NPC converter addresses switching redundancy through voltage reference adjustments.	Conduction loss redistribution may increase harmonics.
System Function Level	Reactive power [31], [121] - [126]	Reactive power control affects loading and loss distribution. In DFIG wind turbine systems, regulating reactive power injection controls junction temperature swings and thermal stress in PSDs.	Reactive power-based controls for junction temperature stabilization are impacted by wind gust conditions, wind configurations, and grid code requirements.
	ESS or active power [128]	Active power affects losses and thermal stress. ESS, as an extra power source in the DC-link, reduces thermal excursions and instabilities.	High-power applications, like AES power systems, have high ESS costs. Integrating ESS and active power control may reduce ESS costs.
Other Levels	Active gate control [30], [129] - [130]	By adjusting gate drive voltage, losses can be regulated without impacting functionality, compensating for variations in on-state resistance and balancing currents among parallel IGBTs.	Thermal-related measurement is challenging, especially in AES power systems with high power density.
	Varying switching frequency [27] - [28]	Modifying switching frequency with linear or hysteresis control effectively manages thermal behavior.	Changing switching frequency may increase current ripple.
	Varying modulation index [32]	Modulating DC-link voltage impacts loss distribution between IGBTs and diodes.	Not applicable universally, only feasible with a converter-fed dc-link, which limits its applicability.
	Submodule junction temperature balancing [131]	The proposed algorithm equalizes junction temperatures within MMCs by addressing elevated thermal stress in specific submodules.	Harmonic study can also be considered.

by the US Office of Naval Research (ONR) in 1998 as a means of enhancing the availability, performance, and cost-effectiveness of converters in future AESs [134], [135]. Implementing the PEBB concept has dramatically impacted the innovation, manufacturing, commissioning, and operation of converters in AES applications [136].

Similar to Figure 35 in which different control layers for managing the thermal behavior of single converters were highlighted, one must understand the control layers of the PEBBs concept to control the thermal behavior of high-voltage power converters in large-scale applications such as AES power systems. These layers are shown in Figure 50 [136]. Figure 51 depicts an AES power system composed of several power electronics converters [137], which has become bigger and more complicated. In this regard, various advancements, including grid configuration and topology, voltage stability analysis, power quality, fault detection, and protection, have been made [138], [139]. To advance thermal management, power ratings, cost-effectiveness, availability, and total performance, various cutting-edge topologies over traditional VSCs have been presented. Some of them have already been implemented in the AESs.

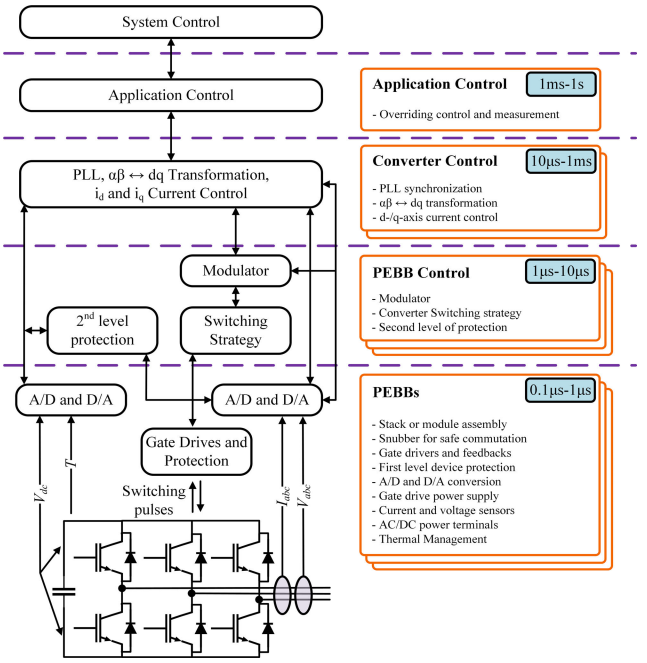


FIGURE 50. Control hierarchy in PEBBs concept [136].

1) MULTI-LEVEL CONVERTERS (MLC)

Unlike the basic VSC, MLCs are power converters that generate AC voltages using more than two DC voltage levels. MLCs offer various benefits, including reduced AC ripple, lower voltage stress on both the PSDs and loads, and a higher effective switching frequency. A great variety of MLCs, such as the NPC multi-level converters (NPC-MLC), the flying capacitor multi-level converters (FC-MLC), the CHB multi-level converters (CHB-MLC), and MMCs have been recently presented [140], [141], [142]. The NPC-MLC is advantageous in terms of high-power density since it has minimal

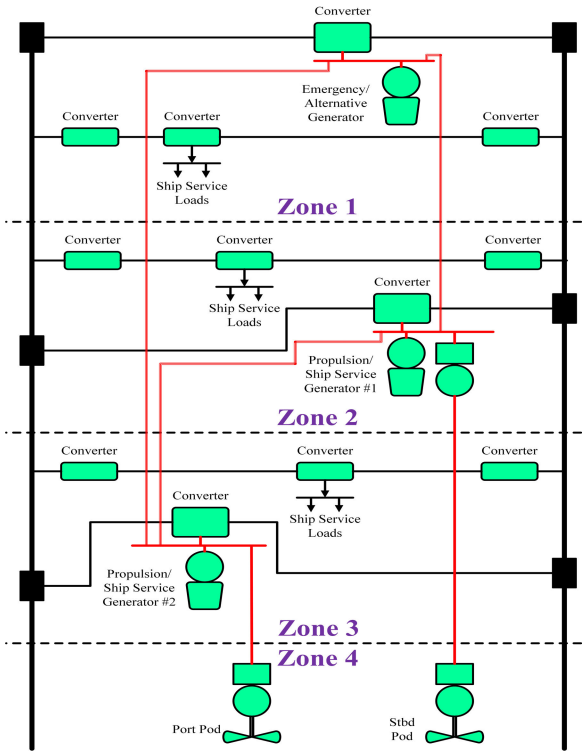


FIGURE 51. An AES power system with zonal distribution (podded propulsors) [137].

needs for passive components. On the other hand, CHBs and MMCs have modular structures, offer FRT capability, utilize low-voltage PSDs, and possess high efficiency and low quantization on the voltage and current. Still, they require many capacitors and have lower power densities. A thorough study of MLCs and their implementation in various fields, including renewable energy systems, EVs, and charging stations, has been conducted in a comprehensive review published in [143]. The work showed that MLCs offer lower THD values, lower distortion in input current, and lower switching frequency, thereby lower switching losses. On the flip side, having many components results in lower reliability, higher cost, and more complicated controllers.

The authors in [71] presented an ATC method of hybrid MMC under overmodulation operation. The ATC was introduced for half-/full-bridge submodules. Two kinds of bypassed switching modes were modified in full-bridge submodules to produce a symmetrical switching arrangement when the leg voltage was positive. The same procedure is applied when the voltage of the leg is negative. While the power loss distribution in full-bridge submodules is more balanced, the symmetrical switching arrangement does not negatively affect the performance, decreasing thermal stress on the most highly stressed devices. Reference [144] proposed an implementation of the NPC-MLC based on a switching-cell array method, adding redundant conduction paths on one side and more options to distribute the switching losses on the other. This way, the converters' temperature distribution is balanced, reducing thermal stress and improving reliability.

Reference [69] presents an approach to incorporate the junction temperature into the capacitor voltage balancing algorithm, called nearest level modulation (NLM), to achieve uniform thermal distribution among the submodules. Unlike the research in [67], the temperature of the devices within the submodule is combined individually with the dedicated capacitor voltage, resulting in different distinct cost functions for the upper/lower IGBTs and upper/lower diodes. The appropriate cost function is chosen for each sampling instant, considering the current direction in each leg and the need to either insert or bypass submodules. The outcomes indicated that the suggested approach significantly reduced the inconsistency and temperature dispersion among the submodules.

A quasi-two-level FC-MLC for PEBBs was presented in [145]. the results showed that the temperature distribution and the measured heat sink temperature are both improved.

2) MULTI-PHASE CONVERTERS

AES power systems typically utilize power converters that have a 3-phase input or output topology. However, using multi-phase motors with more than three phases can improve propulsion motors' power ratings and FRT capability. In addition to providing modularity and redundancy in the structure, using multi-phase converters can also result in lower common mode voltages, which is advantageous for motors and reduces the need for filters. Reference [147] discussed the modeling and control of VSCs associated with different multi-phase power electronics converter topologies, primarily deployed in multi-phase electrical machines. For instance, multi-phase converters play a crucial role in marine applications, where FRT capability, efficiency, and noise are the pressing issues [148]. Reference [149] studied the progress of modern AESs in terms of propulsion drive motors, such as PMSMs, induction machines (IMs), high-temperature superconducting synchronous machines (HTSSMs), and superconducting homopolar DC machines (SHDCMs).

3) SOFT-SWITCHED CONVERTERS

DC/DC power converters usually have resonant features that enable zero-voltage switching (ZVS) or zero-current switching (ZCS) to decrease switching losses and increase the switching frequency. Some soft-switching topologies for 3P AC power converters have been proposed by incorporating auxiliary circuits like 2L-VSCs, 3L-NPCs, and active neutral-point-clamped (ANPC) converters [150]. However, despite the advantages of each topology, soft-switched converters have not been widely adopted in practical applications due to the added complexity, cost, and restricted benefits for drives, where high switching frequencies and fast dynamics are not necessary. A soft switching converter for AESs has been proposed and experimentally verified in [151] and [152], respectively. The proposed converter offers high power density and efficiency, minimizing switching power losses.

TABLE 4. Advantages and disadvantages of different VSC configurations [140], [146].

Configuration	Advantages	Disadvantages
NPC-MLC	• Modularity in structure • Simplicity in structure • Good dynamic response • Less required DC sources • Good FRT capability • Lack of floating capacitors • Balanced switches' blocking voltage	• Having restricted DC-link voltage balance to the 3L configuration • The higher the voltage level, the higher the clamping diodes are required • Unbalanced distribution of losses • Inexpensive • The higher the clamping diodes, the lower the reliability
FC-MLC	• Modularity in structure • Good FRT capability • Low required DC sources • Lack of clamping diodes • Low voltage stress across the switches • The higher the voltage level, the more efficient it is	• Inexpensive due to the capacitors, as opposed to the diodes • Complicated voltage balancing • Limited efficiency • Complicated structure • The higher the capacitors, the lower the reliability • Use of more voltage sensors • Higher harmonics at low switching frequency rates
ANPC-MLC	• Balanced distribution of losses • Good dynamic response • Simplicity in structure • Expandability by flying capacitors	• Higher floating capacitors for levels higher than 3L configuration • Complicated control, as opposed to NPC configuration • Series switches are needed to operate higher voltage levels
CHB-MLC	• Modularity in structure • Simplicity in structure • Good FRT capability • Expandability • Lack of floating capacitors • Straightforward control circuit • Low voltage/current harmonics, so no filter is required • High reliability	• Required more switches • Inexpensive • More DC sources are required • Increased volume due to isolated transformers • Complicated control circuit • Higher number of sensors
MMC	• Modularity in structure • Scalability by cascading similar submodules • Simplicity in structure • Considerable FRT capability • Low losses • Minimized modularity level at the submodules • Low switching frequency • Low quantization on voltage/current (low harmonics) • No filter is required • High reliability • High efficiency	• Complicated data acquisition and interface between submodules • High number of capacitors and submodules, so it can be inexpensive depending on the application • Control circuits are required to balance the current and voltage of submodules • Higher number of sensors

Reference [153] presented an impedance-source inverter rather than traditional VSCs for ship systems. The results showed that the proposed configuration offers lower voltage stress on the elements and higher reliability.

Table 4 summarizes the most used MLC topologies and their advantages and disadvantages. Figures 52a, 52b, 52c, 52d, and 52e illustrate the leg schematic of various MLC configurations such as NPC-MLC, FC-MLC, ANPC-MLC, CHB-MLC, and MMC, respectively.

4) PEBBS CONCEPT

ONR introduced the concept of PEBB in the mid-1990s to tackle the issues related to power electronics converters, such as cost, availability, design, and operation intricacy. According to [137], the PEBB is a method of building power electronics that uses a standardized approach with modules that can be readily configured to satisfy different applications' specific hardware/software requirements. It includes various blocks such as power processors for single or multiple phases, gate drives, sensors, signal converters for sensors, switching or gate drive control blocks, and communication blocks for interacting with controllers and with one another.

The PEBB concept seeks to enable dramatic enhancements in the performance, reliability, and cost-effectiveness of electric energy processing systems by developing an approach to the creation and manufacturing of power electronics systems based on the integration of a set of building blocks with (1) integrated functionality, (2) standardized interfaces, (3) suitability for automated manufacturing and mass production, and (4) application versatility [154]. As mentioned in [137], "each PEBB includes built-in self-protection against voltage surges, overvoltage and undervoltage, fault currents, ground currents, internal faults, overloads, and overtemperature." The PEBB concept is designed to include standard interfaces, modularity, and integrated functionalities to enhance power electronics converters' performance, reliability, and cost-effectiveness. AES power converters have power ratings ranging from tens to hundreds of kilowatts at low

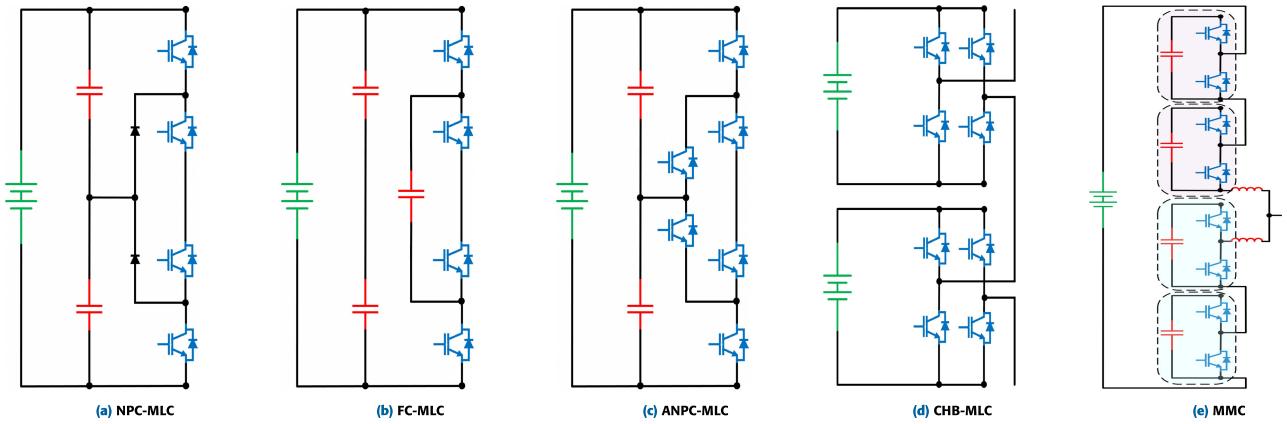


FIGURE 52. Leg schematic of different MLC configurations [140], [146].

voltages (<1 kV) to tens of megawatts at medium voltages (1 kV < & <13.8 kV), as shown in Figure 51. The PEBB approach is used in industrial power converters and is well-suited for AES and other ship systems. Using PEBB modules can simplify the development of power converters for various complicated applications.

Despite their high power-conversion efficiency, the heat dissipated by these PEBBs poses serious thermal challenges, meaning that the thermal aspects of the PEBBs concept in AESs deserve more intense scrutiny to complement the improved electrical performance by providing proper cooling in all conceivable scenarios. Traditional PEBB cooling strategies include heat sinks, direct liquid cooling, and heat pipes. Reference [155] presented an in-depth review of traditional and recent electronic cooling techniques applicable to PEBBs. Nonetheless, the design requirements and limitations imposed on the PEBBs concept in AESs, particularly in pursuit of shipboard power corridor [156] to which the PEBBs may be allotted, can place limitations on the application of conventional cooling methods. The power corridor's concept presents extra design constraints like compactness for the PEBBs. Many cooling strategies apply to the shipboard PEBBs, such as PEBB 1000 and PEBB 6000 [157].

A high-power 57.6 kW PEBB with 1.2 kV DC-link and 1.7 kV SiC MOSFET modules is presented in [158] in which the selection of DC-link capacitors is proposed to control the thermal behavior of the PEBBs concept. The results showed that the temperature rise of SiC modules was low. Reference [159] proposed a dynamic electro-thermal approach through an iterative algorithm for the PEBB concept. The proposed approach improved the power loss distribution model, which has temperature-dependent self-improvement ability and an effective thermal model providing a fast temperature calculation.

Depending on failures and the effectiveness of ATC methods, the PEBB stacks are prone to degrade due to aging and environmental stresses. Therefore, degradation is inevitable. To avert this, the lifetime of the PEBB must be assessed so that maintenance works can be planned ahead. Reference [160] proposed a component stress study to estimate the RUL of the PEBB. Reference [161] presented the concept of a standardized switching cell as an additional building block in converter optimization procedures. It is based on modeling a half-bridge arrangement to improve efficiency, volume, and thermal performance.

In [162], the authors tested and simulated 10 kV, 120 A all SiC half-bridge modules for use in a 4 kV, 100 A PEBB. In [163], an Impedance Measurement Unit (IMU) for 1 kVDC/800 VAC systems with an impedance measurement range from 10 Hz to 1 kHz has been proposed. The IMU remarks a reconfigurable, modular, and scalable structure capable of shunting current and series voltage injection mode. The core control of the perturbation injection unit was applied as per a distributed control scheme. The IMU is built with PEBB units and uses 1.7 kV SiC metal oxide semiconductor field effect transistor (MOSFET) modules. Reference [164] describes the development, manufacturing, and preliminary testing of a 1.7 kV SiC switching cell intended for use in a 250 kW integrated PEBB (iPEBB). In [165], a full-bridge PEBB was produced, which includes all ancillary circuits. The individual PEBB is rated for 6 kV operation, but the insulation design of critical systems allows a common mode voltage of up to 30 kV in an MMC. Similarly, a rapid PEBB thermal management tool, vemPEBB, has been proposed in [166] to tailor multi-fidelity PEBB modeling within the set-based design framework. An isolated gate drive power supply for a 5 kV full bridge PEBB consisting of 4 Austin SuperMOS devices has been developed in [167].

PEBBs concept is a practical solution in developing AES power systems with improved reliability, modularity, scalability, FRT capability, lower production, and lower maintenance costs. Figure 53a represents the open plug-and-play architecture of the PEBB concept that can be seamlessly integrated into various applications and automatically configure all its operational settings, eliminating the need for

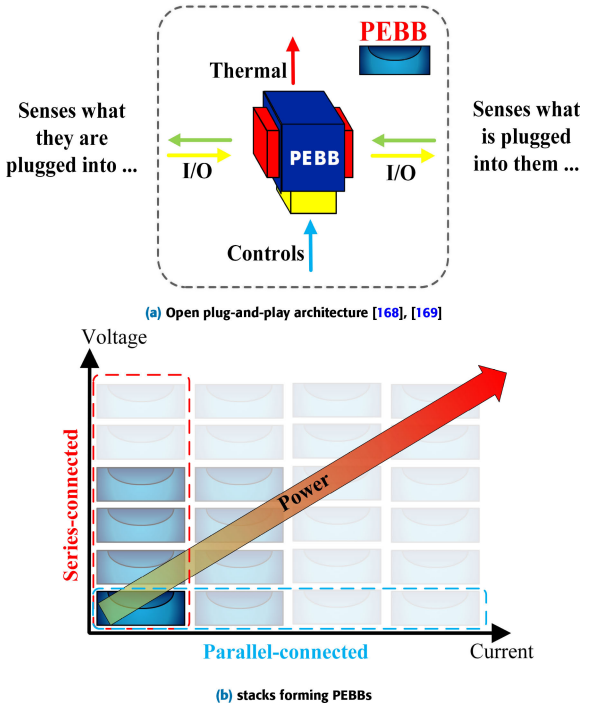


FIGURE 53. PEBBs concept.

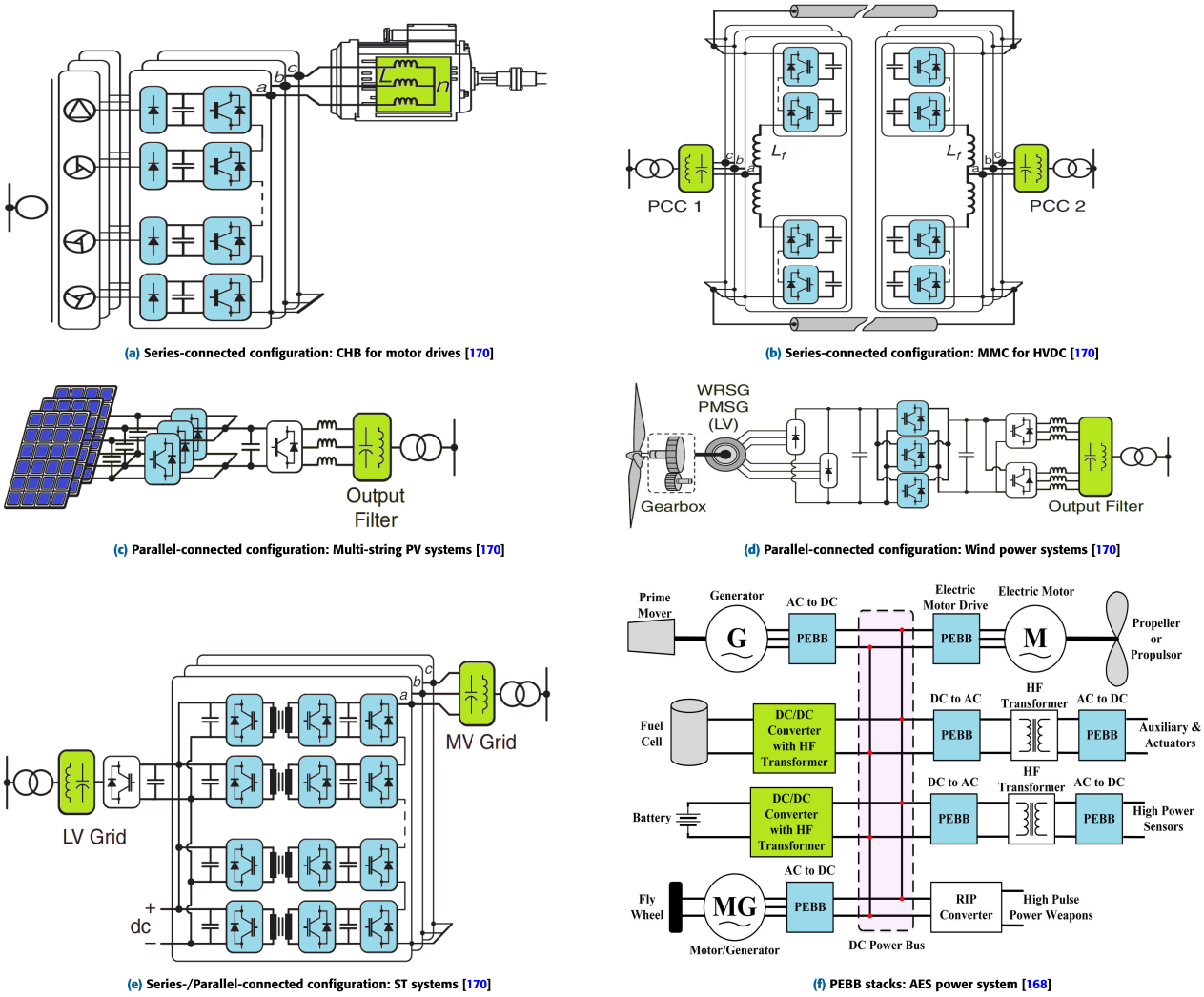
manual adjustments. When the PEBB is plugged into, the host application would immediately detect its presence, specify the producer, and initiate the automatic operation. Each power processing unit within the PEBB would independently control its own parameters for safe operation. The PEBB can be utilized in various applications using standardized interfaces and protocols. These characteristics contribute to cost reduction in defense and commercial sectors [168], [169]. Also, as depicted in Figure 53b, the PEBBs concept offers power converter configurations as modular systems shaped by many submodules connected in series, parallel, or series/parallel [168]. Figure 54 shows some state-of-the-art modular converter configurations based on PEBBs as follows: Series-connected configurations such as CHB for motor drives and MMC for High-Voltage Direct Current (HVDC) systems, parallel-connected configurations such as multi-string PV systems and wind power systems, and series/parallel configuration such as ST systems, and most importantly, AES power systems, as illustrated in Figures 54a, 54b, 54c, 54d, 54e, and 54f, respectively. Plus, Table 5 provides a summary of future opportunities for ATC in different PEBB applications.

B. COMMUNICATION PROTOCOLS OF PEBBS

One important aspect of ATC in PEBBs concept is the communication protocols with which the data is transferred between PEBBs. This can play an even more critical role in the ATC if the thermal-related data can be communicated faster and more precisely. As discussed previously, the most efficient type of PSD is the SiC which increases the switching frequency to around 10-20 kHz. Thus, a short cycle time in the microsecond range is vital. This stresses the growing need for a high-speed data transmission communication protocol. Over the years, various communication protocols for power electronics converters have been proposed [171], [172], [173]. The author in [174] established the primary criterion for communication in power electronics converters: simplicity, real-time communication, data rate, high-speed data transmission, data update cycles, synchronization, reliability and availability, redundancy, diagnostics, security, configuration, scalability, and reconfigurability.

PEBBs offer the plug-and-play architecture for various large-scale applications, providing a network with primary/secondary infrastructure. Several communication protocols have been proposed over the years [171], the important ones are controller area network (CAN) [175], serial real-time communications system (SERCOS) [176], motion and control ring optical (MACRO) [177], [178], [179], which is also an Ethernet communication protocol, MACRO and fiber distributed data interface (FDDI) to form power electronics system network (PESNet) [177], [180], PESNet 1.2 and 2.2 as the very two first communication protocols generated PEBBs [181], process field bus (PROFIBUS) [182], serial peripheral interface (SPI) [183], ethernet for control automation technology (EtherCAT) which interestingly most of the researchers have lately zeroed in on because of real-time capabilities, synchronization performance, fault diagnostics [184], process field net ssochronous real time (PROFINET IRT) [184], Ethernet PowerLink and Ethernet/IP [185], synchronous-converter-control-bus (SyCCo-Bus) [186], and RealSycho [187]. A good comparison between PESNet and SyCCo-Bus protocols has been presented in [188].

Some new communication protocols have been recently proposed, such as PESNet 3.0 [189]. In this paper, the comparison of the minimum cycle time between EtherCAT and PESNet 3.0 communication protocols has been drawn, and the results showed that, as opposed to EtherCAT, the inner-loop control bandwidth could be boosted in PESNet 3.0. In [190], a distributed communication and control system (DCCS) for high-frequency large-scale modular IMUs with tight synchronization and low latency has been presented for improving PEBBs' modularity and scalability. Reference [191] demonstrated a power converter structure that utilizes data transmission between nodes like gate drivers and sensors, enabling a more flexible and distributed control methodology. Reference [192] proposed PESNet 3.0 for high-power SiC MMCs in which the white rabbit network (WRN) is embedded in PESNet 3.0. For the first time, the WRN has been used in the power electronics in this paper, and the outcomes showed that it could remove the sync error (SE) restrictions of field-programmable gate array (FPGA).



(a) Series-connected configuration: CHB for motor drives [170]

(b) Series-connected configuration: MMC for HVDC [170]

(c) Parallel-connected configuration: Multi-string PV systems [170]

(d) Parallel-connected configuration: Wind power systems [170]

(e) Series-/Parallel-connected configuration: ST systems [170]

(f) PEBB stacks: AES power system [168]

FIGURE 54. State-of-the-art modular converter configurations using PEBBs concept.

TABLE 5. Future opportunities for ATC in different PEBB applications.

ATC Method	Motor Drives [32]	PV/Wind Systems [32]	STs [32]	AES Power Systems
Gate drive control	***	**	**	-
Switching frequency control	***	**	**	*
Modulation	**	**	**	***
DC-link voltage control	**	*	*	*
Reactive control	*	***	*	*
Active control	-	***	***	*
Profile shaping	-	***	***	**
Power routing	*	***	***	***

Note. ***: High, **: Medium, *: Low, -: No.

Moreover, some research has been carried out to provide wireless data transmission for communication [193]. Focusing on the PEBBs concept, [194] tests 5G/6G networks for PEBBs, and the results validated that the delay in data transfer can be enhanced by higher integration of the wireless communication module in the control board.

C. THERMAL DATA COLLECTION

A major difficulty in the ATC method is deriving thermal state variables, like the junction temperature. To this end, many solutions have recently been put forward that provide higher accuracy and broader bandwidth than traditional methods [195], [196], [197], [198], [199], [200]. Although

some of these solutions can address the issue to some extent, they are mostly inexpensive to implement and lack high signal-to-noise ratios and low sensitivity to external factors [200] and degradation [201]. Furthermore, temperature sensing is inadequate per se to have all the capabilities ATC can offer. The reason why is that the desired filter brings about phase lag. Although thermal predictors offer an affordable, locally resolved, and zero phase lag option for determining temperature, the model errors restrict their precision for complex calibration and degradation, which are not considered. Therefore, thermal observers graft the advantages of both solutions into one another by incorporating temperature sensor data into a closed-loop control system to reduce real-time model errors of the thermal estimator, as described in various studies including [27], [202], and [203].

D. STATE-OF-HEALTH (SOH) AND DEGRADATION

Many works have focused on degradation forecasting of distribution management systems, which include different types of EVs and batteries, to improve overall reliability by reducing the degradation rate of each component [204], [205], [206]. The operating condition of the components impacts the degradation process [207]. The degradation of the components results in decreased capacity, reducing the system's performance and increasing the reliability concern [208], [209]. The same concept of degradation analysis will be invaluable in power electronics converters since accurately predicting the SoH and the progression of damage is crucial for implementing thermal control in power converters for maintenance purposes. It is important to note that without sufficient data on the components' RULs, it is difficult or even incorrect to use power routing, which could ultimately reduce the system's reliability.

To create the modules' lifetime models, the thermal cycle's data, such as its damage, is gathered linearly [210], [211]. On the one hand, researchers have recently found that aging is non-linear. Therefore, they conducted experiments comparing newly manufactured power modules with pre-aged ones. The findings suggested that the new modules did not experience aging under identical thermal stress. On the other hand, the pre-aged modules showed a continued rise in thermal resistance related to aging. Based on the outcomes, a physics-based lifetime model was created [212]. It should be mentioned that the data creation for the feature of these lifetime models is not straightforward. Real-time power cycling data is essential for temperature-based lifetime models closely connected to various failure mechanisms. The models can only be generated by tracking plastic strain, which is a cause of damage to the modules, throughout a specific operating time. The research to obtain strain from modules needs further development [213], [214].

E. COST ANALYSIS

This technology raises significant concerns regarding the reliability of power electronics and the associated maintenance costs. The costs can be minimized by monitoring and controlling the lifespan of PSDs [263], [264]. However, addressing these challenges is not a simple task, as it requires understanding power device physics, effectively managing electrical variables, and developing optimal plans and schedules for maintenance.

To the best of the authors' knowledge, no comprehensive analysis has been conducted on the cost of power converters when employing ATC methods. While the literature emphasizes the cost reduction associated with these methods, no specific cost analysis or numerical comparison has been performed. An improved ATC method offers several advantages. Firstly, it enables the use of narrower safety margins, leading to enhanced reliability, increased availability, and, usually, cooler systems. Secondly, it reduces the expenses incurred from unscheduled maintenance. Unscheduled maintenance can result in lost revenue and system unavailability, which become critical factors as operational demands increase and financial resources are limited. Therefore, developing a cost-effective ATC method that considers the SoH and degradation of power converters is crucial to optimize maintenance costs [84].

From a cost reduction perspective in the context of the PEBB concept, adjusting the ATC of converter devices based on the thermal behavior of PEBB stacks is advantageous. This is because if a single PEBB fails, only a direct replacement is required to maintain proper power system operation. Implementing ATC and RUL methods facilitates this capability, allowing PEBBs to adapt their operation to align with scheduled maintenance, thereby increasing the cost-efficiency of planned maintenance tasks. Essentially, designing an effective ATC method with SoH and maintenance schedule will allow replacing system components when their failure probability reaches the maximum limit. This modification of ATC with SoH and RUL estimation will guarantee that the failure is always detected, simplifying maintenance scheduling and reducing associated costs [170].

In recent works [265] and [266], a comprehensive review was presented, highlighting the latest developments and emerging trends in technologies and approaches aimed at improving the dependability of power electronics systems. The authors discussed advancements across various levels, encompassing power electronics topology, control strategies, condition monitoring techniques, and digital-twin systems. They compared various FRT methods for full-bridge isolated DC/DC converters, including cost and number of elements.

F. REDUCING THE EFFECT ON THE OPERATION OF THE SYSTEM

The use of ATC methods offers an additional capability for PSDs and allows for altering the PWM frequency or system process to protect the PSDs from overtemperature damage. Although these methods have a negligible impact on system function under regular conditions, they can significantly

TABLE 6. Some important classifications and future outlooks to help ATC of PEBBs concept in AES power systems.

Criteria	Approaches	Future Work Perspectives
Enhancement in overload feature	- Decrease in power loss: • Frequency ([26], [27], [117], [215], [216], [217], [218]), • Peak current ([26], [27], [117], [219], [216], [220]), • Duty ratio ([215]), • Adjust current restriction to coolant temperature and frequency ([219]). - Increase in power loss: • Reduction in temperature swings ([221], [222]).	• Improving the reliability of operation close to thermal restrictions • Achieving a more reasonable difference between the maximum junction temperature throughout the operation and the nominal junction temperature • Enhancing the operation performance during transient at thermal restrictions
Decrease in thermal cycle	Manipulation in terms of the following: - Switching power loss: • Gate resistance ([210], [223], [224]), • Frequency ([27], [28], [45], [46], [216], [210], [225], [226], [227], [228], [229]), • Gate drivers ([32], [230], [222], [231], [232], [233], [234], [235]), • Shoot-through duty ratio ([233]). - Loading: • Reactive power flow ([31]), • Adjustment of current or voltage restriction ([32], [216], [225]), • Flux control of electric machines (minimized converter's loss) ([236]), • Optimized Maximum Power Point Tracking (MPPT) ([237]), • Optimized current for low-load applications ([238]). - Interface: • Cooling fan ([239]), • Liquid metal pump control ([240]), • Thermo-electric cooling control ([241]). - Modulation strategy control: • DPWM ([28], [32], [227], [242], [243]), • FCS-MPC ([51], [52], [244], [245], [246], [247], [248]).	• Lowering thermal cycles which bring about damages to PSDs • Enhancing the longevity of power electronics converters • Coming up with an optimum trade-off between reliability, availability, the lifetime of power converters, and PSDs' rating
Controlling thermal stress across PSDs	- Parallel PSDs: • Multi-chip modules ([249], [250], [251], [252], [253]), • Parallel power modules ([74], [75]). - Configurations: • Hybrid ANPC converter ([248]).	• Keeping an optimal distribution of thermal stress across PSDs • Monitoring the degradation and SoH of PSDs in ATC
Controlling thermal stress across PSDs in PEBBs	- Series PEBBs: • MMCs ([69], [71], [254], [255], [256], [257]), • CHB converters ([93]). - Parallel PEBBs: • Parallel ([32], [242], [258]), • Load sharing in microgrids ([259]), - Control of certain elements: • Power routing ([54], [56], [57], [77], [84], [89], [258], [260], [261]), - Redundancy concept: • Multi-phase power routing ([78], [105], [262]).	• Regulating the distribution of loading on various elements • Regulating RUL • Attaining optimal maintenance schedules

affect system operation when thermal limits are approached. All conditions must be considered to mitigate this effect, but protection against thermal damage stays reliable. The work presented in [219] is a good example. In this study, the maximum peak current of a traction inverter could be doubled to around 200% based on the operating point and not surpassing the maximum junction temperature. This was due to the decaying thermal impedance frequency response as the frequency went up.

G. PSD TECHNOLOGY AND PACKAGING

ATC methods are becoming increasingly vital in new PSD technologies and packaging. However, it also presents new challenges. WBG semiconductors such as SiC and gallium nitride (GaN) have smaller footprints and thicknesses than their silicon (Si) equivalents while keeping the same dielectric strength [267], [268]. This makes it possible to create more compact power electronic converters [269]. However, due to the smaller size of the PSDs, their thermal capacitance is lower, resulting in increased thermal/mechanical stress due to higher thermal cycling. This means that the lifetime of WBG-based power modules is more affected by thermal cycles than Si PSDs. Passive methods have been proposed to reduce the thermal cycling of WBG devices by using thermal buffers to increase adequate thermal capacity without degrading the thermal path [270]. As the method brings about a more complicated module packaging, the ATC is an effective method for the lifetime extension of WBG semiconductors [230], [271], [272], [273].

Although ATC using WBG devices has several advantages, there are significant challenges in obtaining accurate

measurement and high-bandwidth junction temperature data. With WBG semiconductors, various temperature-sensitive electrical parameters (TSEPs) that can be obtained from high bandwidth are not applicable in the same way as with Si devices or require a more intricate circuit for data collection. This issue has been discussed in several research papers, including [197], [198], [201], [274], and [275].

The ever-growing use of WBG semiconductors has revolutionized module packaging to improve the deployment of enhanced electrical features, unlike Si devices. Bond-wire-free transfer-molded power modules with lead frames are used to increase integration density, which can withstand higher thermal stress than soft silicone encapsulation modules. However, such modules still experience thermal cycling-induced aging effects, such as delamination of the chip from the lead frame and mold cracking [276], [277]. Recent solutions, such as board integration of PSDs, have been presented to decrease switch cell inductance and enhance system integration. Still, they can degrade the semiconductors' thermal path, leading to increased thermal cycling [278]. Hence, using ATC methods dramatically improves the reliability and lifetime of future packaging of WBGs.

Table 6 summarizes some hot research spots and radical challenges for future work.

V. CONCLUSION

The ATC method is used to improve the performance and reliability of a power converter by regulating its thermal behavior through control techniques. The main objective of the ATC techniques is to lower the average temperature and swing amplitude in PSDs. The main highlights of this paper are as follows:

1) The ATC methods in different converter configurations; such as single configurations (two-level, three-level, multilevel converters), parallel configurations, cascaded configurations, and modular configurations; have been reviewed, and a detailed comparison has been provided.
2) A brief overview of the most commonly used thermal networks and their comparison has been provided. The mathematical and theoretical principles of these networks deserve a separate review paper.
3) The ATC methods with the power routing approach have been presented. There are no papers related to power routing for single configurations because it does not apply to them. But many papers propose the optimal power distribution between modular power converters.
4) Different layers of thermal control based on various bandwidths have been discussed in detail. The layers include the modulation level (e.g., modulation with switching power loss reduction, modulation with conduction loss redistribution), the system function level (e.g., controlling reactive power, active power, or ESS), and other levels (e.g., active gate control, switching frequency, manipulation of the loss distribution between IGBTs and diodes). And a detailed comparison of different control layers has been provided.
5) Next, the PEBBs concept has been introduced and discussed. So far, various ATC methods have been presented based on control levels, configurations, and modulations. After that, the discussion continued with the PEBBs concept and the most important converter configurations to form PEBBs stacks, such as NPC-MLC, FC-MLC, ANPC-MLC, CHB-MLC, and the most important one, MMC. The MMC configuration is the best candidate for the PEBBs concept to meet AES power systems' requirements, such as modularity, scalability and simplicity in structure, hot-swapping, redundancy, low filter requirements, and lower quantization on current and voltage. The advantages and disadvantages of each one of these configurations in the PEBBs concept have been presented.
6) Having several MMCs for shaping PEBB stacks raises thermal stress. Hence, a precise yet cost-effective ATC method is very much needed to control the thermal behavior of the PEBBs concept. Since research has yet to be carried out on thermal control of the PEBBs concept, this paper tried to explain the whys and the wherefores of implementation of the ATC methods discussed in this paper to this concept. Also, the communication protocols that help the ATC methods in this concept have been briefly discussed, which must be improved for better data acquisition. This helps transfer thermal-related data of each PEBB stack, leading to better health monitoring.
7) Finally, a very detailed scope of future work is presented with categorized recent papers of different areas where improvements can/must be made in the PEBBs concept. Also, some future work perspectives, such as thermal data collection, state-of-health, degradation forecasting, cost analysis, PSD technology, PSD packaging, etc., have been proposed.

This work was investigated in a timely and comprehensive manner. It will serve as a comprehensive and useful reference for those who are working on controlling the thermal behavior of power converters and how these methods can be employed in different applications such as PEBBs concept in ship power systems, aircraft, motor drives, HVDC, wind power systems, multi-string PV systems, ST systems, etc.

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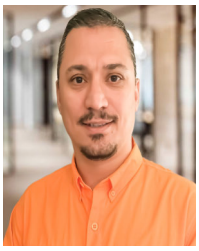

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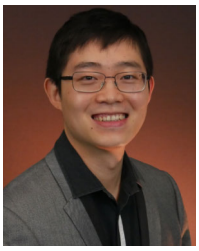

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