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Mitigating commutation failures in HVDC systems with SFCL deployment

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ABSTRACT

Commutation failures represent a prevalent issue encountered in line-commutated-converter high voltage direct current (LCC-HVDC) systems. As the widespread deployment of HVDC systems continues, the risk associated with commutation failures increases, posing a growing threat to power grids due to their potential to trigger severe consequences, including cascading failures and widespread blackouts. This research paper aims to address the significant issue of commutation failure within direct current (DC) systems through advocating for the use of resistive-type Superconducting Fault Current Limiters (R-SFCLs). To substantiate the efficacy of this proposed strategy, an array of simulations are executed using the PSCAD/EMTDC software. This comprehensive study investigates the performance characteristics of R-SFCLs configured with varying resistance values, scrutinizing their response under diverse fault resistance scenarios and distinct fault initiation times within the LCC-HVDC system. The outcomes of these simulations are that SFCLs confer significant advantages for mitigating commutation failures, surpassing traditional mitigation methods in terms of effectiveness. Consequently, SFCLs emerge as an optimal solution to prevent commutation failures in the HVDC systems.

1. Introduction

In the modern era, high-voltage direct current (HVDC) systems are rapidly expanding due to their cost-effectiveness, suitability for long-distance transmission, and the ability to connect unsynchronized networks. A key component of HVDC systems is the power converter, which switches between AC and DC. The two main types of converters used are Line Commutated Converters (LCC) and Voltage Source Converters (VSC). Most operational HVDC systems currently employ LCC with thyristor valves, a mature technology with low conversion losses. However, LCC-HVDC systems consume reactive power, require large filters, and may experience commutation failures. Commutation failures in HVDC inverters, often caused by AC voltage dips [1], can lead to power interruptions, equipment stress, and malfunctioning of protective relays [2–4]. Repetitive failures may even cause system shutdown [5].

To address this issue, various prevention methods have been researched in the past [6–10]. Traditionally three main approaches have been applied. One direct solution is to advance inverter firing angles when AC voltage dips are detected by control systems [11]. However, this approach has limitations, as control systems may not always respond quickly, and it may not be effective in certain situations, such as during commutation initiation or in the case of three-phase faults [12]. The second approach involves HVDC system controller modifications. A widely adopted method is the Voltage Dependent Current Order Limit (VDCOL) method, which safeguards HVDC systems by regulating current orders when AC or DC voltages fall below a specified threshold [13–15]. However, it cannot completely prevent commutation failures, especially when the fault is in close electrical proximity to the inverter [16,17]. The third solution involves the incorporation of additional components, with Capacitor-Commutated Converter HVDC (CCC-HVDC) being a common choice. CCC-HVDC inserts capacitors between thyristor valves and converter transformers to reduce reactive power consumption. This extends the extinction angle (γ), providing a greater margin for commutation. Nevertheless, CCC-HVDC subjects thyristor valves to significant voltage stress and shortens their operational lifespan [18–21].

The superconducting fault current limiter (SFCL) stands as a significant and practical application of high-temperature superconductors (HTS) [22]. Proposed initially in 1966, SFCLs have undergone continuous development. As of today, both HTS YBCO tapes and SFCL devices have achieved commercial maturity. Second-generation HTS YBCO tapes now boast a critical current of 510 A, a substantial increase from a decade ago [23]. SFCLs industrial projects have been developed globally and are operating reliably.

The distinctive attributes of SFCLs lie in their inherent HTS properties and engineering configuration, particularly its fault current limiting

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capabilities. Additionally, SFCLs show promise as a tool to prevent commutation failures, an area with limited research. Previous work, such as [24], qualitatively described the effects of resistive SFCL on commutation failure and demonstrated their effectiveness in enhancing HVDC system converter restoration. Furthermore, [25] revealed that flux-coupling-type SFCLs can reduce successive commutation failures and improve HVDC system fault recovery.

However, prior research failed to consider the resistance of SFCLs, fault initiation times, and fault resistance all at the same time. The simulation results presented herein demonstrate that an appropriately resistant SFCL can prevent commutation failures. The subsequent simulations prove that SFCLs can effectively mitigate commutation failures, regardless of the fault type or initiation time. Understanding the interplay between the resistance of SFCLs, fault initiation times, and fault resistance is crucial for ensuring the stability and reliability of power systems. By comprehensively considering these factors together, researchers and engineers can design SFCLs with appropriate resistance values, preventing commutation failures and ensuring seamless operation during various fault conditions. This holistic approach not only enhances the effectiveness of SFCLs in mitigating commutation failures but also paves the way for more robust power grid systems, reducing downtime, minimizing damage, and ultimately improving the overall resilience of electrical networks.

The paper is organized as follows: Section 2 introduces the fundamentals of commutation failure and SFCLs. Section 3 provides a quantitative analysis of the impact of SFCLs on commutation failure. This is followed by Section 4, which presents a case study on a monopolar HVDC system, offering practical insights and application of the theoretical concepts discussed earlier. Finally, the paper concludes with Section 5.

2. Fundamental concepts: Commutation failure and superconducting fault current limiters

2.1. Operating principles of LCC in HVDC systems

The firing angle (α) in power systems represents the phase angle at which a thyristor conducts, controlled by a gate signal. The extinction angle (γ) indicates when the charge generated during thyristor conduction is dissipated and is essential in commutation failure analysis.

Power converters often use a six-pulse Graetz bridge configuration, comprising six thyristor valves, as shown in Fig. 1. These valves conduct in pairs from the top and bottom rows, connecting AC phases with DC terminals. Proper commutation involves only two valves conducting simultaneously, resulting in a DC output voltage.

In practice, commutation has an overlap period defined by the overlap angle (μ) due to AC source inductance. The firing angle (α) influences the output DC voltage, allowing control over power transmission.

Understanding these concepts is crucial for analyzing commutation in power systems, where α, γ, and μ interplay to determine system behavior.

2.2. Commutation failure mechanism

In power systems, commutation failures in inverter thyristor valves can occur when the extinction angle (γ) is insufficient for the valve to regain its blocking capability. Thyristors, crucial components in power systems, possess inherent characteristics that can lead to unintended conduction. To ensure proper commutation, a reverse voltage must be applied to the valves for a specific duration, eliminating stored charge generated during forward conduction, and restoring the valve's blocking capability. This process, known as deionization, plays a critical role in successful commutation.

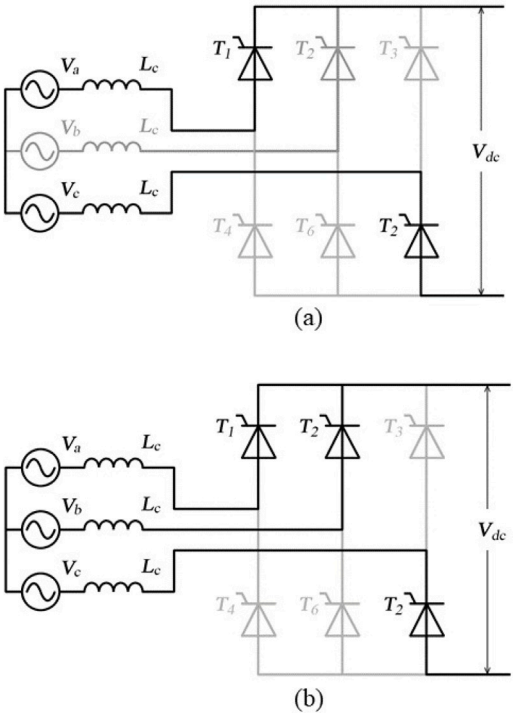

Fig. 1. (a) Ideal commutation process in Graetz bridge. (b) Practical commutation process in Graetz bridge.

In essence, a successful commutation process requires not only adequate time for commutation itself (as indicated by the commutation overlap angle μ) but also a sufficient commutation margin (indicated by the extinction angle γ), ensuring that the thyristors are ready for the next cycle of operation.

2.3. Superconducting fault current limiters

R-SFCLs represent a straightforward yet promising category among various SFCL types. These devices operate based on the nonlinear resistivity and temperature-phase transition properties of superconductors. During normal operation, the current passing through the superconductor remains below its critical value. While some minor AC losses may occur, the overall losses remain minimal, and the effective resistance perceived by the power systems remains negligible. However, during a short-circuit fault event, the grid current surpasses the critical current of the superconductor. Consequently, a non-negligible resistance emerges to restrict the current flow.

3. Quantitative analysis of SFCLs' impact on commutation failure

3.1. Mechanisms for inhibiting commutation failure using superconducting fault current limiters

For a $\Delta - Y$ transformer, commutation voltages are represented as U_{OP}, U_{PQ}, and U_{QO}, as illustrated in Fig. 2. We assume a transformer turns ratio of k for this configuration.

$$U_{OP} = kU_A, \quad U_{PQ} = kU_B, \quad U_{QO} = kU_C \tag{1}$$

For a $Y-Y$ transformer, commutation voltages are denoted as $U_{MO'}$, $U_{MP'}$, and $U_{MQ'}$, as shown in Fig. 3. In this case, the transformer's turns ratio is $\frac{k}{\sqrt{3}}$.

$$U_{MO'} = \frac{k}{\sqrt{3}}U_A, \quad U_{MP'} = \frac{k}{\sqrt{3}}U_B, \quad U_{MQ'} = \frac{k}{\sqrt{3}}U_C \tag{2}$$

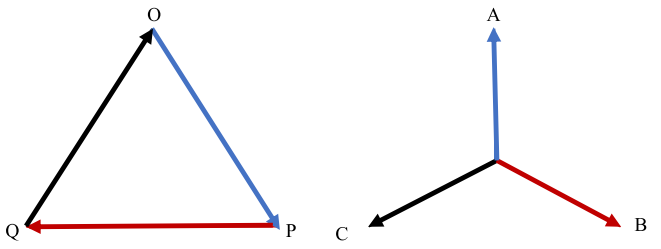

Fig. 2. Phasor diagram of commutation and three-phase voltages in $\Delta-Y$ configuration.

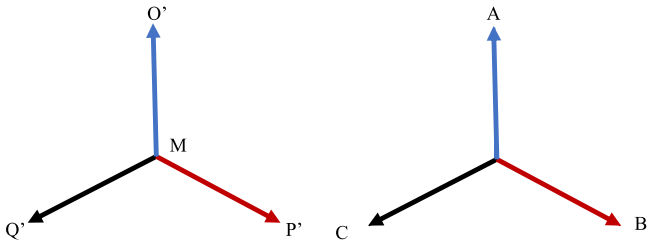

Fig. 3. Phasor diagram of commutation voltages and three-phase voltages in $Y-Y$ configuration.

3.1.1. Commutation voltages for a single-phase-to-ground fault

In the event of a single-phase-to-ground fault (AG), where the voltage of phase A (U_A) decreases by ΔU, the resulting commutation voltages (U_{OP}, U_{PQ}, U_{QO}, $U_{O'P'}$, $U_{P'Q'}$ and $U_{Q'O'}$) are calculated as follows

$$\begin{cases} U_{OP} = k(U_A - \Delta U) \\ U_{PQ} = kU_B \\ U_{QO} = kU_C \\ U_{MO'} = \frac{k}{\sqrt{3}}(U_A - \Delta U) \\ U_{MP'} = \frac{k}{\sqrt{3}}U_B \\ U_{MQ'} = \frac{k}{\sqrt{3}}U_C \end{cases} \tag{3}$$

$$\begin{cases} U_{O'P'} = \frac{k}{\sqrt{3}}\sqrt{3U_A^2 - 3\Delta U U_A + \Delta U^2} \\ U_{P'Q'} = kU_B \\ U_{Q'O'} = \frac{k}{\sqrt{3}}\sqrt{3U_C^2 - 3\Delta U U_C + \Delta U^2} \end{cases} \tag{4}$$

According to the voltage-time-area theory, the commutation area is directly proportional to the voltage amplitude. Among the six voltages mentioned earlier, U_{OP} is significantly smaller than the other five voltages. Consequently, this situation necessitates a higher SFCL resistance, leading to the observation of noticeable peak values in each half cycle.

3.1.2. Commutation voltages for a three-phase fault

For three-phase faults, where the voltages of all three phases decrease by ΔU respectively, the commutation voltages for the Y-Y transformer become:

$$\begin{cases} U_{OP} = k(U_A - \Delta U) \\ U_{PQ} = k(U_B - \Delta U) \\ U_{QO} = k(U_C - \Delta U) \\ U_{MO'} = \frac{k}{\sqrt{3}}(U_A - \Delta U) \\ U_{MP'} = \frac{k}{\sqrt{3}}(U_B - \Delta U) \\ U_{MQ'} = \frac{k}{\sqrt{3}}(U_C - \Delta U) \end{cases} \tag{5}$$

$$\begin{cases} U_{O'P'} = k(U_A - \Delta U) \\ U_{P'Q'} = k(U_B - \Delta U) \\ U_{Q'O'} = k(U_C - \Delta U) \end{cases} \tag{6}$$

In this scenario, the six commutation voltages are approximately equal, leading to the requirement for nearly identical SFCL resistance values, resulting in a stable voltage waveform.

3.1.3. Commutation voltages for a double-phase fault

For double-phase faults, where the commutation voltages for the Y-Y transformer are:

$$\begin{cases} U_{OP} = kU_A \\ U_{PQ} = \frac{k}{2}U_B \\ U_{QO} = \frac{k}{2}U_C \\ U_{MO'} = \frac{k}{\sqrt{3}}U_A \\ U_{MP'} = \frac{k}{2\sqrt{3}}U_B \\ U_{MQ'} = \frac{k}{2\sqrt{3}}U_C \end{cases} \tag{7}$$

$$\begin{cases} U_{O'P'} = \frac{k\sqrt{3}}{2}U_A \\ U_{P'Q'} = 0 \\ U_{Q'O'} = \frac{k\sqrt{3}}{2}U_C \end{cases} \tag{8}$$

It is evident that $U_{P'Q'}$ is the smallest among all voltage values, causing a noticeable peak in the waveform. Double-phase faults are considered the most severe fault type.

3.1.4. Commutation voltages for a double-phase-to-ground fault

Finally, for double-phase-to-ground faults, the commutation voltages for the Y-Y transformer are determined as:

$$\begin{cases} U_{OP} = kU_A \\ U_{PQ} = k(U_B - \Delta U) \\ U_{QO} = k(U_C - \Delta U) \\ U_{MO'} = \frac{k}{\sqrt{3}}U_A \\ U_{MP'} = \frac{k}{2\sqrt{3}}(U_B - \Delta U) \\ U_{MQ'} = \frac{k}{2\sqrt{3}}(U_C - \Delta U) \end{cases} \tag{9}$$

$$\begin{cases} U_{O'P'} = \frac{k}{\sqrt{3}}\sqrt{3U_A^2 - 3\Delta U U_A + \Delta U^2} \\ U_{P'Q'} = \frac{k}{\sqrt{3}}(U_B - \Delta U) \\ U_{Q'O'} = \frac{k}{\sqrt{3}}\sqrt{3U_C^2 - 3\Delta U U_C + \Delta U^2} \end{cases} \tag{10}$$

In this case, the six commutation voltages are larger, necessitating smaller SFCL resistance values, compared to the previous scenario.

4. Case study

4.1. Modeling of the investigated DC grid

A single-line diagram of the simulated DC network is shown in Fig. 4. The test network comprises three AC grids connected via a monopolar 500 kV HVDC link.

On both the rectifier and inverter sides, a twelve-pulse converter is used, consisting of two six-pulse Graetz bridges. These bridges are connected to Y-Y and Y-Δ transformers, respectively, ensuring a 30-degree phase shift in the AC voltage supplied to each bridge. The series connection of these bridges effectively reduces the ripple component, which is six times the fundamental frequency, thereby minimizing harmonic distortion.

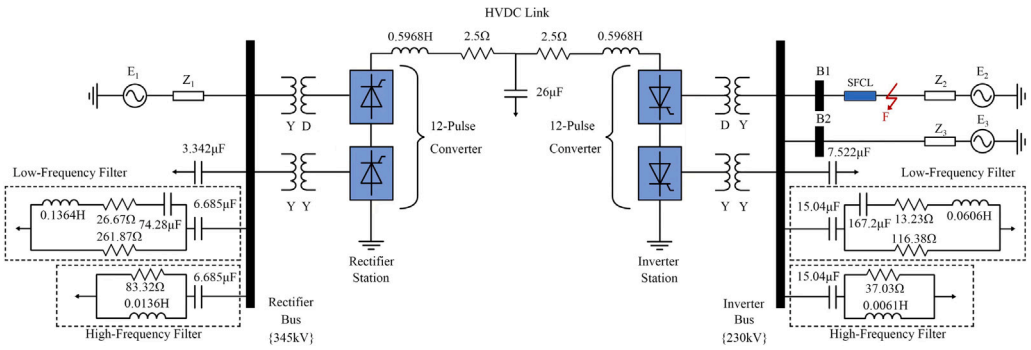

Fig. 4. Single-line diagram of the representative DC network.

Table 1
Parameters of the test network.

Parameter [Unit]	Rectifier	Inverter
Bus line-to-line voltage [kV]	345	230
AC system frequency [Hz]	50	50
Nominal firing angle [deg]	15	–
Nominal extinction angle [deg]	–	15

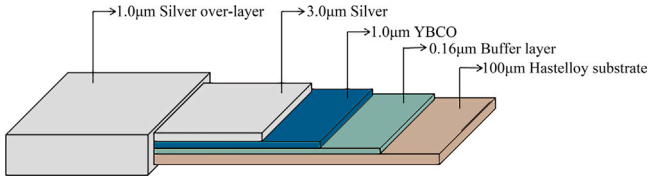

Fig. 5. Geometrical sizes of the 2G YBCO tapes employed in the R-SFCL model. Sizes refers to the SF12100 tapes from Superpower Inc. company.

The rectifier side features one AC system, while the inverter side has two identical AC systems. To model the AC networks, a voltage source and a reactance are employed in series, connected to the transformers through rectifier and inverter buses.

During the simulations, four types of short-circuit faults will be introduced at the designated locations. R-SFCLs with varying resistance values will be installed and tested in one AC network on the inverter side.

Low-frequency and high-frequency filters are deployed on both sides to effectively filter out harmonics.

The parameters of the test network are listed in Table 1.

4.2. Thermal-electric analogy method for R-SFCL modeling

To simulate the transient behavior of the R-SFCL, calculations of layer resistances and current distribution within these layers are necessary. Additionally, it is essential to compute the temperature rise of the tapes during fault periods. An effective R-SFCL model should not only account for the heating of the HTS material but also consider heat transfer within the HTS material, interactions with adjacent layers, and heat exchange with the surrounding environment (LN_2 cooling bath). Implementing these calculations directly can be computationally challenging (see Fig. 5). To address this, we employ a thermal-electric analogy method for solving the heat transfer equations within the SFCL layers, which are shown in Fig. 5. A comprehensive description of this method can be found in [26]. Fig. 6 depicts an equivalent network representing the thermal behavior of the R-SFCL, established using the thermal-electric analogy method. The R-SFCL model comprises series-connected coils, each consisting of superconducting YBCO tapes and a parallel stainless steel shunt resistor. The number of coils can be adjusted to set the SFCL resistance.

Each HTS module contains several tapes arranged anti-parallel for reduced inductance, all connected through a common center contact. The modules are cryogenically cooled with liquid nitrogen (LN_2) at 77 K, and the SFCL model exhibits a consistent quench time of less than 1 millisecond. In this simulation, we incrementally increase the resistance from 0 to 100 Ω to assess its impact on suppressing commutation failures.

4.3. Simulation results

4.3.1. Exploring SFCL resistance values for achieving successful commutation

The results derived from an extensive series of PSCAD simulation tests conducted on the proposed SFCLs are presented and analyzed in Fig. 7. These simulations encompass a comprehensive range of fault scenarios, each characterized by distinct fault types and varying fault resistance values. To ensure methodological consistency, a fault was intentionally initiated at $t = 2$ s in all cases, persisting for a precisely defined duration of 0.2 s.

The primary objective of this systematic investigation was to assess the dynamic behavior of the SFCL in response to the complexity of real-world electrical faults. A key focus was the role of fault resistance, which was methodically varied within the spectrum of 0 Ω to 100 Ω. The critical inquiry revolved around identifying the minimum SFCL resistance necessary to ensure seamless and successful commutation under these diverse fault conditions.

Furthermore, the study explores the temporal aspects of fault initiation. Multiple fault initiation times were scrutinized, spanning a time window from 2.000 s to 2.020 s, with intervals of 0.002 s. This nuanced analysis aimed to discern the intricate relationship between fault initiation timing and the corresponding SFCL resistance values, thereby providing invaluable insights into the SFCL's adaptability and effectiveness in mitigating commutation failures within a dynamic LCC-HVDC system.

In the context of a single-line-to-ground fault occurring at point F within the test network, as depicted in Fig. 7(a), it becomes evident that the minimum SFCL resistance required to ensure successful commutation exhibits a consistent trend. As the fault resistance decreases, the minimum SFCL resistance needed increases. To illustrate, when the fault resistance reaches 0 Ω, the SFCL resistance must be set at a minimum of 35 Ω to guarantee successful commutation. Conversely, when the fault resistance is 100 Ω, an SFCL with a mere 1 Ω resistance value meets the requirement. This is because as the fault resistance increases, the fault current decreases, making it easier to control and limit the current using SFCLs. Therefore, a lower resistance SFCL is needed to effectively limit the fault current and ensure successful commutation. It is important to note that this necessary SFCL resistance may vary with different fault initiation times; however, regardless of the precise timing of the fault event, configuring the SFCL with the corresponding resistance value consistently prevents commutation

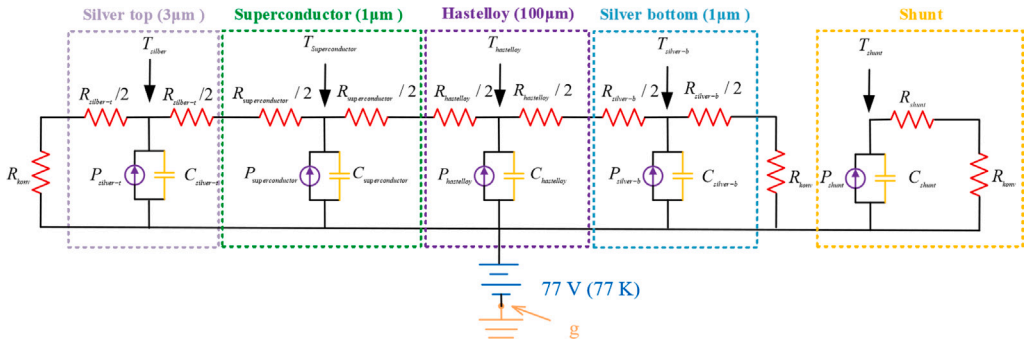

Fig. 6. Equivalent thermal-electric circuit of 2G YBCO tape.

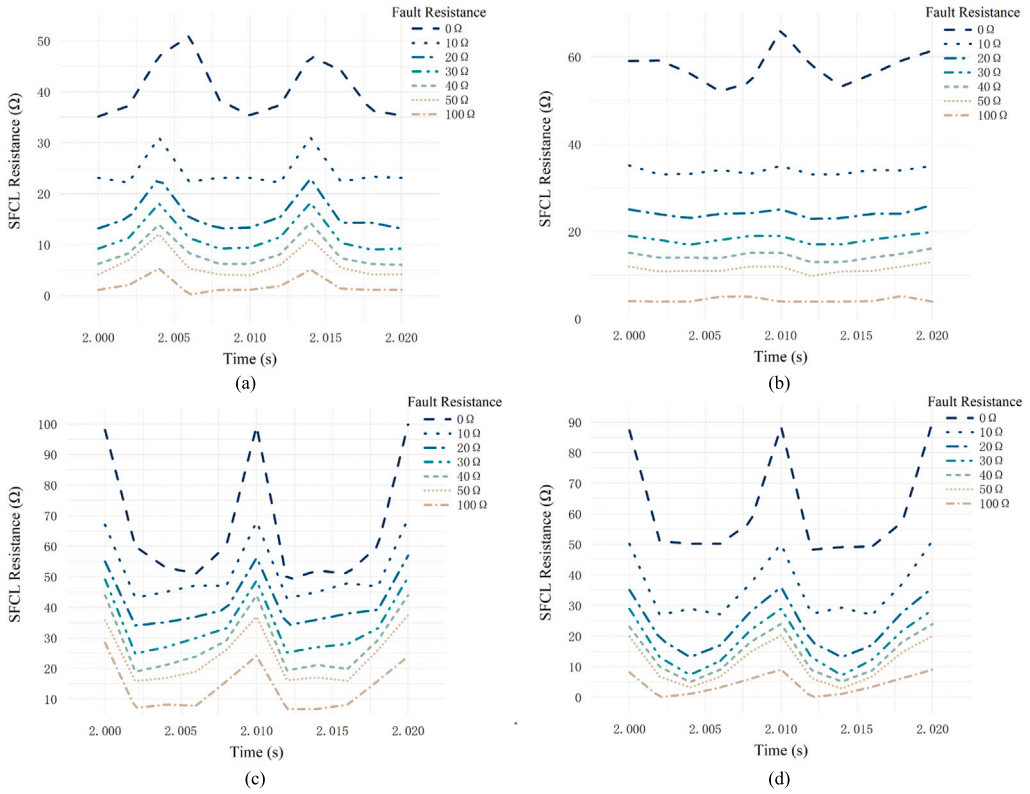

Fig. 7. Minimum SFCL resistance for commutation failure suppression across various fault types and initiation times. (a) for single-line-to-ground faults, (b) for three-phase faults, (c) for double-phase faults, and (d) for double-phase-to-ground faults.

failure. This underscores a noteworthy advantage of employing SFCL for commutation failure mitigation over the conventional method of adjusting the firing angle. It is important to emphasize that during the analysis, a distinct resistance peak was observed, lasting for ten milliseconds, and this corresponds to the mathematical underpinnings in prior sections.

In the case of a three-phase fault, as depicted in Fig. 7(b), we observe that the requisite SFCL resistance is generally higher when compared to a single-line-to-ground fault. This phenomenon arises due to the symmetrical nature of the fault, resulting in only minor variations in the minimum SFCL resistance for different fault initiation times, particularly when the fault resistance is substantial. This observation aligns harmoniously with our previous mathematical analysis. To elaborate further, a SFCL resistance of approximately 5 Ω is deemed sufficient to ensure successful commutation when the fault resistance amounts to 100 Ω. Conversely, when the fault resistance is nil (0 Ω), an SFCL resistance within the range of 52–68 Ω is found effective in averting commutation failure. Notably, these resistance values exhibit fluctuations corresponding to different fault initiation times, reaching their zenith at 2.010 s and nadir at approximately 2.005 s. This sensitivity to fault initiation times highlights the importance of considering the timing of faults when designing SFCL systems for commutation failure mitigation.

In the context of double-phase faults, as demonstrated in Fig. 7(c), we examine the critical aspect of determining the minimum SFCL resistance required to effectively mitigate commutation failure across various fault initiation times. Similarly, the requisite SFCL resistance for double-phase faults far surpasses that demanded by single-line-to-ground faults or even three-phase faults. This observation emphasizes the unique challenges posed by double-phase faults and underscores the remarkable adaptability of SFCLs to distinct fault scenarios. With increasing fault resistance, SFCL resistance requirements inversely diminish, effectively mitigating commutation failure. This reveals the dynamic interplay between fault characteristics and SFCL response, showcasing the device's adaptability to diverse fault conditions. We also observe a high sensitivity of the required SFCL resistance to the fault initiation time, with peaks at specific intervals, namely 2.000, 2.010, and 2.020 s. This temporal dependence highlights the significant

influence of fault timing on SFCL performance. Conversely, during intermediate time periods, the SFCL resistance requirement diminishes.

For a double phase to ground fault, Fig. 7(d) presents the scenario, revealing a distinct behavior in comparison to single-line-to-ground and three-phase faults. Notably, the required SFCL resistance surpasses that necessitated by single-line-to-ground faults but falls short of the demands observed in double-phase faults, resembling a less severe counterpart. An intriguing revelation lies in the sensitivity of the minimum SFCL resistance to the precise timing of fault initiation. This recurring theme accentuates the significance of fault initiation timing on SFCL performance, consistently highlighting the highest resistance requirements at temporal junctures of 2.000, 2.010, and 2.020 s.

The observed results in the simulations can be explained by the behavior of the DC system, fault conditions, and the role of the SFCL. In the first scenario (single-line-to-ground faults), a fault occurs, leads to an unbalanced fault condition. Lower fault resistance (0 Ω) leads to a more severe fault condition with higher fault current. The SFCL's role is to limit this fault current, preventing excessive current flow and subsequent commutation failure. The SFCL's resistance requirement is higher for lower fault resistance to effectively limit the fault current. Varying fault initiation times do not significantly affect the SFCL's resistance requirement because the unbalanced fault condition remains consistent.

In the second scenario (three-phase faults), all three phases are involved, creating a symmetrical fault condition. The SFCL still needs to limit fault current, but the balanced nature of the fault reduces the severity compared to unbalanced faults. The SFCL's resistance requirement is generally higher than for single-line-to-ground faults due to the involvement of all phases. Fault initiation times have a minor impact on SFCL resistance requirements due to the symmetrical nature of the fault.

In the third scenario (double-phase faults), The SFCL must limit the fault current in a situation where two phases are involved. Similar to single-line-to-ground faults, the SFCL's resistance requirement is higher for lower fault resistance. The SFCL's resistance requirement is sensitive to fault initiation times because the severity of the fault and fault current vary as different phases are involved.

In the fourth scenario (double-phase-to-ground faults), the faults are less severe than double-phase faults but more severe than single-line-to-ground faults. The SFCL must limit fault current in a situation where two phases are involved and at least one phase is grounded. The resistance requirement for SFCL falls between that of double-phase and single-line-to-ground faults. Fault initiation times still have a noticeable impact due to the asymmetrical fault nature, with peaks at certain times.

In summary, the severity of commutation failures in LCC-HVDC systems depends on fault conditions and the SFCL's ability to limit fault current. The SFCL's resistance requirement varies with fault type, fault resistance, and fault initiation times, with more severe faults demanding higher SFCL resistance. The sensitivity to fault initiation times arises from variations in fault current magnitude at different time instants.

Fig. 8 presents a comparative analysis of the minimum fault resistance required to prevent commutation failure across the four types of short circuits. Notably, double-phase faults pose the most severe challenge, demanding a significantly higher fault resistance of approximately 600 Ω to ensure successful commutation. For the other fault types, a fault resistance of 250 Ω is sufficient to maintain a stable system without experiencing commutation failure.

These results underscore the adaptability and efficacy of SFCLs in safeguarding power grids from the potentially catastrophic consequences of commutation failures. As witnessed in our investigation, the required SFCL resistance varies significantly depending on fault type, fault resistance, and fault initiation time, emphasizing the dynamic nature of the interaction between fault characteristics and SFCL response. Our findings not only contribute to the understanding of commutation failure but also provide practical guidance for the implementation of SFCLs in real-world HVDC systems. By tailoring SFCL parameters to specific fault conditions, power system operators can enhance the reliability and resilience of their networks. As the demand for clean and efficient energy transmission continues to grow, SFCLs stand as a promising technology, offering a robust solution to one of the critical challenges facing HVDC systems.

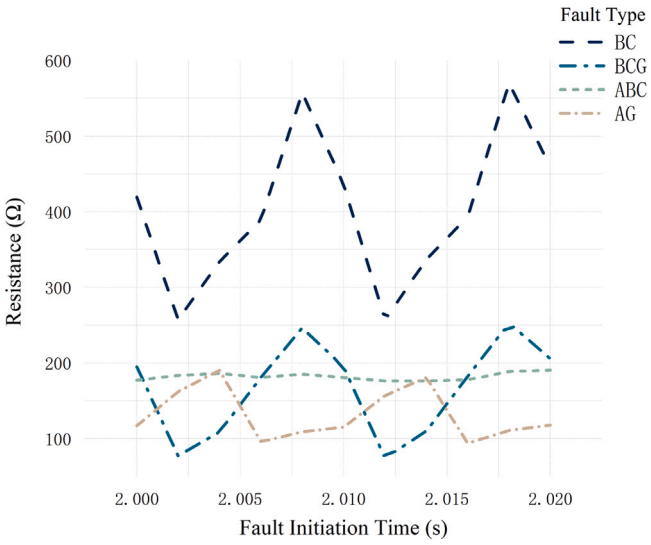

Fig. 8. Minimum fault resistance for successful commutation at different initiation times across four fault types.

4.3.2. Impact of SFCL on a LCC-HVDC system affected by commutation failure

Through simulations and analyses, this study investigates how the integration of SFCLs impacts the behavior of HVDC systems during fault conditions. The analysis focuses on key parameters: Active Power, Extinction Angle, Voltage Waveforms, and Valve Voltages. These parameters provide valuable insights into the influence of SFCLs on HVDC system performance during faults.

In Fig. 9(a), we witness a pivotal transformation in the behavior of active power when a fault occurs at 2.0 seconds (s). The active power experiences a rapid decline from its initial 980 MW to nearly 0 MW, a stark signal of power transmission interruption due to commutation failure. This phenomenon arises as the fault disrupts the normal current flow in the system. However, the inclusion of an SFCL brings about a remarkable change. The SFCL's resistive nature acts as a buffer, limiting the abrupt drop in active power to only 50% of the loss observed in the absence of an SFCL. This reduction signifies the SFCL's effectiveness in preserving power continuity during fault events.

Moving to Fig. 9(b), we explore the behavior of the extinction angle, a critical parameter indicative of commutation success or failure. In the absence of an SFCL, the extinction angle rapidly diminishes to 0 degrees within milliseconds, a clear indication of commutation failure. This abrupt drop in the extinction angle is a consequence of the inverter's inability to effectively switch from one thyristor valve to another during the fault. However, with the strategic installation of an SFCL, a transformative improvement unfolds. The SFCL plays a pivotal role in maintaining the extinction angle above zero degrees, signifying the system's ability to successfully manage the commutation process even under fault conditions. This remarkable achievement underscores the SFCL's capability to avert commutation failure.

Fig. 9(c) provides a comparative analysis of voltage waveforms, shedding light on the profound impact of an SFCL. In the absence of an SFCL, the DC voltage at the inverter side plunges to zero, an unmistakable signal of commutation failure. Conversely, with the inclusion of an

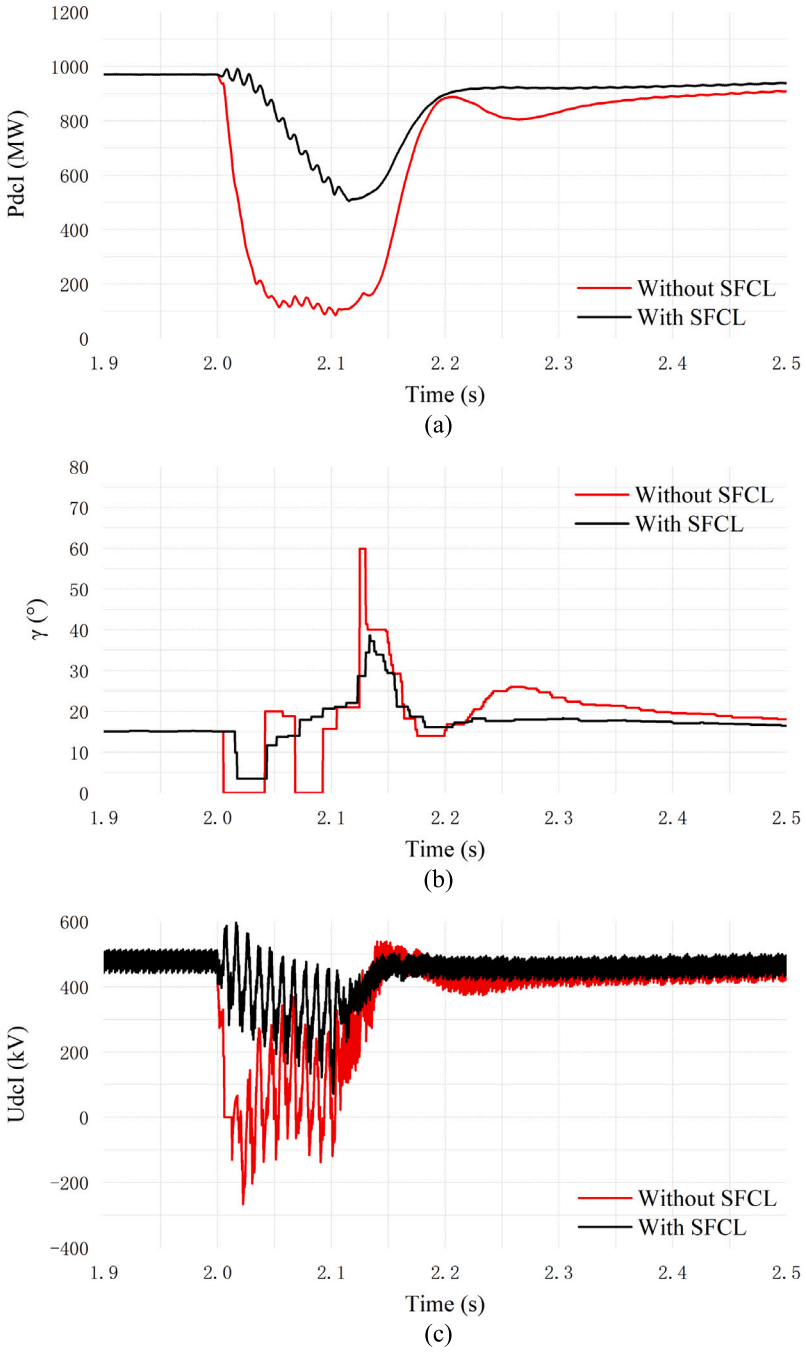

Fig. 9. Comparative analysis of the DC grid with and without SFCLs in terms of (a) Active power, (b) Extinction angle, and (c) Voltage waveforms.

SFCL, a transformative effect takes place. The SFCL actively enhances the DC voltage, preventing it from reaching zero, and thus averting commutation failure. This transformation underscores the SFCL's role as a guardian of voltage stability within the HVDC system.

Fig. 10 examines valve voltages, specifically those of T3 and T6. Without the protective shield of an SFCL, instances occur where the voltages of T3 and T6 simultaneously drop to zero, a clear manifestation of commutation failure. This simultaneous conduction of valves represents a precarious situation where the inverter fails to maintain proper phase synchronization. However, with the strategic integration of an SFCL, these concerns are addressed effectively. The SFCL intervenes to ensure stable valve operation, effectively mitigating the risk of commutation failure.

In summary, the SFCL acts as a protective device that limits fault currents and controls the system's behavior during commutation failures. It prevents extreme drops in power, maintains positive extinction angles, stabilizes DC voltage, and ensures proper valve switching, all of which contribute to the successful mitigation of commutation failures in the LCC-HVDC system.

5. Conclusion

This paper presents a comprehensive analysis of R-SFCLs as a viable solution to mitigate commutation failures in the LCC-HVDC systems. Commutation failures, a pervasive issue in HVDC transmission, can lead to adverse consequences in power grid stability. This study explores the performance of R-SFCLs through detailed simulations using the PSCAD platform.

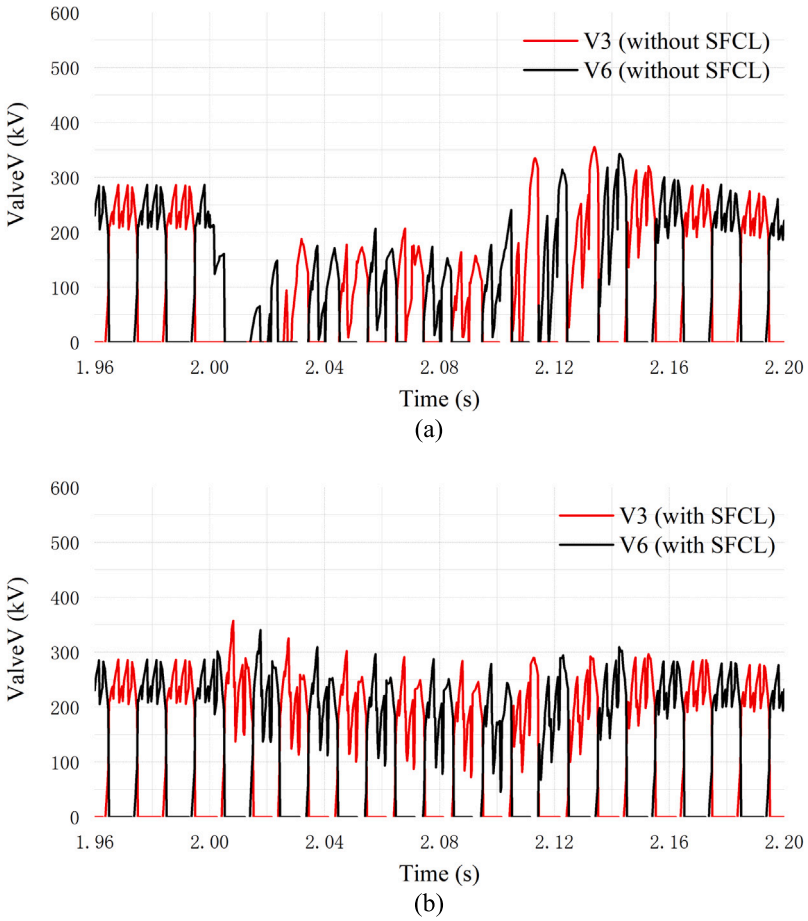

Fig. 10. Comparison of valve voltage waveforms for T3 and T6 with and without SFCLs. (a) without SFCLs (b) with SFCLs.

The analysis encompasses a range of fault scenarios, including variations in fault resistance values and fault initiation times, for four distinct fault types occurring within the DC system. The primary objective is to determine the efficacy of R-SFCLs in preventing commutation failures under diverse operating conditions.

The results unveil a promising outcome: SFCLs with specific resistance values exhibit the capability to preempt commutation failures. This resilience is maintained even in the face of both symmetrical and unsymmetrical faults. Moreover, the implementation of R-SFCLs yields notable improvements in voltage and active power waveforms, contributing to enhanced system stability. An additional benefit observed is the augmentation of the extinction angle, which is pivotal for LCC-HVDC system performance.

In conclusion, the findings of this study underscore the significance of selecting suitable resistance values when deploying SFCLs. Such an approach demonstrates the potential to effectively mitigate commutation failures, addressing a critical challenge in the LCC-HVDC systems. These results hold promise for the continued development and application of R-SFCLs in the context of HVDC transmission, with the ultimate goal of bolstering grid reliability and stability.

CRediT authorship contribution statement

Qihuan Dong: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Validation, Visualization, Writing – original draft, Writing – review & editing. **Haozong Wang:** Software. **Binshu Chen:** Investigation. **Ning Zhang:** Funding acquisition. **W.T.B. de Sousa:** Supervision. **Yilu Liu:** Supervision.

Declaration of competing interest

The authors of this manuscript, Qihuan Dong and Haozong Wang, Binshu Chen, Ning Zhang, W.T.B de Sousa, Yilu Liu declare no conflicts of interest regarding the research conducted and the submission of this paper to the International Journal of Electrical Power and Energy Systems. We affirm that this research was carried out without any external influence, financial or otherwise, that could be perceived as a potential conflict of interest.

Additionally, we confirm that no funding agency or organization with a vested interest in the results of this research has had any influence over the research design, data analysis, interpretation of findings, or the decision to submit this manuscript for publication.

We provide this statement to assure the integrity and transparency of our research work and to comply with the guidelines and standards set by the International Journal of Electrical Power and Energy Systems.

Data availability

The data that has been used is confidential.

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Ethical compliance

Our research involves no human or animal subjects and adheres to ethical standards in electrical engineering.

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