An Embedded GaN Power Module with Double-Sided Cooling and High-Density Integration

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***Abstract*—In this paper, an embedded GaN half-bridge power module with double-sided cooling, low inductance, low thermal resistance, on-package decoupling capacitors, localized common mode filter, and integrated gate drivers is proposed. The two GaN dies are embedded in a printed circuit board (PCB) with heat dissipation paths to a ceramic substrate from both sides of the devices to achieve double-sided cooling capability. Thermal and electrical performance are fully analyzed and optimized. A low-cost module assembly procedure is presented utilizing standard layer attaching process. Finally, a compact 2.7 cm × 1.8 cm half-bridge GaN power module is fabricated to verify both electrical and thermal performance through experiments. The switching performance of the power module is tested under 400 V/25 A double-pulse test that shows the power loop inductance is as low as 1.03 nH and the overshoot voltage of the switching waveform is less than 5% of the dc bus voltage. The thermal resistance is verified to be 0.32 K/W, and the fabricated power module is employed in a buck converter with 500 W output power at 600 kHz switching frequency.**

Keywords— GaN power module, embedding technology, double-sided cooling, integrated gate driver, parasitic inductance.

I. Introduction

The lateral Gallium Nitride (GaN) high electron mobility transistors (HEMT) are being applied in many power electronics applications that require fast switching capabilities and low on-resistance, making them suitable for high-frequency, high-density, and high-efficiency systems [1-2]. However, the fast switching speed requires more attention to the circuit design, especially to the parasitic elements [3-4]. The large parasitic inductance in the power loop causes more severe voltage overshoot and switching loss. The parasitic inductance of the gate loop also should be reduced due to the lower threshold voltage of GaN device. In addition, the heat dissipation of lateral GaN dies are more challenging due to the lateral structure and higher current density. Therefore, a reliable GaN power module need to consider thermal management, electrical performance, and cost reduction.

Several researches have proposed unique power modules to integrate decoupling capacitors and driver components to reduce the parasitic parameters in the gate loop and the power loop. GaN Systems [5] proposed a GaN half-bridge power module based on the insulated metal substrate (IMS), while another printed circuit board (PCB) integrated with drivers and decoupling capacitors on top of the IMS. Similarly, a multi-substrate hybrid GaN module is proposed in [6-7] to integrate the gate drivers and decoupling capacitors. Reference [8] presents a PCB-embedded GaN power module with on-package drivers and capacitors. However, most power modules with integrated components are single-sided cooling. A recent effort [9] to improve the thermal performance of a GaN power module with integrated components by implementing double-sided cooling. Two GaN dies are sandwiched between two ceramic substrates, and copper pillars are used to connect drain to source to achieve double-sided cooling, but this usually results in higher manufacturing costs. The other problem arises due to the height mismatch between the device and other components. Therefore, attaching direct bonded copper (DBC) on the top only can cover the die, not the entire area.

To design a double-sided, low inductance, integrated gate driver, and low-cost power module, an embedding technology has been applied to the proposed GaN half-bridge power module. The structure of the proposed module, optimization of parasitic parameters and thermal analysis are discussed. The designed module shows excellent switching performance with 1.03 nH power loop inductance and less than 5 % overshoot voltage at 400 V/25 A. Such modules will find immediate applications in on-board chargers and data centers with significantly improved power density and operation frequency.

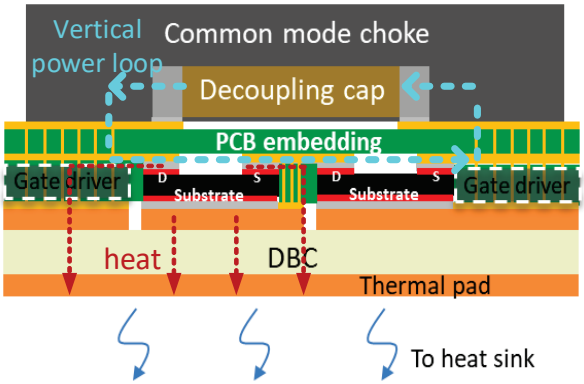
II. Embedded Power Module Analysis

A. Embedded GaN Power Module

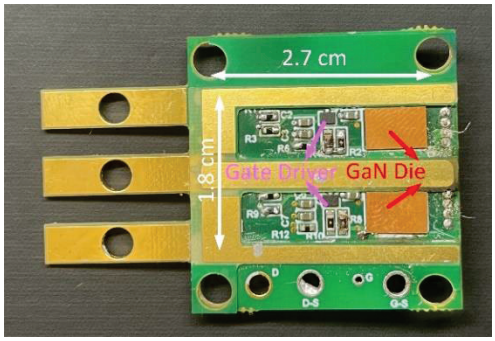
The concept of a single-sided cooling GaN power module is popular because of the easy-to-implement structure. However, the junction temperature of GaN dies in power modules with single-sided cooling can still be high since part of the heat is generated on the top side. Therefore, employing double-sided cooling will further reduce the thermal resistance, thereby improving the thermal management.

This paper proposes a low-cost, double-sided-cooled, vertical loop power module with integrated decoupling capacitors, common-mode filter, and integrated gate driver. The proposed module shown in Fig. 1 is realized by embedding technology with a size of 2.7 cm × 1.8 cm for 5 kW applications. The hybrid structure adopts the benefit of low-cost PCB and

excellent thermal performance of DBC because of the high thermal conductivity of AlN. Two GaN dies are soldered to the bottom layer of the PCB with the die substrate attached to the DBC directly. The decoupling capacitors and gate drivers are integrated on the multilayer PCB to reduce the parasitic inductance in both the power loop and the gate loop. The integrated electromagnetic interference (EMI) filter placed on the top of PCB is designed to achieve higher attenuation than adding external EMI filters [10]. The majority of the heat generated by the die can be dissipated through the bottom layer as the die is attached to the DBC directly; the heat generated on the top side of the die will be directed through the thermal vias from the PCB to the DBC as well to realize double-sided cooling.



(a)



(b)

Fig. 1. (a) Illustrastion of the layers and components at the cross-section of the power module with double-sided cooling, decoupling capacitors, CM choke, and gate driver; (b) bottom view of the PCB showing gate drivers and GaN dies in the embedding layer without DBC attached.

B. *Power Loop Parasitic Design and Optimization*

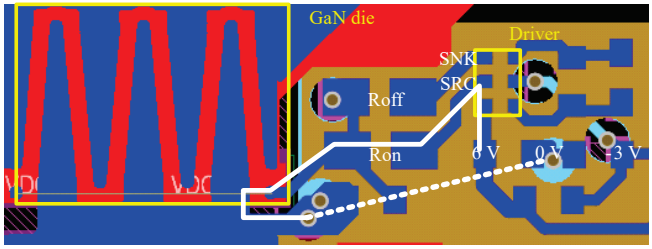
The power loop inductance in a half-bridge power module induces the voltage overshoot that causes stress on devices during the trun-off transient. The influence of loop inductance becomes more severe in extreme fast-switching GaN devices. Very high drain-current slope d*i*/d*t* is generated during switching transient of GaN devices and voltage overshoot caused by loop inductance is larger than that of SiC and Si devices. Besides, The effect of power loop inductance results in increased switching energy losses. Therefore, the power loop inductance needs to be minimized.

In the conventional 2-D power module package design, the loop inductance is reduced by shortening the physical length of the commutation loop, but it is still too large for GaN device. To further reduce the parasitic inductance, the vertical power loop or 3-D power loop is the option. The proposed power loop adopts the vertical power loop structure thanks to the design flexibility enabled by multi-layer PCB technology as shown in Fig. 1(a). It creates a vertical current path within the multi-layer PCB. The parasitic inductance is reduced significantly due to the self-cancellation of magnetic flux. In the vertical power loop, the loop inductance is mainly governed by the board thickness. To decrease the thickness of the board, the multi-layer PCB is chosen to be 0.4 mm with a power loop inductance of 1.27 nH simulated from Ansys Q3D.

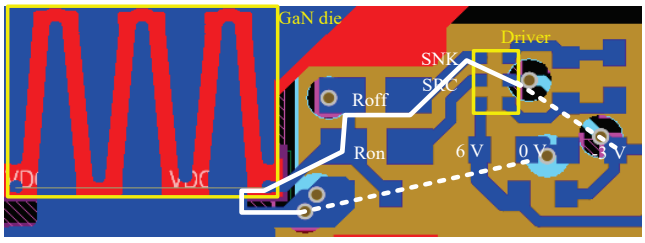
C. *Gate Loop Parasitic Design and Optimization*

For GaN HEMT dies, the value of the threshold voltage is very low, which makes the GaN dies more sensitive to the gate circuit [11]. Besides, the margin of tolerance of GaN die is stringent. The maximum rating for gate to source voltage of the selected 650 V/60 A GaN die is -10 V to 6 V. Therefore, the oscillation at the gate during the switching should be less than the maximum voltage rating. Gate overshoot voltage and undershoot voltage are affected by the gate loop inductance. An optimized gate loop inductance and proper external gate resistance need to be identified.

In the proposed design, the gate loop inductance is significantly reduced by integrating gate drivers. The gate drivers are embedded adjacent to the GaN dies to minimize parasitic inductances as shown in Fig. 1(b). A small gate loop area with a shielding layer is shown in Fig. 2. Besides, the 1EDN7550U gate driver is selected for integration because of the small PG-TSNP-6 package size will further reduce the gate loop area. The simulated turn-on gate loop inductance and turn-off gate inductance of the upper die are 0.32 nH and 0.29 nH, respectively; and those of the lower die are 0.30 nH and 0.34 nH.



(a) Turn-on gate loop



(b) Turn-off gate loop

Fig. 2. PCB layout showing (a) the turn-on gate loop and (b) the turn-off gate loop.

D. Cross-coupling Capacitances Minimization

In a half-bridge GaN power module, the switch node (SW) voltage swings between bus voltage (VDC+) and ground voltage (VDC-) that results in a very high dv/dt rate. The coupling capacitance between high power nodes (VDC+ and SW) and other noise-sensitive signal traces could cause coupling noises that lead to the false triggering of the gate signals. Therefore, large copper pads placed between these power nodes and gate signal paths are used as shielding layers to minimize the coupling noises. Fig. 3 shows the designed layer arrangement of the 4-layer PCB in the power module. Take the high-side switch as an example, all signals and auxiliary power are referenced to a large solid shielding layer that has the same potential as the high-side ground, so the coupling capacitances between the VDC+ and the signal traces are minimized. These coupling capacitances on the high side with shielding and without shielding layers are extracted by Ansys Q3D and listed in Table I.

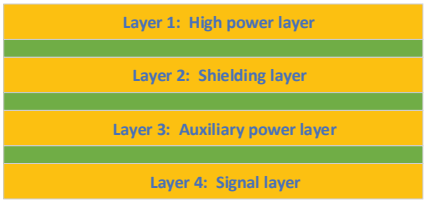


Fig. 3. Layer stack of 4-layer proposed

TABLE I. COUPLING CAPACITANCE BETWEEN POWER NODE (V_{DC}) AND HIGH-SIDE SIGNAL

	VDC+ to PWM	VDC+ to auxiliary power (-3 V)	VDC+ to auxiliary power (6V)
With shielding layer	0.00 pF	0.01 pF	0.00 pF
Without shielding layer	4.68 pF	7.5 pF	1.7 pF

E. Thermal Performance Evaluation

Steady-state thermal simulations are conducted for GaN HEMTs comparing different structures as shown in Fig. 4. Three structures using the same GaN die and outline dimensions are designed representing the single-sided cooling (Fig. 4(a)), the traditional double-sided cooling using DBCs (Fig. 4(b)), and the proposed double-sided cooling (Fig. 4(c)) structure. The power loss of each GaN die is set at 5 W and the temperature at the module exterior is kept constant at 70 °C. According to the thermal simulation, although the double-sided cooling structure using two layers of DBC presents the lowest thermal resistance, it yields a high-cost fabrication procedure, especially if vertical loop is desired. Compared to single-sided cooling, the proposed double-sided cooling structure reduces the junction-to-case thermal resistance to 0.318 K/W because of the additional path dissipating heat from the top side of the die. The proposed power module is considered optimal for the tradeoff between cost and thermal performance.

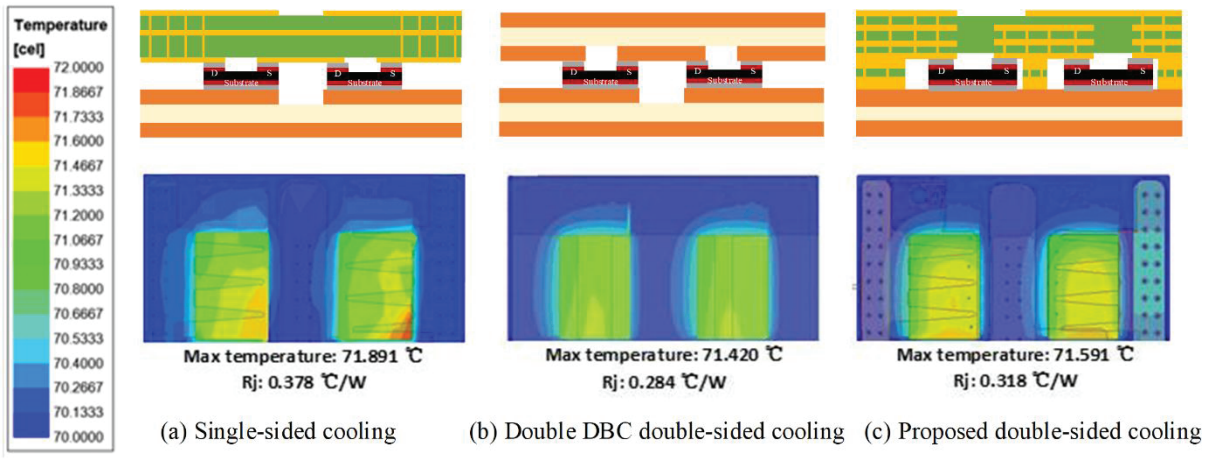


Fig. 4. Thermal simulation setup and results of (a) PCB+DBC power module with single-sided cooling; (b) double DBC with double-sided cooling; (c) PCB+DBC power module with double-sided cooling.

III. POWER MODULE FABRICATION

The components used to fabricate the power module are listed in Table II. The GaN dies used in the module are GS-065-060 with a size of 6.0 mm × 4.0 mm × 0.27 mm from GaN Systems. For the embedding process, the gate driver selection is critical since the size and thickness should be comparable to the GaN dies. In this design, 1EDN7550U [12] is chosen due to the small PG-TSNP-6 package with a size of 1.5 mm × 1.1 mm × 0.375 mm. The 0.1 mm difference in the thickness of the gate driver and GaN die can be evened after applying the soldering layer. The decoupling capacitance is selected as 1 µF to reduce the influence of inductance on the power loop. The PCB

embedding power module fabrication flow chart is shown in Fig. 5, and the detailed process is described as follows:

1) Power module PCB and cavity PCB are fabricated. The cavity PCB is selected to have a thickness of 0.254 mm to be aligned with the GaN thickness.

2) A 100-um thick stencil board is used to apply solder paste Sn965Ag3Cu0.5 with the melting temperature 217 °C on the bottom layer of the power module PCB. The GaN dies, gate drivers, and the cavity PCB are placed in the corresponding positions on the power module PCB. Apply a suitable temperature profile [13] in the T-962A reflow oven and reflow the power module board, cavity board, and all the components.

3) The bus decoupling capacitors and the CM choke are placed on the top layer of the power module. Sn965Ag3Cu0.5 solder wire is used in this step and melted by the soldering iron.

4) Attaching the DBC substrate to the power module board with cavity board needs a second reflow profile, which should be handled carefully to prevent the solder in the previous step from melting. The Sn63Pb37 solder paste is selected in this step with a melting temperature of 183 °C, which is lower than that of the solder used in step 2. First, the solder paste is applied to all the pads on the DBC, and the DBC is attached to the power module with cavity PCB. Second, the DBC is heated by the hot plate, and put a thermocouple close to the DBC for temperature monitoring until the temperature reaches 185-195 °C. The ramp rate should be less than 3°C/second. Third, heat is applied for 20-30 seconds and then heat is removed.

TABLE II. COMPONENT SELECTION

Component	Value	Part
GaN die	650 V/ 60 A	GS-065-060
Driver		1EDN7550U
Turn-on resistor	5 Ω	RCS06035R10FKEA
Turn-off resistor	0 Ω	HCJ0603ZT0R00
Driver decoupling cap	1 µF	CGB2A1X5R1E105K033BC
Bus decoupling cap	0.3 µF	C4532X7T2J304M250KA

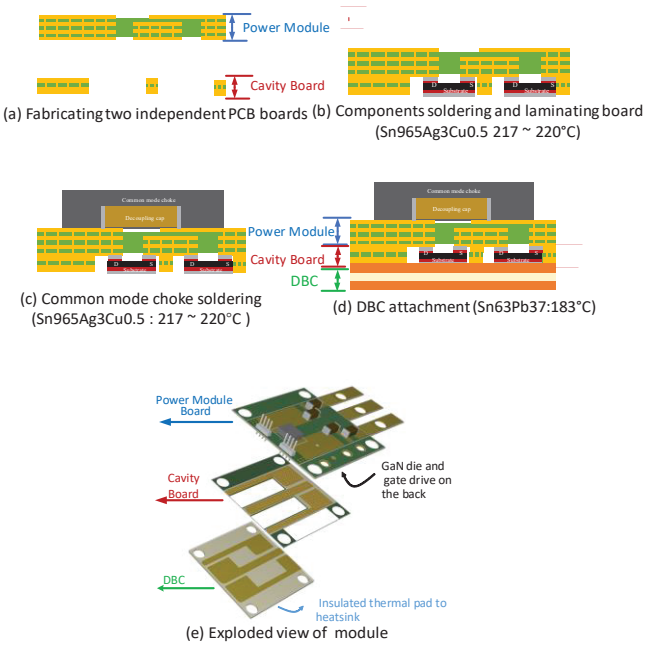


Fig. 5. Fabrication process of the proposed GaN power module.

IV. EXPERIMENTAL VERIFICATION

This section focuses on the characterizations of the switching dynamics and thermal performance of the power module fabricated. The EMI performance of the power module with integrated common-mode choke is discussed in [10] and omitted herein.

A. Double Pulse Test

A double pulse test (DPT) circuit is built as shown in Fig. 6 to characterize the power module's switching behavior. The power module is tested at 400 V dc bus voltage and 25 A load current at room temperature (25 °C), and the characterization results of hard-switching transition for the proposed power module are shown in Fig. 7. The overshoot voltage across the die is less than 5% of the static voltage from the turn-off transient as shown in Fig. 8. Moreover, the loop inductance extracted from the ringing frequency yields 1.03 nH, which is much smaller than comparable designs (e.g. 2.35 nH in [5]):

$$L_{loop} = \frac{T^2}{4\pi^2\left(C_{oss} + C_{para} + C_{probe}\right)} = \frac{2.3\ ns^2}{4\pi^2(127 + 1.5 + 1.8)\ pF} = 1.03\ nH \quad (1)$$

where C_{oss} is the output capacitance of GaN die, C_{para} is the parasitic capacitance induced by PCB layout, and C_{probe} is the capacitance induced passive probe.

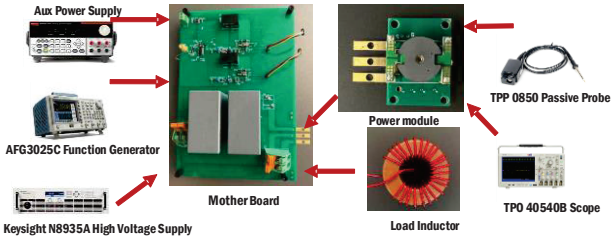


Fig. 6. Double pulse test prototype setup.

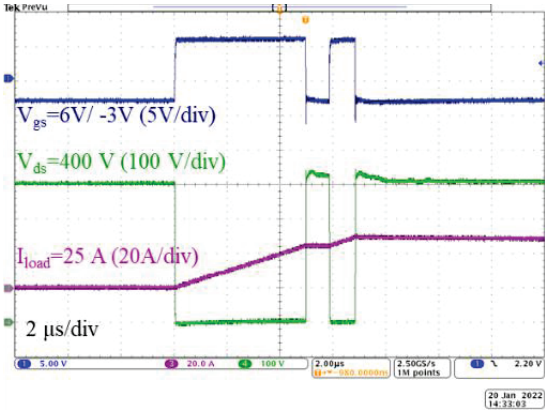
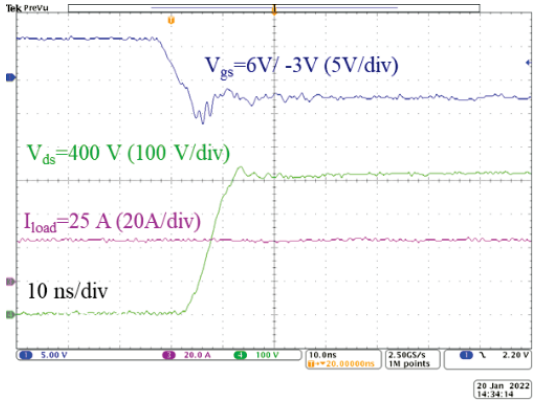


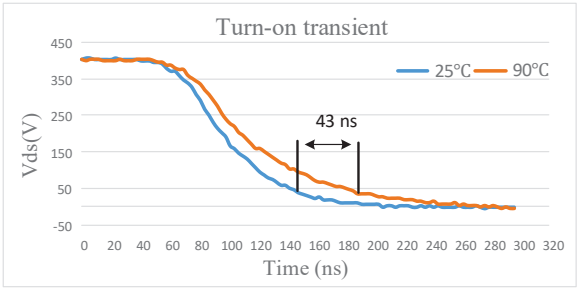
Fig. 7. Switching waveforms obtained from the double-pulse test under 400 V and 25 A.



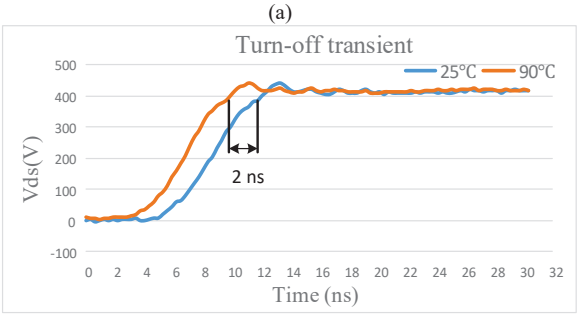
(b)

Fig. 8. Zoom-in view of switching waveforms at the turn-off transient showing low overshoot and fast dv/dt.

The power module is placed on a hotplate and heated up to 90 ºC to characterize the switching performance under higher ambient temperature. The temperature-dependent turn-on and trun-off transient on the drain to source voltage are shown in Fig. 9(a) and (b) respectively. The bus voltage is 400 V and the load current is 25 A. With the rise of temperature, the turn-on process becomes slower and the turn-off process becomes faster. Those behaviors are attributed to the negative temperature coefficient of threshold voltage and positive temperature of the transconductance of selected GaN dies, which is indicated in the transfer characteristics shown in Fig. 10.



(a)



(b)

Fig. 9. Double pulse test at 25ºC and 90ºC ambient temperature showing (a) drain-source voltage waveforms at the turn-on transient and (b) drain-source voltage waveforms at the turn-off transient.

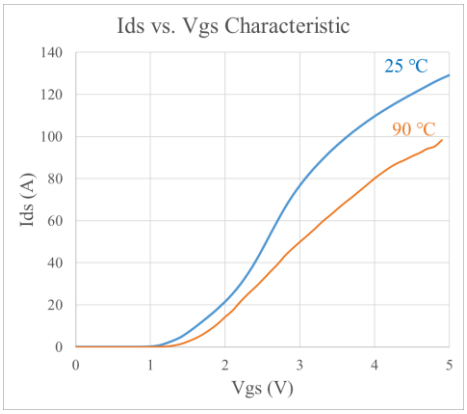


Fig. 10. Transfer characteristics of GaN HEMTs at 25ºC and 90ºC ambient temperatures.

B. *Continuous Switching Test of Power Module*

Based on the proposed embedded power module with double-sided cooling design, a buck converter is built for the power module with the integrated gate drivers as an example to demonstrate the continuous switching performance. The Fig. 11 shows the experiment setup and the heat dissipation method is liquid cooling. The proposed power module is placed on the cold plate with a thin layer of thermal interface material (TIM) in between. The input voltage is set to 120 V with a duty cycle of 0.5. The output power of the converter is kept at 500 W when the switching frequency is 600 kHz with zero-voltage switching (ZVS) to minimize switching loss and avoid any shoot-through as shown in Fig. 12.

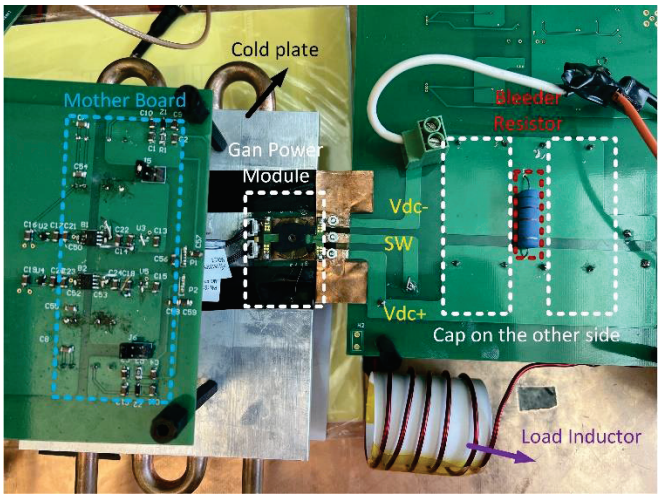


Fig. 11. Experiment setup of 500 W/ 600 kHz buck converter using the proposed power module.

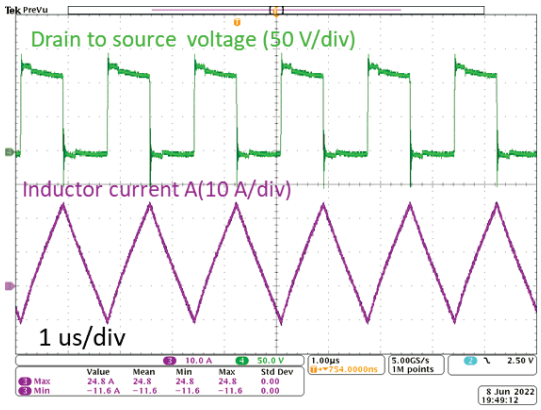


Fig. 12. Buck converter experimental waveforms of the proposed power module with 500 W output power and 600 kHz switching frequency.

C. *Thermal Resistance Measurement*

The thermal resistance of the power module fabricated is measured by applying 9.4 W loss to each die through reverse conduction. The liquid cooling method at 20 °C is adopted using the cold plate ATS-1001 from Advanced Thermal Solutions to be consistent with the thermal simulation done in FEA with the model parameters listed in Table Ⅲ. Since measuring the die junction temperature is not possible due to the embedding structure of the power module, the temperature on the top surface of the power module is measured by a thermal imager FLIR ONE as shown in Fig. 13 to indirectly verify the junction to case temperature of the module. Three points on the top surface are measured with an average temperature of 29.9 °C. In the FEA simulation, identical testing conditions are set and simulated that shows a similar top surface temperature of 29.6 °C. Therefore, consistency is verified between the simulation and experiment results, which suggests the simulated junction-to-case thermal resistance of 0.32 K/W is valid.

TABLE III. PROPERTIES OF MATERIALS IN POWER MODULE

	Layers(mm)	GaN device (mm)	Thermal Conductivity (W/m·K)
Power module board (Cu/FR4)	4×0.034 Cu		388
	3×0.066 FR4		0.25
Solder	0.100		59
Cavity board (Cu/FR4)	2×0.034 Cu	0.254	388
	0.186 FR4		0.25
Solder	0.100		59
DBC (Cu/AlN)	2×0.200 Cu		388
	0.380 AlN		170
TIM	0.100		5
ATS-1001 cold plate	15		

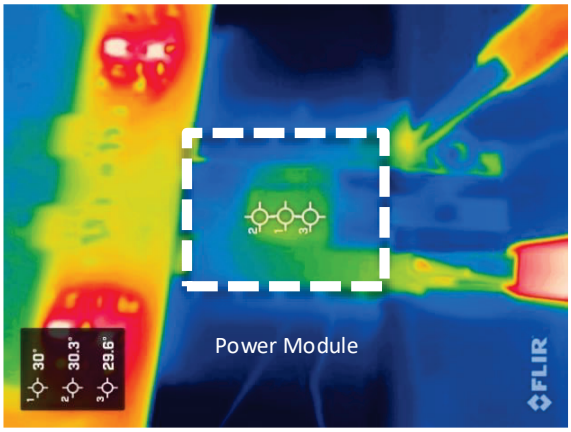


Fig. 13. Thermal image of the power module showing top surface temperatures for thermal resistance verification.

V. CONCLUSION

A compact embedded GaN half-bridge power module with double-sided cooling, low inductance, low thermal resistance, and integrated gate drivers has been proposed. Embedding technology is explored with multiple layer-attachment as a cost-effective solution to achieve double-sided cooling and enhanced design flexibility. The experimental results validate the module performance under 400 V/25 A double-pulse test with 1.03 nH power loop inductance and less than 5 % overshoot voltage. In the continuous switching test, a 500 W buck converter is built based on the presented GaN module with an operating frequency of 600 kHz. Furthermore, the proposed module is verified with thermal characterization results that shows low junction-to-case thermal resistance of 0.32 K/W. In the future work, continuous switching performance of the power module under higher power levels will be evaluated.

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